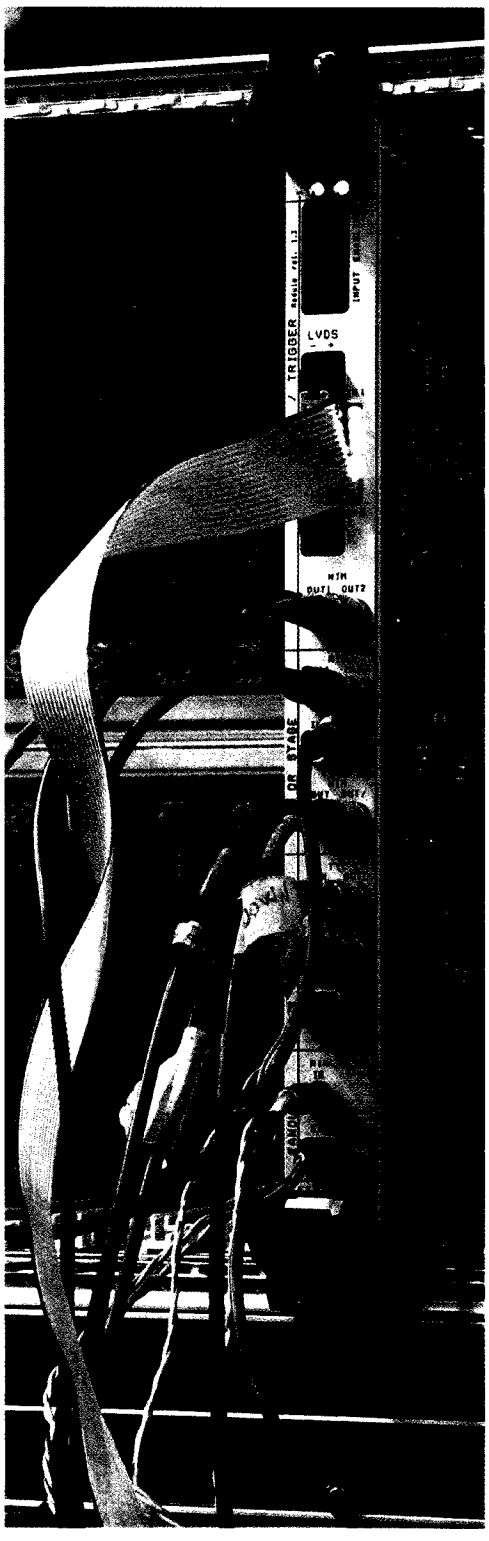
EEE Trigger Card

BASIC PRINCIPLE OF OPERATION

The DAQ of the EEE system is build around the CAEN USB-VME bridge unit. This device is easy to use (one can just plug it into any free USB port on any modern computer); however one is limited by the cycle time of USB and this would add an unacceptable overhead if one had to issue a series of VME reads on receipt of each trigger. Luckily the CAEN TDCs selected for use in the EEE project come with a built-in DAQ. Each TDCs puts data into its own FIFO every time it receives an event trigger. Thus one can read out the data asynchronically using the USB-VME bridge without imposing any dead time on the system. The TDCs also have internal counters counting the 40 MHz clock (**bunch counter** has 25 ns LSB and 12 bits, **extended time tag** has 800 ns LSB and 27 bits). It should be noted that these two



data words have to be combined together to form one time offset; this time offset is with respect to the last valid GPS time stamp. Additionally since the two TDCs have independent clocks there is no guarantee that they are both exactly 40 MHz - we will have to calibrate them. This is done by generating an event 1 second (as defined by the 1 PPS signal from the GPS) after reseting the clock. This part of the trigger logic is discussed below.

In addition to the TDC data we also need the absolute time of each event. To generate the absolute time at each EEE station we use the HYTEC GPS module. Again, due to dead time considerations, we can not read this module every event; instead we use the one pulse per second (1 PPS) to (a) create a time stamp in the GPS unit for subsequent read out and (b) reset the internal counters in the TDCs. The absolute time of an event is thus the GPS time plus an offset obtained from internal counters inside each TDC.

The LabView DAQ system running on the PC has to sort out and put the data from the two TDCs into single events and also read out the GPS unit at appropriate times and insert the GPS time values within the data stream at the correct place.

The role of the EEE trigger card is to create all the signals needed by such a system. It should be noted that 3 types of signals are used (NIM, TTL and LVDS).

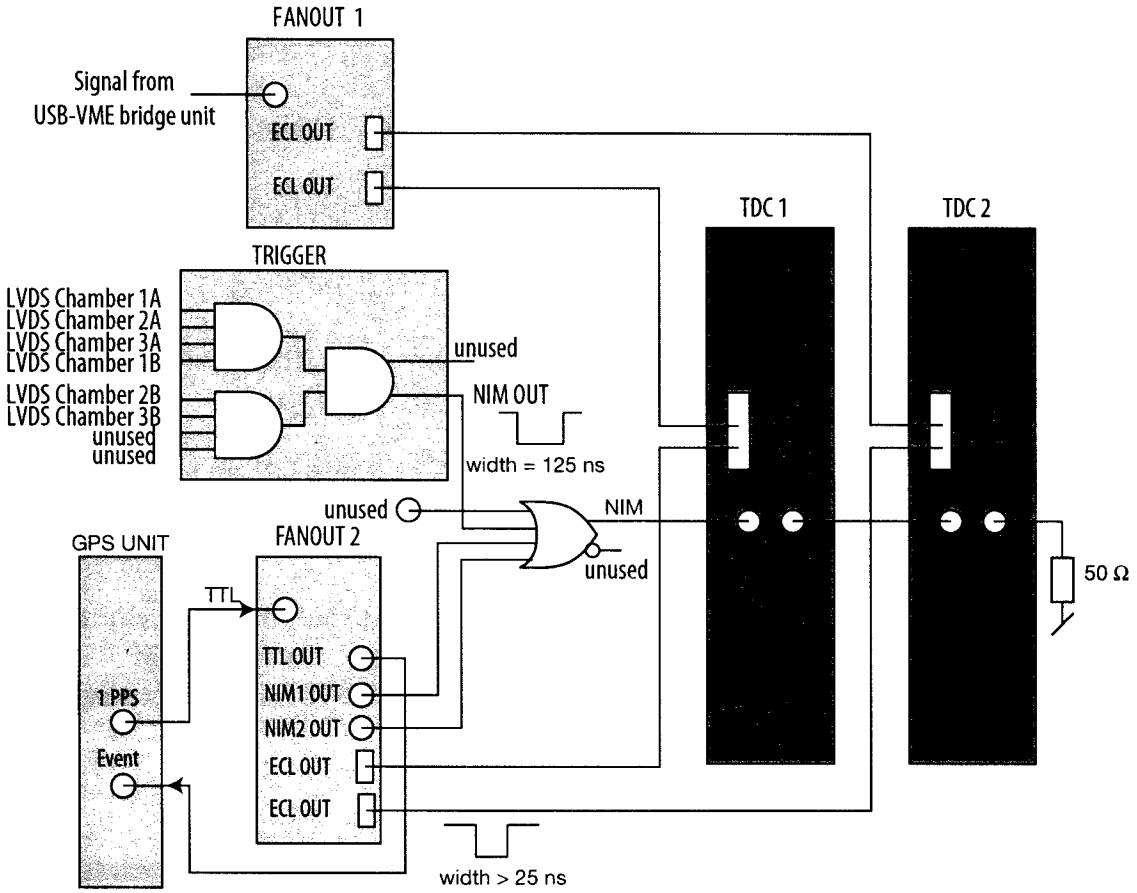
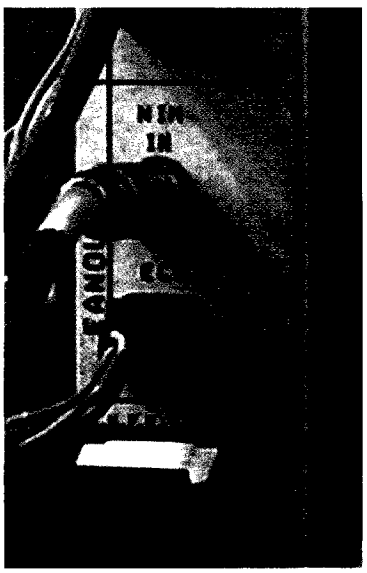


Figure 1: Block diagram of trigger card

In figure 1 we show the block diagram of the trigger logic.



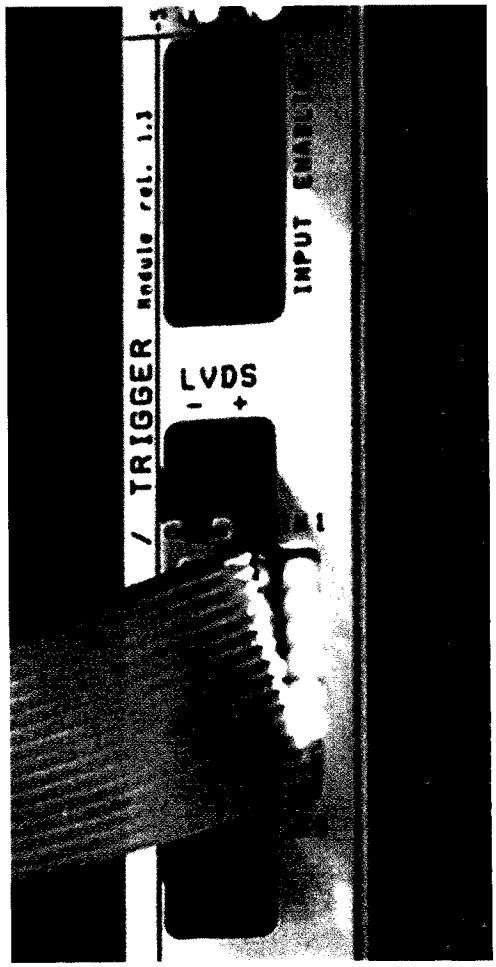
Fanout 1

Fanout 1 receives a NIM signal from the CAEN UBS-VME bridge - converts it to ECL that is then connected to the CLR inputs of the two TDC's. This signal is generated once at the start of run and it ensures that the buffers of both TDCs are cleared and the event number zeroed. The DAQ uses the event

number to match up the data from the two TDCs.

Trigger

The trigger forms the 6 fold coincidence of the trigger (3 chambers - ends A and B). Each input can be enabled/disabled by switches just above the input socket and the status shown by green LEDs next to the socket (LED ON indicates that the input is enabled).



We use flatcable to connect the trigger input signals to the trigger card. At the chamber end we simply split the flat cable into pairs and solder the pair to the 'OR output' of the frontend card.

Fanout 2

Fanout 2 receives the 1 PPS signal from the Hytec GPS unit. It generates a TTL signal that is connected to the GPS unit 'event' - this will generate a time stamp in the GPS memory that can be later read-out. There are two NIM outputs labeled OUT1 and OUT2. OUT1 is generated in time with the input from the GPS unit while OUT2 is delayed by 1.5 μ sec.

The two ECL outputs are also delayed by 1.5 μ sec and are used to reset the counters

(bunch id and extended time tag) in the TDCs (CRST). The two NIM outputs (OUT1 and OUT2) are connected to the OR STAGE and will generate events to the TDCs. OUT1 will generate an empty event (event with no hits in the chambers) but that will contain the counter values of the two TDCs that correspond to 1 sec. The TDC counters are then reset with the CRST ECL signals and another empty event is generated by OUT2. This event will have values of TDC counters close to zero. This jump in counter values is recognized by the DAQ system that will then readout the GPS time and insert a 'GPS event' into the data stream. The large delay of 1.5 μ sec between OUT1 and OUT2 is to allow for the 1 μ sec delay introduced by CAEN in the trigger signal if the search window is set to look into the future (normally the case with the EEE trigger logic).

OR STAGE

The OR STAGE is simply a 4 fold OR with the output fed to the TDCs (in daisy chain). 3 of the 4 inputs are foreseen to be in use (chamber coincidence trigger plus the two triggers generated by the 1 PPS signal of the GPS unit). There is one unused input that could be connected to another trigger source if so required.