

TOFFEE: a full custom amplifier-comparator chip for timing applications with silicon detectors

This content has been downloaded from IOPscience. Please scroll down to see the full text.

2017 JINST 12 C03031

(<http://iopscience.iop.org/1748-0221/12/03/C03031>)

View [the table of contents for this issue](#), or go to the [journal homepage](#) for more

Download details:

IP Address: 192.84.137.176

This content was downloaded on 09/03/2017 at 15:56

Please note that [terms and conditions apply](#).

You may also be interested in:

[Ultra-Fast Silicon Detectors for 4D tracking](#)

V. Sola, R. Arcidiacono, A. Bellora et al.

[Front end electronics for silicon strip detectors in 90nm CMOS technology: advantages and challenges](#)

J Kaplon and M Noy

[System-level considerations for the front-end readout ASIC in the CBM experiment from the power supply perspective](#)

K. Kasinski, P. Koczon, S. Ayet et al.

[Development of front-end electronics for LumiCal detector in CMOS 130 nm technology](#)

M. Firlej, T. Fiutowski, M. Idzik et al.

[Performance of the NA62 LAV front-end electronics](#)

A Antonelli, G Corradi, F Gonnella et al.

[A prototype of pixel readout ASIC in 65 nm CMOS technology for extreme hit rate detectors at HL-LHC](#)

A. Paternò, L. Pacher, E. Monteil et al.

[SKIROC2_CMS an ASIC for testing CMS HGCAL](#)

J. Borg, S. Callier, D. Coko et al.

[8-channel prototype of SALT readout ASIC for Upstream Tracker in the upgraded LHCb experiment](#)

C. Abellan Beteta, S. Bugiel, R. Dasgupta et al.

[Integrated input protection against discharges for Micro Pattern Gas Detectors readout ASICs](#)

T. Fiutowski, W. Dbrowski, S. Koperny et al.

RECEIVED: November 14, 2016

REVISED: January 15, 2017

ACCEPTED: February 21, 2017

PUBLISHED: March 8, 2017

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS,
26–30 SEPTEMBER 2016,
KARLSRUHE INSTITUTE OF TECHNOLOGY (KIT), KARLSRUHE, GERMANY

TOFFEE: a full custom amplifier-comparator chip for timing applications with silicon detectors

F. Cenna,^{a,b,1} N. Cartiglia,^b A. Di Francesco,^c J. Olave,^{b,d} M. Da Rocha Rolo,^b A. Rivetti,^b J.C. Silva,^c R. Silva^c and J. Varela^c

^aUniversità di Torino,
via Pietro Giuria 1, Turin, Italy

^bINFN — sez. Torino,
via Pietro Giuria 1, Turin, Italy

^cLIP,
Av. Elias Garcia 14-1, Lisbon, Portugal

^dPolitecnico di Torino,
Corso Duca degli Abruzzi 24, Turin, Italy

E-mail: cenna@to.infn.it

ABSTRACT: We report on the design of a full custom amplifier-comparator readout chip for silicon detectors with internal gain designed for precise timing applications. The ASIC has been developed in UMC 110 nm CMOS technology and is aimed to fulfill the CMS-TOTEM Precision Proton Spectrometer (CT-PPS) time resolution requirements (~ 30 ps per detector plane). It features LVDS outputs and the signal dynamic range matches the requirements of the High Precision TDC (HPTDC) system.

The preliminary measurements results with a test board are included.

KEYWORDS: Analogue electronic circuits; Front-end electronics for detector readout; VLSI circuits; Electronic detector readout concepts (solid-state)

¹Corresponding author.

Contents

1	Introduction	1
2	Ultra Fast Silicon Detectors	2
2.1	UFSD for CT-PPS	2
3	TOFFEE design overview	3
3.1	Preamplifier	3
3.2	Discriminator and stretcher	4
4	Simulations	6
5	Tests	6
6	Conclusions and future plans	7

1 Introduction

In the HL-LHC [1] environment, time tagging will be a fundamental tool due to the pile-up of events (~ 150 -200 per bunch crossing). Time tagging is needed to distinguish events overlapping in space but separated in time by a few tens of picoseconds. In the CMS-TOTEM Precision Proton Spectrometer (CT-PPS) detector [2] of the CMS experiment the reconstruction of the time information will allow to identify the correct interaction vertex by the so called z coordinate (1.1):

$$\Delta z = c\Delta(t_1 - t_2)/2, \quad (1.1)$$

where t_1 and t_2 are the time of arrival of the two leading protons of the event. By reconstructing the time coordinate with a precision of $\sigma_t \sim 20$ ps, it will be possible to determine the z position of the vertex with an accuracy of ~ 4 mm.

The timing capabilities of a sensor-front end system are determined by the characteristics of the signal at the output of the preamplifier and by the TDC binning, according to the formula (1.2)

$$\sigma_t^2 = \left(\frac{N}{\frac{dV}{dt}}\right)^2 + \left(\frac{\sigma_{\text{Bin}}}{\sqrt{12}}\right)^2 + \sigma_{\text{TimeWalk}}^2, \quad (1.2)$$

where the first term (noise-to-slope ratio) depends on the noise N and the steepness of the signal dV/dt , the second on the TDC resolution and the third on the sensor signal variations due to non homogeneous charge deposition inside the detector bulk (Landau fluctuations). A charge measurement technique, as Time Over Threshold (TOT), can be used for time walk correction.

In order to improve the time resolution it is required to minimize the noise and to have concurrently large and uniform signals from the detector and a fast readout electronics. The speed of both detector and electronics play a key role in determining the overall time resolution.

In timing applications it is important to minimize the slope-to-noise ratio, which requires electronics with fast peaking time T_p . Moreover, the speed of the sensor signal is limiting the shaping time. By considering a sensor signal collecting time T_c , an estimate of the resulting amplifier rise time can be $T_{\text{tot}} = \sqrt{T_p^2 + T_c^2}$. Being the signal slope and the amplifier noise proportional respectively to $1/T_{\text{tot}}$ and $1/\sqrt{T_p}$, the first contribution to the resolution of formula (1.2) can be approximated as

$$\sigma_t \propto \sqrt{T_p + \frac{T_c^2}{T_p}} \quad (1.3)$$

which has a minimum for a peaking time as close as possible to the charge collection time of the sensor [3].

2 Ultra Fast Silicon Detectors

Ultra Fast Silicon Detectors (UFSD) [4] have been designed with the aim to reconstruct the time coordinate of a particle with a silicon detector. A p^+ implant (gain layer) below the n^{++} electrode produces a high electric field zone which allows multiplying the charge carriers generated by an impinging particle. When crossing the gain layer, electrons multiply via impact ionization mechanism [5] and produce additional electrons and holes (gain electrons and gain holes). The gain electrons are soon collected, while the gain holes drifting to the p^{++} electrode generate a large current. UFSD have low gain (~ 10 -20) when compared with similar devices like APDs and allows to keep the multiplication noise low. Low gain also leads to milder electric fields, which makes the electrodes segmentation easier and the overall behavior similar to the one of standard silicon detectors.

The signal shape depends on the sensor thickness, in particular the amplitude depends on the gain value while the length on the bulk thickness. For a fixed gain value the signal amplitude is constant while the rise time decreases with decreasing thickness.

A sensor thickness of $50 \mu\text{m}$ and a gain value of ~ 15 have been chosen. UFSD current signals have been simulated with the program *Weightfield2* [6] and TCAD Synopsys Sentaurus: the typical signal produced by a minimum ionizing particle (MIP) impinging on a $50 \mu\text{m}$ thick UFSD with a gain of ~ 15 has a total length of $\sim 1.2 \text{ ns}$ [7], delivering a charge of $\sim 8 \text{ fC}$ to the amplifier stage.

2.1 UFSD for CT-PPS

The UFSD specifically designed for the CMS-TOTEM Precision Proton Spectrometer and produced by CNM (Centro Nacional de Microelectrónica, Barcelona) features a 32 fat strip array with a dead space between strips of $50 \mu\text{m}$. In this array, the 16 strips closer to beam line are narrower ($3 \text{ mm} \times 0.5 \text{ mm}$) and have a capacitance of 3 pF while the 16 strips further away are wider ($3 \text{ mm} \times 1 \text{ mm}$), with a capacitance of 6 pF .

The sensor has a nominal gain of ~ 15 . The signal from each strip will be detected by a DC-coupled front-end mounted close to the detector module inside the PPS roman pot (RP).

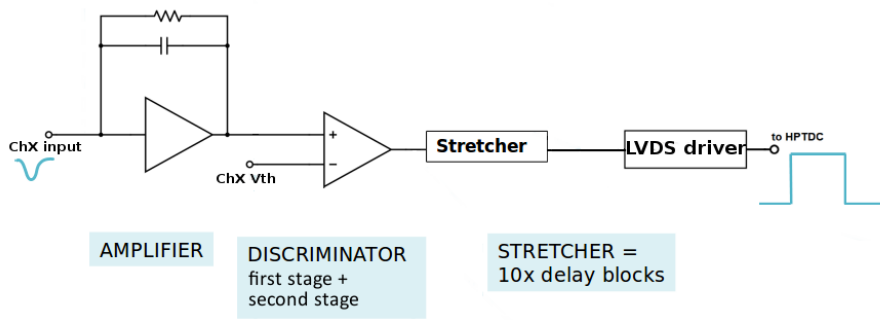


Figure 1. TOFFEE signal processing chain.

3 TOFFEE design overview

TOFFEE (Time Of Flight Front-End Electronics) is an 8 channels front end ASIC for UFSD read out, designed in standard 110nm CMOS technology. Each channel is independent and the signal processing chain, depicted in figure 1, is composed by: (i) transimpedance amplifier, (ii) single threshold discriminator, (iii) stretcher and (iv) LVDS driver. The High Precision TDC (HPTDC) [8] is a general purpose data driven multi-hit time-to-digital converter. The dead time between hits requires a minimum pulse width to enable the measurement of the leading and trailing edges of the pulse. A stretcher is used to widen the discriminator output in order to produce a pulse wider than 5 ns, as required by HPTDC. TOT technique is used for time walk correction.

The ASIC is optimized for a sensor capacitance of 3-10 pF and an input charge between 3 and 30 fC. The total power budget per channel is less than 30 mW, constrained by thermal dissipation in the RPs used for the CT-PPS detector. The output format matches HPTDC inputs through LVDS links (32 pairs per detector module), which consume 10 mW of the power budget per channel.

3.1 Preamplifier

The preamplifier (figure 2) is implemented with a telescopic cascode common source amplifier with split bias current and NMOS input transistor. The bias current is provided by two independent branches. The left branch is powering the cascode transistors $M3$ and $M2$ with a current properly chosen to meet the desired specs of output swing and slew rate. Taking into account that by reducing this current the output swing increases but the slew rate decreases, appears clear that a trade off is necessary. The value chosen for this current is $200 \mu\text{A}$. The right branch delivers a current of $\sim 12 \text{ mA}$ to the input transistor $M1$ and thus the most of the bias current. Thanks to this branch the current can be kept high to increase the transconductance g_{m1} without reducing the output swing of the stage [3].

The value of the current in transistor $M1$, its transconductance g_{m1} and dimensions have been chosen to reach a high gain and a unity-gain-frequency of 14 GHz, to cope with the short collection time T_c of the sensor. The power consumption is 14.4 mW, within the specification requirements of less than 20 mW.

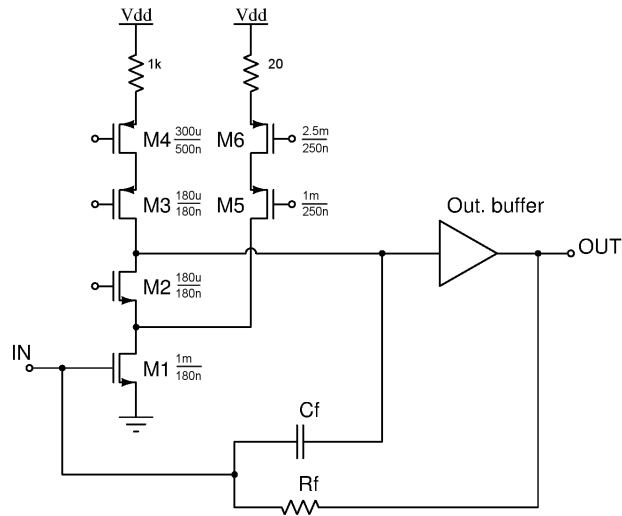


Figure 2. Preamplifier architecture.

From the transconductance and the drain-to-source resistance of the transistors of the telescopic cascode it is possible to estimate the DC gain as:

$$A_v = -g_{m1} \frac{(r_{ds1} g_{m2} r_{ds2})(r_{ds4} g_{m3} r_{ds3})}{r_{ds1} g_{m2} r_{ds2} + r_{ds4} g_{m3} r_{ds3}} \approx 212 \quad (3.1)$$

in good agreement with simulations results ($A_v = -255$).

The amplifier also features resistors for noise degeneration and an output buffer for load driving. The latter is implemented with a source follower with local feedback, in order to maximize the output swing.

Noise analysis. The noise contribution sources of the preamplifier is analyzed in a qualitative way. The three cascode transistors **M2**, **M3** and **M5** can be seen as three different source degenerated amplifiers where the degeneration role is played respectively by **M1**, **M4** and **M6**. Therefore, their equivalent transconductances appear to be negligible if compared with the one of their degeneration transistors making the noise contribution of these devices small [3]. The same concept is applied also to transistors **M4** and **M6** where the degeneration has been obtained with the use of a couple of resistors as depicted in figure 2. These considerations leads to an expected main contribution due to transistor **M1**.

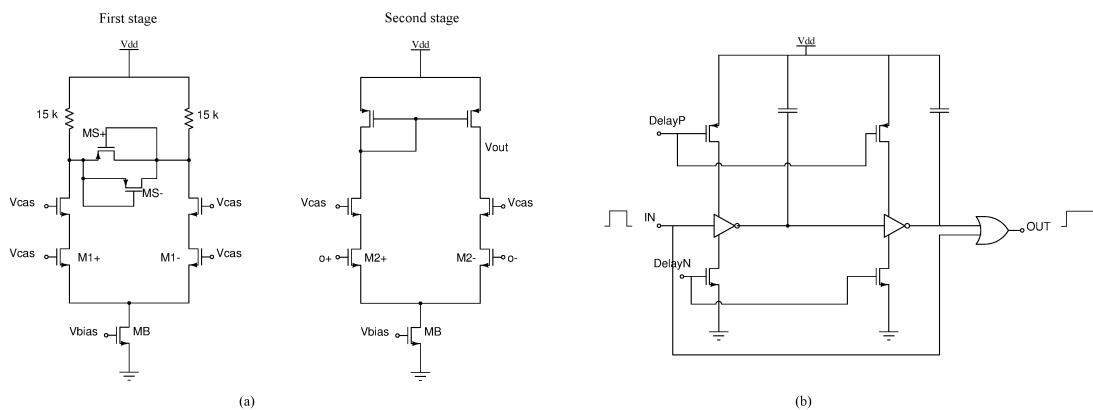
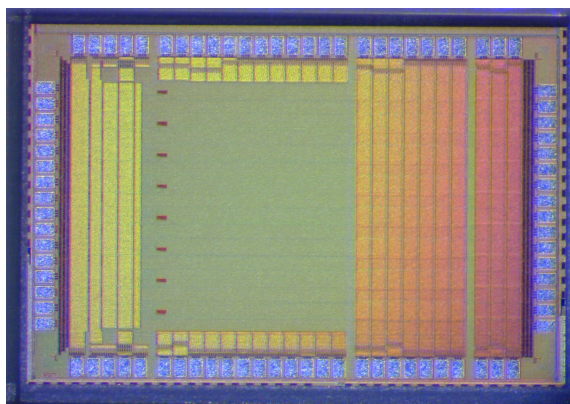
This is confirmed by simulations results in table 1, in which it is shown that transistor **M1** contributes for more than 50% to the total noise of the telescopic cascode.

3.2 Discriminator and stretcher

To achieve the highest speed, the discriminator is implemented with a cascade of two stages (figure 3.a). The total gain of the comparator is then given by the product of the gains of the cascaded stages [3]. The first is a differential pair which further increases the gain of the amplifier, while the second is a single threshold discriminator.

Table 1. Noise contribution of the transistors of the telescopic cascode.

Transistor	Weight (Simulation)
M1	63%
M2	24%
M3	2.2%
M4	5.5%

**Figure 3.** The figure shows in (a) two stages of the discriminator and in (b) one of the ten blocks composing the stretcher.**Figure 4.** A microscope caption of TOFFEE.

The stretcher is composed of ten consecutive digital delay blocks (figure 3.b). Each block is formed by an inverter and two starving transistors: the amount of delay added to the signal is tuned by the gate voltage applied to them.

TOFFEE features a preamplifier gain of ~ 7 mV/fC, a gain-bandwidth of 14 GHz, a RMS noise of ~ 800 μ V (for a detector capacitance of 6 pF) and a power consumption of ~ 25 mW per channel. The preamplifier is the main contribution to the power consumption of the analog domain (~ 15 mW), while the discriminator contributes with ~ 230 μ W, being the power dissipated by the digital stretcher negligible. The estimated power consumption of the LVDS driver is ~ 10 mW.

The ASIC has been received from foundry in September 2016. A sample is shown in figure 4.

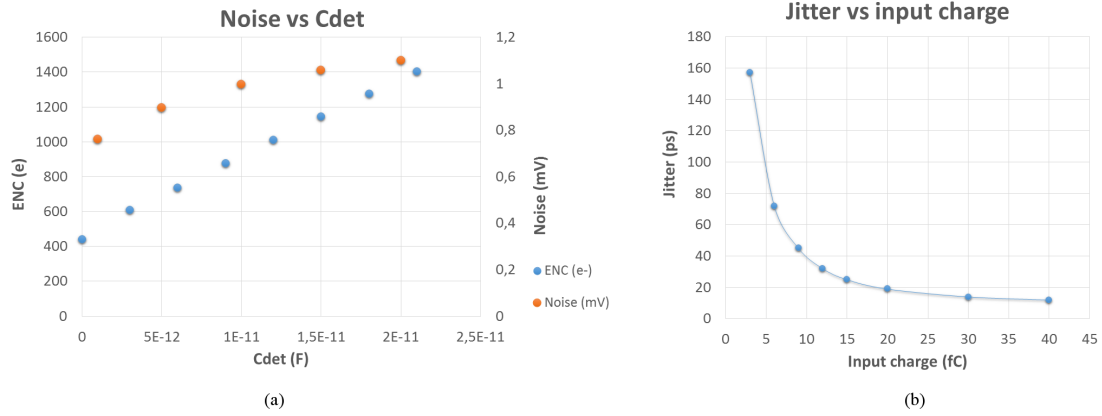


Figure 5. (a) Simulated amplifier output noise as a function of detector capacitance. (b) Jitter as a function of input charge from post-layout simulations for a detector capacitance of 6 pF and an input charge of 8 fC.

4 Simulations

According to simulations, the preamplifier signal has a peaking time of ~ 2 ns in schematic and ~ 3 ns in post-layout simulations and then can be compared to the T_c of UFSD sensors. The typical expected charge from the sensors is in the range between 5 and 10 fC.

Simulations have been performed to study the dependency of the Equivalent Noise Charge (ENC) from the detector capacitance. The results, summarized in figure 5.a, show an increase of the ENC for detectors with bigger capacitance as expected. Concerning the jitter, it has been evaluated with post-layout simulations as a function of the input charge. A time resolution of ~ 45 ps is expected from one single detector for a MIP signal (~ 8 fC) and a detector capacitance of 6 pF as displayed in figure 5.b. This result can be additionally improved by using more planes in parallel where the time resolution is

$$\sigma_t = \frac{\text{jitter}}{\sqrt{N_{\text{planes}}}} \quad (4.1)$$

leading to a ~ 22 ps time resolution with $N_{\text{planes}} = 4$.

The estimated time walk, i.e. the spread of the Time of Arrival (ToA) distribution without ToT correction is ~ 1.3 ns. With ToT correction we expect a time walk jitter contribution of ~ 30 ps.

5 Tests

TOFFEE tests started in October 2016 using a first version of custom boards. These preliminary tests are performed injecting a square input signal to the channels of the chip by using a pulse generator and a RC filter. Amplitude and width have been chosen in order to reproduce the expected sensor signal slew rate whereas the values of R and C are chosen in order to emulate the signal shape of UFSD sensors.

The injected signal has an amplitude of 4.8V, rise and fall times of 2.5 ns, a frequency of 100 kHz and a width of $1.38 \mu\text{s}$ and is locked to a TTL trigger sent to an oscilloscope. The amplitude allows to maximise the pulser signal-to-noise ratio but this requires the use of a 50 dB attenuator to avoid the preamplifier saturation. The values chosen for the filter are $R = 1 \text{ k}\Omega$ and $C = 1 \text{ pF}$, in order to reproduce the charge collection time of the UFSD sensors. A DAC board is used to

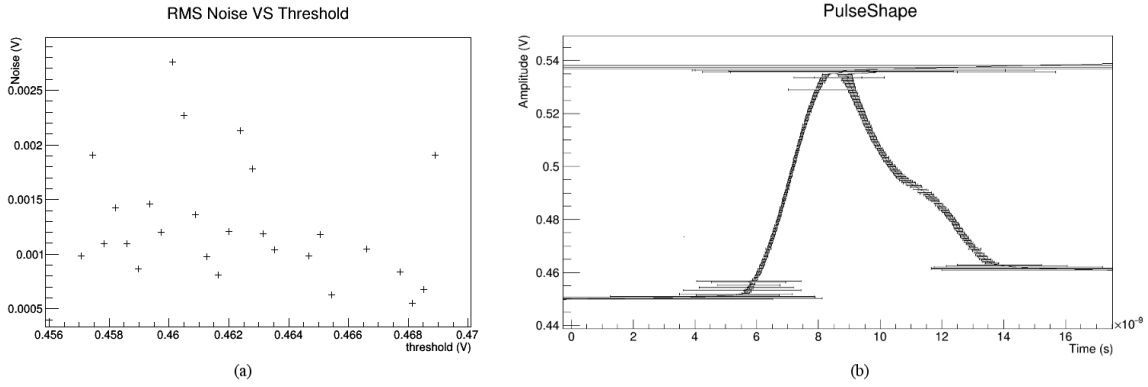


Figure 6. (a) Measured noise as a function of the threshold voltage for 1 pF input capacitance. (b) Reconstructed pulse shape from threshold voltage (amplitude), time of arrival and time over threshold (time).

automatically set the discriminator threshold voltage with a remote computer. A 1 k Ω resistor in series with the DAC output ensures the stability of the DAC board driver.

The LVDS output of TOFFEE is read by a differential probe connected to the oscilloscope, which automatically measures the delay between the trigger signal and the LVDS signal, calculates the average and the standard deviation σ . The noise is evaluated from the slew rate and jitter of the output signal at various threshold values. The measured values, shown in (figure 6.a), are compatible with simulations.

The pulse shape has been reconstructed using the time of arrival and time over threshold measured on the oscilloscope, as shown in figure 6.b. It shows a signal of amplitude 110 mV with peaking time 3 ns, compatible with expectations for the signal of an UFSD with the same charge.

By varying the discriminator threshold voltage it has been possible to measure (i) the signal slew rate dV/dt

$$SR = \frac{V_{th2} - V_{th1}}{\text{mean}_2 - \text{mean}_1} = 25 \text{ mV/ns}, \quad (5.1)$$

(ii) the jitter of the TOFFEE + pulse generator system $\sigma = 44 \text{ ps}$ and (iii) to evaluate the noise

$$\text{Noise} = SR \cdot \sigma = 1.1 \text{ mV}. \quad (5.2)$$

These three values are consistent with simulations.

To measure the ASIC contribution to the total jitter as a function of the input charge the previously described setup has been used. The input charge Q_{in} can be varied by sweeping the pulse amplitude V_{pulse} following the relation $Q_{in} = C \cdot V_{pulse}/\text{attenuation}$. The total jitter read at the oscilloscope (LVDS jitter) comprises the contributions of pulse generator jitter and the one from the ASIC, as shown in figure 7. For a charge of $\sim 12 \text{ fC}$ the expected resolution is $\sim 36 \text{ ps}$.

6 Conclusions and future plans

A full-custom amplifier comparator ASIC have been developed to read-out silicon detectors for timing applications. TOFFEE's amplifier rise-time ($\sim 2\text{-}3 \text{ ns}$) and slope ($> 20 \text{ mV/ns}$) allow minimizing the front-end jitter: according to simulations, for a single TOFFEE-UFSD system the

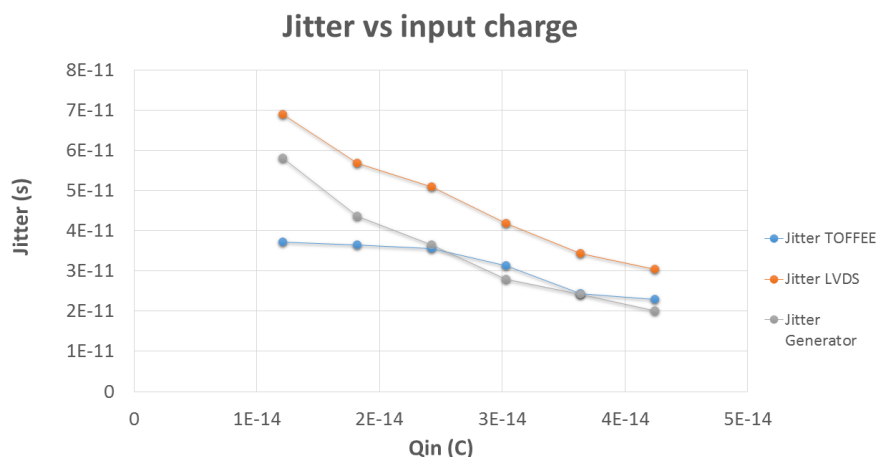


Figure 7. Measured jitter as a function of the injected charge for an input capacitance of 1 pF.

time resolutions is ~ 45 ps for a typical 8 fC MIP signal and a detector capacitance of 6 pF. The time resolution can be further improved by using more modules in parallel: with 4 modules a resolution of 22 ps can be reached, satisfying the CT-PPS requirements.

The measured time resolution for a ~ 12 fC signal is ~ 36 ps.

A more reliable measurement needs the use of the real sensors instead of the test pulse. For this reason tests with UFSD sensors + TOFFEE and a new custom board are foreseen for the beginning of 2017.

Acknowledgments

Special thanks to Miguel Silveira and Ricardo Bugalho (PETsys Electronics).

Part of this work has been financed by the European Union's Horizon 2020 Research and Innovation funding program, Grant Agreement no. 669529 (ERC UFSD669529), by the Italian Ministero degli Affari Esteri and INFN Gruppo V and COST Action TD1401 Fast Advanced Scintillation Timing, supported by COST (European Cooperation in Science and Technology).

References

- [1] A. Barachetti et al., *HiLumi LHC: P7 High Luminosity Large Hadron Collider design study final project report*, [CERN-ACC-2016-0007](#), CERN, Geneva Switzerland, (2016).
- [2] M. Albrow et al., *CMS-TOTEM precision proton spectrometer*, [CERN-LHCC-2014-021](#), CERN, Geneva Switzerland, (2014) [CMS-TDR-013] [TOTEM-TDR-003].
- [3] A. Rivetti, *CMOS: front-end electronics for radiation sensors*, CAT# K15985, Taylor & Francis, U.K., (2015) [ISBN:9781466563100].
- [4] H.F.W. Sadrozinski et al., *Ultra-fast silicon detectors*, [Nucl. Instrum. Meth. A](#) **730** (2013) 226.
- [5] W. Maes, K. De Meyer and R. Van Overstraeten, *Impact ionization in silicon, a review and update*, [Solid-State Electron.](#) **33** (1990) 705.

- [6] F. Cenna et al., *Weightfield2: a fast simulator for silicon and diamond solid state detector*, *Nucl. Instrum. Meth. A* **796** (2015) 149.
- [7] N. Cartiglia et al., *Design optimization of ultra-fast silicon detectors*, *Nucl. Instrum. Meth. A* **796** (2015) 141.
- [8] J. Christiansen, *HPTDC, High Performance Time to Digital Converter version 2.2*, http://tdc.web.cern.ch/tdc/hptdc/docs/hptdc_manual_ver2.2.pdf, CERN-EP/MIC, CERN, Geneva Switzerland, (2004).