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A multichannel front-end readout ASIC for picosecond time resolution systems based on thin UFSD

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Abstract: This work presents FAST, a multichannel readout ASIC designed to measure the time of arrival of MIP particles in Ultra-Fast Silicon Detectors (UFSD) with a time resolution of about 30 ps. The FAST ASIC is oriented to future High Energy Physics experiments, where high time resolution is exploited to mitigate pile-up effects, and more generally, to those applications that require accurate Time-of-Flight Silicon systems with low power consumption. The prototype has been designed in 110 nm CMOS technology, in three different flavors of front-end architecture. Each flavor is implemented in a different 20-channel ASIC. For all flavors, the power consumption of the front-end is 1.2 mW/channel. The three flavors of FAST are described in the paper, together with the simulation showing the timing performance of FAST coupled to different sensors geometries.

Keywords: Analogue electronic circuits; Front-end electronics for detector readout; Timing detectors

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1 Introduction

The future generation of High Energy Physics (HEP) experiments will push higher the instantaneous luminosity, for example at the High Luminosity-LHC (HL-LHC) it will increase by a factor of five. At HL-LHC, this increase leads to about 200 nearly-simultaneous pileup interactions per bunch crossing [1]: high precision timing measurement is a powerful tool to disentangle the different interactions and therefore mitigate pile-up effects. To this end, dedicated MIP timing layers are planned in the upgrade of the HL-LHC experiments: the High Granularity Timing Detector (HGTD) for ATLAS and the MIP Timing Detector (MTD) for CMS are two examples of such detectors [1, 2]. Another example of a high precision Time-Of-Flight (TOF) measurement at LHC is provided by the CT-PPS spectrometer operated by the TOTEM-CMS experiments. Also in this case, a precision of 20–30 ps is required [3] while the power consumption limit is more relaxed (tens of mW/channel) than those expected for the CMS and ATLAS timing layers (about 3 mW/channel for the CMS MTD [1]).

Generally, the measurement of a particle Time-Of-Arrival (ToA) in a system is affected by uncertainties stemming from both the sensor and the readout electronics. For a simple model composed of a silicon sensor coupled with its readout electronics, equation (1.1) shows the most important contributions that affect the time resolution σ_t in a timing detector. The terms $\sigma_{\text{landau noise}}$ and $\sigma_{\text{distortion}}$ depend on the sensor [4] whereas the other terms depend purely on the electronics. In particular, the σ_{jitter} term depends upon the front-end electronics properties such as the slew rate and the noise. $\sigma_{\text{time walk}}$ is due to the signal amplitude variation on an event-to-event basis and generally its contribution depends upon the discriminator properties. When using a leading-edge discriminator, as it is in this work, it can be corrected off-line with the Time-over-Threshold (ToT) technique. The last term, σ_{TDC}, depends on the Time-to-Digital Converter (TDC) used to readout the discriminator output.

$$\sigma_t^2 = \sigma_{\text{landau noise}}^2 + \sigma_{\text{distortion}}^2 + \sigma_{\text{time walk}}^2 + \sigma_{\text{jitter}}^2 + \sigma_{\text{TDC}}^2 \tag{1.1}$$

The term $\sigma_{\text{distortion}}$ can be minimized by an accurate sensor design (uniform weighting field, saturated electron-holes velocity [5]) while $\sigma_{\text{landau noise}}$ can be minimized using thin sensors. A good example of optimized devices with these properties are the Ultra Fast Silicon Detectors (UFSD). These sensors are thin Low Gain Avalanche Detectors (LGADs) able to generate signals of about 10 µA with a duration T_c (collection time) of 1.2 ns. Thanks to this property, UFSD are considered suitable for applications where picosecond resolution and radiation tolerance up to 10^{15} n_{eq}/cm^2 are required [6]. The requirement of having a fast peaking time T_p has repercussions also on the electronics optimization and demands a front-end design that minimizes the noise to slope ratio as much as possible. Formula 1.2 shows the noise to slope ratio $\sigma_v/(\partial V/\partial t)$ expressed as a function of T_c and T_p. By considering constant the proportional factor k, σ_{jitter} reaches the minimum when T_p equals T_c [7].

$$\sigma_{\text{jitter}} = \frac{\sigma_v}{\frac{\partial V}{\partial t}} = k \cdot \sqrt{T_p + \frac{T_c^2}{T_p}} \tag{1.2}$$

Peaking times T_p shorter or longer than the optimum value degrade the time resolution. In the first case, the front-end is so fast that it follows correctly the signal shape generated by the sensor, but the noise will dominate due to the large bandwidth, degrading the overall timing performance. In the second case, the noise will be low since the bandwidth is reduced, however, the time resolution is degraded by the limited slew rate of the amplifier. It is therefore clear that T_p must be well tuned to reach a high time resolution and that a combined sensor-front-end development is mandatory. In addition to the bandwidth optimization, all other noise sources of the front-end must be reduced as well. Particular attention must be paid in sizing the input transistor because it can compromise completely the system performance.

This work presents the design and the simulation results for three front-ends, each optimized to minimize the jitter using a reference sensor capacitances C_{det} of 6 pF and keeping the power consumption as low as possible (goal about 1.2 mW/channel). The paper is organized as follows: in the next section the FAST ASIC is described focusing the attention in the description of the channel architecture. In section 2.2 the proposed front-ends are described in detail. The simulated timing performances of FAST coupled with UFSD, taking into account most part of the terms reported in Formula 1.1, are discussed in section 3.2. The last section is dedicated to the project summary, the paper conclusion and the outlooks of this work.

2 The FAST ASIC: general description of the prototype

The FAST ASIC has been developed aiming to achieve a 30 ps time precision when coupled to thin UFSD. Three different flavors of the FAST ASIC were manufactured, using a few different technical choices, all designed in a 110 nm with 1-poly 8-metal layers. Each flavor is implemented in a chip of 1.6 mm × 5 mm, consisting of 20 independent channels. The chip output signal, a step starting at ToA and with a duration equal to ToT, is in LVDS format, chosen to be compatible with commercial devices like TDCs and FPGAs, is common to the three flavors.

Each channel is 0.17 mm wide and 1.2 mm long. The 20 channels are arranged along the short side of the chip as depicted in figure 1, with a channel input pitch of 170 µm.

FAST has been designed to manage an injected charge dynamic range between 3 fC and 60 fC: as a reference, the charge Most Probable Value (MPV) expected from a 55 µm thick UFSD with a

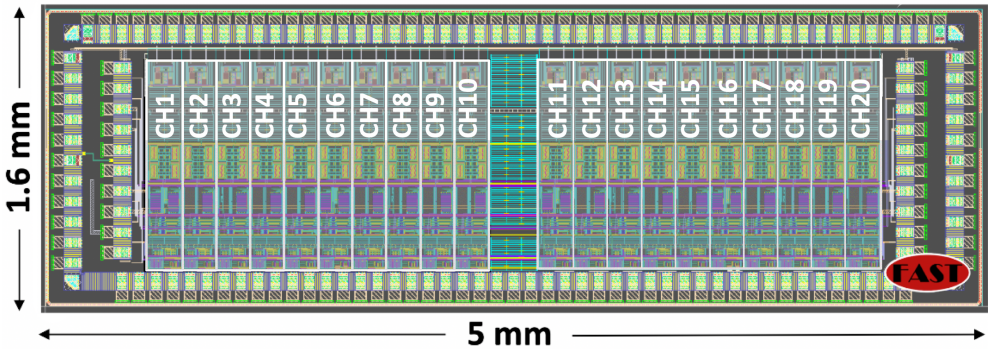


Figure 1. Layout of the full chip. Inputs and LVDS outputs are physically located at the bottom and top of the picture, respectively. PADs on the right and left are used to provide the bias signals.

gain of 15 is about 8 fC. All three front-ends are designed to work with C_{det} between 2–10 pF (6 pF is the nominal one) and with a power consumption for the analog domain limited to 1.2 mW per channel. These values, together with other specifications are summarized in table 1.

Number of channels	20	Typical RMS noise	1–3 mV
Number of FAST flavors	3	Front-end power consumption	< 1.2 mW/ch
Operation voltage	1.2 V	Driver power consumption	1 mW/ch
Die size	1.6×5 mm^2	Time walk correction	based on ToT
Sensor capacitance	2–6 pF	MPV (in 55 µm thick UFSD)	8 fC
Typical SNR	60	Input dynamic range	1–60 fC

Table 1. Table of specifications for the design of FAST.

2.1 The channel architecture

The channels of the three flavors are arranged in the same way: the input current signal coming from the sensor is converted by the first stage into a voltage signal and amplified minimizing the noise to slope ratio. This block defines the timing properties of the whole channel and for this reason the largest part of the power is used here. Once amplified, the signal is first digitized by a two-stage leading-edge discriminator (DISC1 and DISC2) and then it is sent to a pulse width regulator (PWR) that adds an adjustable time Δt (up to 6 ns) to the digital output duration. The PWR is used for compatibility with commercial TDCs which requires a minimum pulse duration of a few ns and, if not needed, it can also be turned off. The chain ends with the LVDS driver which sends the information off-chip allowing to drive output loads up to 5 pF preserving the timing properties of the front-end.

Figure 2 shows a block diagram of the circuit described above, connected to a sensor via wire bonding. Since the most crucial block is the very front-end, three possible flavors have been explored. The three ASICs are named FAST-REG, FAST-EVO1 and FAST-EVO2; they are described in the next section.

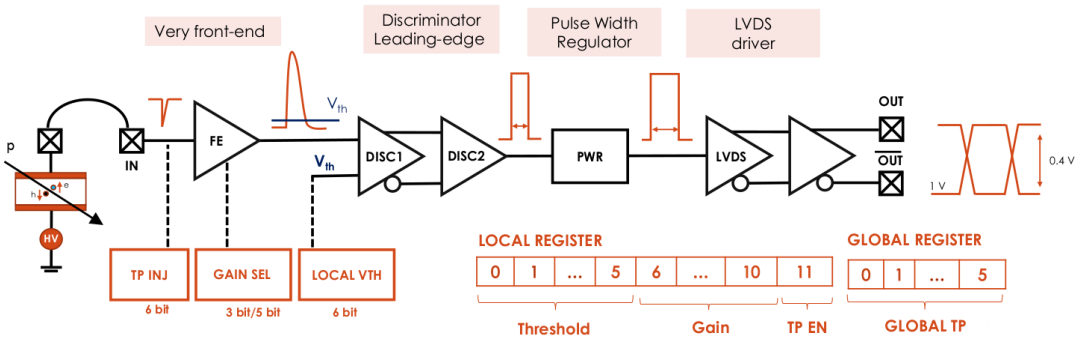


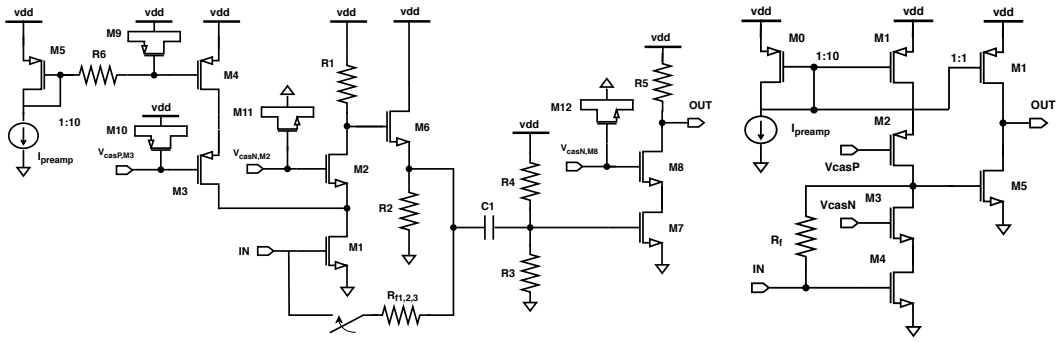
Figure 2. Scheme of the readout electronics implemented in the channels of FAST.

Mixed-signal circuitry is used to modify a few properties of the front-end, for example the analog gain, or simply for testing purposes. An example of built-in testing capabilities is the possibility, using a 6-bit programmable DAC, to inject charge (between 1 fC and 20 fC) in the front-end. A 6-bit DAC is implemented for the local threshold tuning required to reduce the fabrication mismatch effects among the channels.

2.2 The front-end architectures

The three FAST front-ends are based on Trans-Impedance Amplifiers (TIA). Power consumption, bandwidth and noise are the major factors to consider in the jitter minimization of the amplifiers. A design effort has been made sizing the input transistor to limit the noise as much as possible. In all flavors, its geometry has been chosen large enough to maximize the transconductance g_m while reducing the $1/f$ spectral density. On the other hand, the device has been kept as small as possible to avoid the increase of the total input capacitance which contributes to both the thermal and the flicker noise. Considering for instance the EVO flavors, the best balance corresponds to an input transistor having a width of 18 µm and length of 0.36 µm. The input transistor operates in weak inversion to maximize its g_m and thus reducing the TIA input impedance. This allows keeping the bandwidth wide also when using large sensors of a few pF capacitance. Two TIA architectures (REG and EVO), inspired by previous prototypes [8, 9], are proposed to explore different combinations of bandwidth and noise. Since the transistor type can affect the maximum value of g_m, also a third flavor, based on the EVO architecture (and thus called EVO2) and using radio frequency transistors, has also been included.

The TIA architecture used for the EVO and REG flavors are depicted in figure 3. The EVO architecture is based on a buffered broadband amplifier in TIA configuration followed by a cascode common source amplifier. In these blocks, the bandwidth is increased by means of some design techniques like the use of n-type cascodes to minimize the Miller effect for the input transistors and the use of resistors to reduce the introduction of parasitics. The core amplifier gain of the first stage is maximized by using two branches connected to the input transistor drain. The first branch is made by M1, M2 and R1 and sinks a small current of 80 µA that allows using high values of R_1 and consequently to increase the gain. The second branch is a cascode current mirror made by M3 and M4. It provides a current up to 1 mA to M1, increasing its transconductance g_m and thus also the open-loop gain of the amplifier. With a nominal current of 1.2 mA the gain of this amplifier is



(a) Front-end of the EVO flavors **(b)** Front-end of the REG flavor

Figure 3. FAST Front-end amplifiers. On the left the architecture solution adopted for REG and on the right the EVO.

35 dB. The broadband is buffered by an N-type source follower. The TIA configuration is obtained connecting the resistor R_f in the feedback of the broadband amplifier. The gain of the stage is defined by selecting in the channel configuration register one of three possible values of R_f. Since the bandwidth depends on R_f, the feedback resistor also determines three different bandwidths: 230 MHz, 580 MHz (nominal) and 665 MHz obtained with R_f values of 31.6 kΩ, 11.6 kΩ and 5.3 kΩ, respectively. The nominal bandwidth has a peaking time of 600 ps. Noise at the TIA output in nominal conditions is 770 µV rms, where the largest contribution comes from the thermal noise related to R_f. The second amplification stage is used to obtain large signal amplitudes aiming at reducing the time walk in the leading-edge discriminator. This block is AC coupled to the TIA amplifier to filter noise, low frequency variations due to sensor leakage current and voltage shifts due to fabrication process mismatch that may affect the operation point of the second stage input transistor. This second stage is a cascode common source with sufficient bandwidth to preserve the timing properties of the input signal. The input transistor polarization is provided by a dedicated bias made by R3 and R4. Power consumption is 60 µV and gain is 13.6 dB for frequencies between 550 kHz and 470 MHz. The signal processing chain made by the two stages so far described can be seen as a pass-band TIA amplifier with multiple gains of 25 kV/A, 55 kV/A (nominal) and 146 kV/A. In the nominal condition, the total simulated noise is 2.7 mV rms.

The REG flavor depicted in figure 3b is a TIA amplifier with a core amplifier based on a splitted cascode common source amplifier. The TIA is followed by a common source amplifier. In this architecture active loads are used to increase the open loop gain at the price of limiting the bandwidth to 100 MHz. Only one feedback resistor is used in this flavor and it fixes the gain to 179 kV/A. Power consumption is 1.2 mW. More details can be found in [10].

3 Timing performance of FAST

The signal shape sent to the discriminator defines important properties of the front-end such as jitter and the maximum tolerated rate. In particular, signals with long tails limit the input rate because of the long time they need to restore the baseline. In the following, post-layout simulations are discussed describing the timing performance in terms of jitter and rate of the proposed front-ends.

3.1 Signal shape, jitter and rate

The simulated response of the FAST EVO2 amplifier to an 8 fC delta function is shown in figure 4 (left) as the sensor input capacitance is varied between 2 and 20 pF. The simulation shows that signals are modulated both in amplitude and duration based on the sensor capacitance. In particular, when the input capacitance is limited to 2 pF, the signal amplitude is about 500 mV voltage and the duration is 2.5 ns. In this case the maximum tolerated rate is 400 MHz. The signal duration with a load of 20 pF sensors is 12 ns and the maximum rate falls to ~ 80 MHz. The configurable gain of the EVO channels allows obtaining three different signal shapes for each capacitive load, tuning the maximum tolerated rate. Figure 4 (right) shows these analog outputs (EVO2) expected for an 8 fC delta shape, with a sensor of 6 pF. The minimum gain (green curve), producing a narrower signal (3 ns), increases the tolerated rate to ~ 300 MHz.

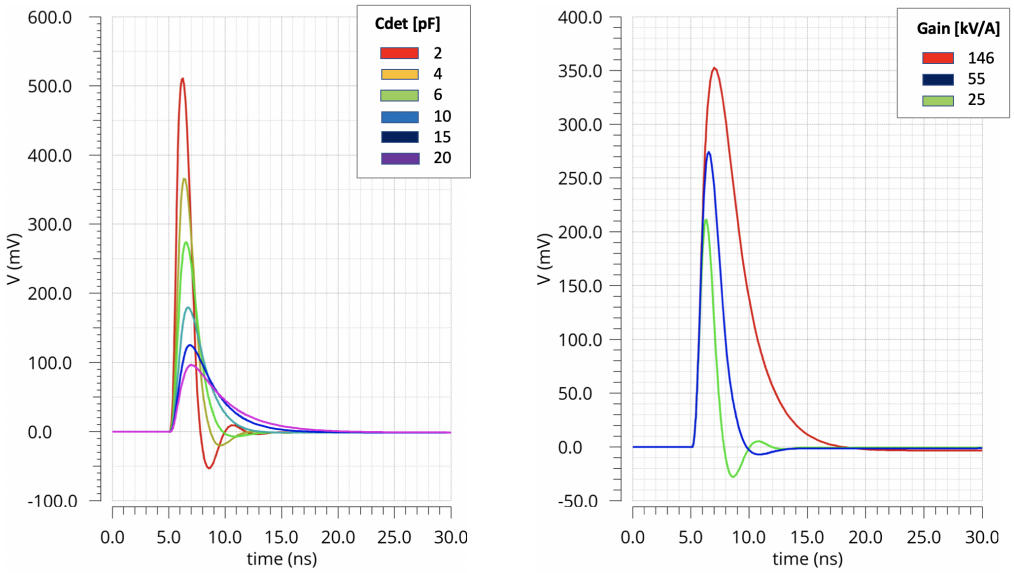


Figure 4. On the left the analog output of EVO2 with a delta shape input of 8 fC for sensor capacitance from 2 to 20 pF. The gain of the front-end is 55 kV/A (nominal value). On the right effects in the signal shape of EVO2 due to the programmable gain with C_{det} equal to 6 pF. Also in this case the input is 8 fC.

Gain [kV/A]	Input resistance [Ω]	Amplitude [mV]	Jitter [ps]	RMS noise [mV]	Max rate [MHz]
25	90	211	19.8	2.6	300
55	165	274	18.5	2.7	227
146	490	352	19.8	3.4	128

Table 2. Timing properties of EVO2 for different gains. The input is a delta shape of 8 fC and the sensor has a capacitance of 6 pF.

Table 2 summarizes properties such as the signal jitter and maximum rate of figure 4. The values show that even if the noise increases at low gain, the jitter remains constant to about 20 ps.

However, the maximum rate increases up to 300 MHz. The jitter remains constant because the noise increase is compensated by the larger slew rate.

The jitter of the three flavors of FAST for an input charge between 4 and 20 fC is shown in figure 5. This simulation has been obtained by probing the LVDS output of FAST in transient noise simulations, injecting each charge 400 times with a fixed threshold of 3 fC. Jitter is estimated as the standard deviation of the ToA. In these simulations, the input current has a trapezoidal shape with a duration of 1.2 ns, similar to the expected signal shape generated by a 55 µm thick UFSD. The figure shows the jitter of FAST for two typical values of capacitance: 6 pF and 3.4 pF. These values correspond to UFSD geometries of 1×3 mm^2 and 1.3×1.3 mm^2 with a thickness of 55 µm, which are those planned in future timing layers. In both cases, the EVO channels behave similarly. The EVO2 has always the lowest jitter as a consequence of the use of radio frequency transistors. Concerning the REG channels, they exhibit slightly higher values of jitter at low charges. As an example, an input signal with an MPV of 8 fC and 6 pF sensors, the EVO channels have a jitter of ~18 ps and REG channel of 24 ps. The jitter is much lower when a 3.4 pF sensor is used, about 12 ps for the three flavors of FAST. In all cases under discussion and for all flavors, the jitter saturates at 8–10 ps.

Figure 6 reports the expected jitter for a trapezoidal input of 8 fC, 1.2 ns long, for sensor capacitances from 4 to 20 pF. Considering the 30 ps time resolution target, figure 5 shows a promising behavior even with large C_{det}, up to 10 pF for EVO1 and EVO2, whereas for REG the upper limit of 30 ps is achieved with C_{det} up to 7 pF.

3.2 Timing performances of FAST with silicon sensors

System level simulations have been used to estimate the time resolution of the complete sensor-front-end system. These simulations aim to include all terms in equation (1.1) except for the TDC contribution. The uncertainties coming from the sensor have been simulated with Weightfield2 (WF2) [11] that allows introducing all the effects that degrade the timing properties like distortion in the electrical field or the non uniform charge deposition in silicon by a MIP ($\sigma_{\text{landau noise}}, \sigma_{\text{distortion}}$). WF2 is used to generate the current signals given as the input to the FAST transient noise simulations performed with a threshold fixed to 3 fC. For each signal, the ToA of the event, corrected by time-walk by means of the Time over threshold technique, is computed. The results are shown in figure 7.

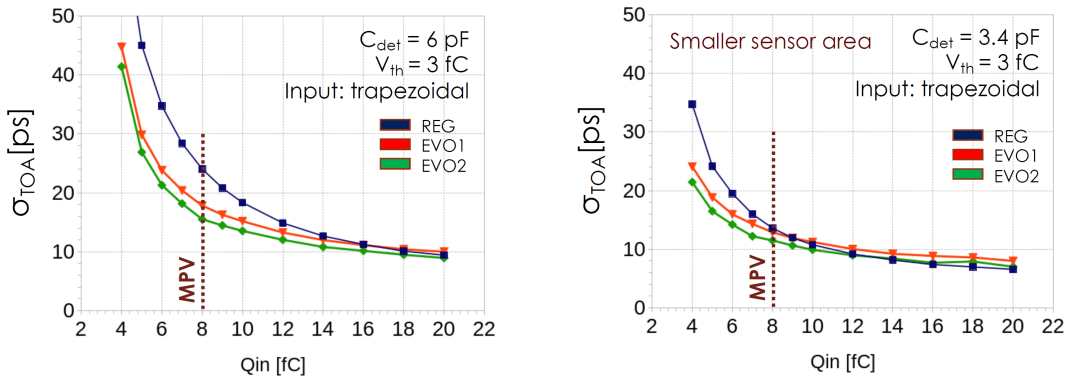


Figure 5. Jitter of the three FAST flavors for input charges between 4 and 20 fC. On the left values for a 6 pF sensor capacitance and on the right values for a 3.4 pF sensor capacitance.

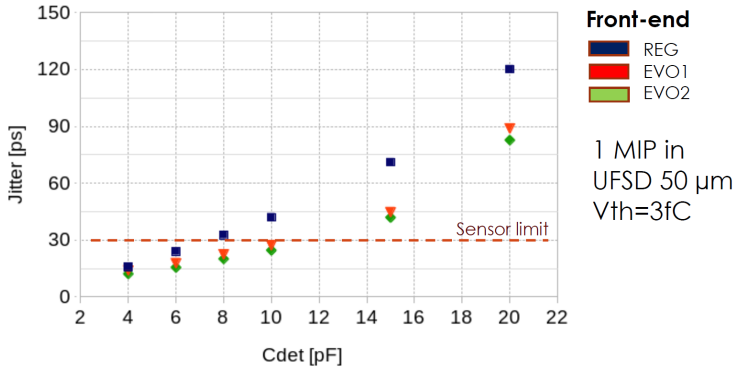


Figure 6. Jitter as a function of C_{det}, for the different FAST flavors, for a trapezoidal shaped injected signal of 8 fC.

In this study, the effect of the sensor thickness is explored: the sensor thickness affects the signal total integral, the signal slew rate and the input capacitance. Thin sensors positive aspects are a steeper signal and a reduced sensitivity to radiation damage effects while thicker sensors generate larger signals and have a lower sensor capacitance for a given area. System level simulations are important to find the best trade-off between the different parameters of the detector, and they were performed for the three FAST front-end amplifiers.

System level simulations using the signals generated by a MIP in UFSD sensors of different thicknesses (35 µm, 55 µm and 75 µm) and geometries ($1 \times 3\,\text{mm}^2$, $1.3 \times 1.3\,\text{mm}^2$ and $1 \times 1\,\text{mm}^2$) coupled with each of the three flavors of FAST have been performed. Each combination of thickness and geometry determines a value of C_{det}. The trend observed with a geometry of $1 \times 3\,\text{mm}^2$ is similar for the three flavors: as C_{det} increases, the time resolution degrades. This trend is expected in systems where the time resolution is driven by the jitter term, an indication that the resolution is dominated by the electronics. The opposite occurs with the geometry of $1 \times 1\,\text{mm}^2$: the time resolution improves as the C_{det} increases, indicating that the steeper signal of thinner detector brings

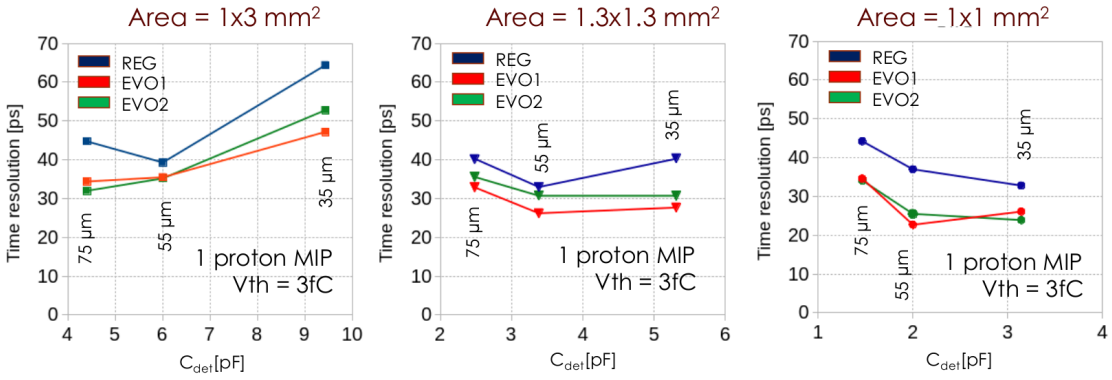


Figure 7. Time resolution simulated in a system comprising a UFSD and a FAST channel for different sensor geometries and thicknesses (35 µm, 55 µm and 75 µm). The input signal from the sensor has the expected charge from 1 MIP and it includes the Landau fluctuation in the ionization process. The threshold is kept fixed to 3 fC.

more benefit than the negative aspects due to an increase in capacitance. This indicates that the time resolution in this geometry is limited by the sensor. For the $1.3 \times 1.3\,\mathrm{mm}^2$ geometry, the two effects seen in the previous cases compensate and the time resolution is constant as C_{det} changes. The simulation shows that the best reachable time resolution is 23 ps, obtained with EVO2, a sensor 55 µm thick and a geometry of $1 \times 1\,\mathrm{mm}^2$.

4 Conclusions

We designed, simulated, and manufactured a new family of ASIC chips, for precise Time-of-Flight applications. The chips, called FAST, were produced in CMOS 110 nm technology. According to our simulations, when coupled to thin UFSD, FAST reaches a precision of about 30 ps. In order to explore different read-out architectures, the FAST chip family comprises of 3 different flavors (REG, EVO1 and EVO2), realized in 3 separate readout chips. All three FAST flavors are optimized for a 3–6 pF input capacitance and they require 1.2 mW/channel for the front end. Post-layout simulations, performed using typical signals from 6 pF UFSD, show that the jitter is approximately 18 ps and 24 ps for EVO and REG solution, respectively. The EVO front-ends combined with up to 10 pF LGADs exhibit a jitter below 30 ps. Simulations performed to study the effect of the sensor thickness in the final system showed that the contributions to the time resolution from sensor and electronics are balanced in sensors having a geometry of $1.3 \times 1.3\,\mathrm{mm}^2$. The time resolution, in this condition, is approximately 30 ps, independent of the sensor capacitance and thickness. In smaller geometries, for example $1 \times 1\,\mathrm{mm}^2$, even if the sensor contribution is dominant, the final time resolution can reach 23 ps with the EVO front-ends. Experimental tests are ongoing to compare measurements with these simulation results, which are competitive with other solutions designed using higher power consumption and smaller sensors. During the development of FAST, we extensively used a system level approach, where the simulation of the front-end chip is coupled to a full sensor simulation. System level simulations proved to be a powerful tool to identify the best combination of sensor geometries and read-out architectures.

Acknowledgments

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