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Developments and first measurements of Ultra-Fast Silicon Detectors produced at FBK

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ABSTRACT: Segmented silicon sensors with internal gain, the so called Ultra-FAST Silicon Detectors (UFSD), have been produced at FBK for the first time. UFSD are based on the concept of Low-Gain Avalanche Detectors (LGAD), which are silicon detectors with an internal, low multiplication mechanism (gain ~ 10). This production houses two main type of devices: one type where the gain layer is on the same side of the read-out electrodes, the other type where the gain layer is on the side opposite to the pixellated electrodes (reverse-LGAD). Several technological splits have been included in the first production run, with the aim to tune the implantation dose of the multiplication layer, which controls the gain value of the detector. An extended testing on the wafers has been performed and the results are in line with simulations: the fabricated detectors show good performances, with breakdown voltages above 1000 Volts, and gain values in the range of 5–60 depending on the technological split. The detectors timing resolution has been measured by means of a laboratory setup based on an IR picosecond laser. The sample with higher gain shows time resolution of 55 ps at high reverse bias voltage, indicating very promising performance for future particle tracking applications.

KEYWORDS: Particle tracking detectors (Solid-state detectors); Timing detectors; Detector modelling and simulations II (electric fields, charge transport, multiplication and induction, pulse formation, electron emission, etc)

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1 Introduction

Ultra-Fast Silicon Detector (UFSD) is a new concept of silicon detector based on Low-Gain Avalanche Detectors (LGAD) design, and optimized to provide both good spatial resolution and high timing performance [1]. First applications of UFSD are envisioned in LHC upgrades, where excellent time resolution coupled with good spatial resolution helps to reduce drastically pile-up effects and improve the tracking reconstruction process [2]. Standard silicon detectors can be still used in timing applications, provided the sensor geometry is appropriate [3]. However, their performance are limited at ≈ 100 ps given their small signals and the saturation of the drift velocity of charge carriers ($v_{\text{sat}} \approx 10^7$ cm/s). To overcome these intrinsic limits of silicon detectors, the UFSD design has been developed with the aim to produce larger and fast signals suited for timing applications. These devices exploit the effect of charge multiplication in a similar way to Avalanche PhotoDiodes (APDs) but with a lower gain in the range from 10 to 30. Such a technology merges the best characteristics of standard p-in-n silicon sensors in terms of segmentation, low leakage current, low noise, with the main feature of APDs, producing signals that are a factor of 10 higher than those of standard sensors, however without the problems connected with APD high gain.

The first LGAD sensors have been produced in recent years by CNM Barcelona [4] and characterised by several groups, showing very promising performance in terms of timing [5, 6]. These detectors are based on a n^+ -in-p structure and feature an extra p^+ implant extending several microns underneath the n^+ -implant. The p^+ region creates a strong electric field that provides multiplication.

In this work, we present the technology and the characterisation results of the first UFSDs produced at FBK Trento. We propose a revised junction structure based on a p-type deep implant in order to create an effective and reliable multiplication layer. In addition, alternative designs and fabrication approaches are tested to pass from single pad structure to strips and pixel detectors. In

fact, standard UFSDs feature a blank ohmic contact on the back side while the read-out junction is placed on the front side. When the front junction is patterned, this structure could lead to large spatial non-uniformities due to the lower multiplication of the charge collected at the junction edges. In order to cope with these segmentation issues, we tested a double-sided UFSD structure having a large and uniform multiplication region on the one side and ohmic segmented pixels on the other side. This structure has been proposed in ref. [7] where TCAD simulation are also reported. This design allows having a very uniform electric field, while keeping the possibility of fine electrode segmentation.

2 Technology and detector design

2.1 Fabrication technology

The first UFSD detectors have been fabricated at the FBK clean room facility by using a CMOS-like fabrication process. A fully double-sided photolithography technology has been used to define the junction structure, contacts and the metal grid, while ion implantation has been used to fabricate all the doped layers. The detectors have been manufactured on high resistivity ($> 5000 \text{ Ohm}\cdot\text{cm}$) p-type Float-zone (FZ) 6" silicon wafers. The thickness of the wafer used in this first production batch is $275 \mu\text{m}$.

The amplification mechanism in LGAD is normally provided by avalanche multiplication due to a presence in the detector structure of a "multiplication" region where the electric field reaches values higher than 200 kV/cm . Under such a high electric field the charge carriers acquire enough energy to create additional electron-hole pairs by means of the "impact ionization" effect. The multiplication region may be obtained by adding a moderately p-type doped region close to the junction. By the technological point of view, different fabrication approaches can be used to create an effective multiplication layer. The standard one, already used in the production of the first LGAD samples [4], consists in diffusing a p-type layer several microns thick underneath the n^{++} electrode. In this case, the n^{++} and the p regions overlap and partially compensate. A possible drawback of this scheme is that any variation in diffusion of the dopants due to thermal steps during the fabrication process could lead to a modification of the net doping and thus of the gain value [6].

In the present production at FBK, a slightly different approach in designing the junction profile has been developed and tested, exploiting the strong experience with Silicon Photo-Multipliers (SiPM) [8]. The schematic cross section of the proposed device is shown in figure 1a. The gain layer on the front side is made of a shallow n^{++} region and a deep p^+ region, obtained by means of high-energy Boron implantation. A scheme of the doping profiles across the junction is sketched in figure 1b. It is worth nothing that in this scheme the n^{++} and the p^+ profiles do not overlap, thus preventing any doping compensation and providing a reliable structure almost insensitive to variations in thermal diffusion of the dopant elements during the fabrication process. In addition, this scheme provides a uniform electric field without any peaked or steep regions, leading to lower detector noise. In fact, hot spots or regions with a too high electric field could lead to increased noise via tunneling effect or field-enhanced generation mechanisms. A previous analysis and design optimisation of the UFSD main parameters was performed in [7] by means of Sentaurus TCAD simulation toolkit and by using models calibrated on the FBK technology. Simulations show that

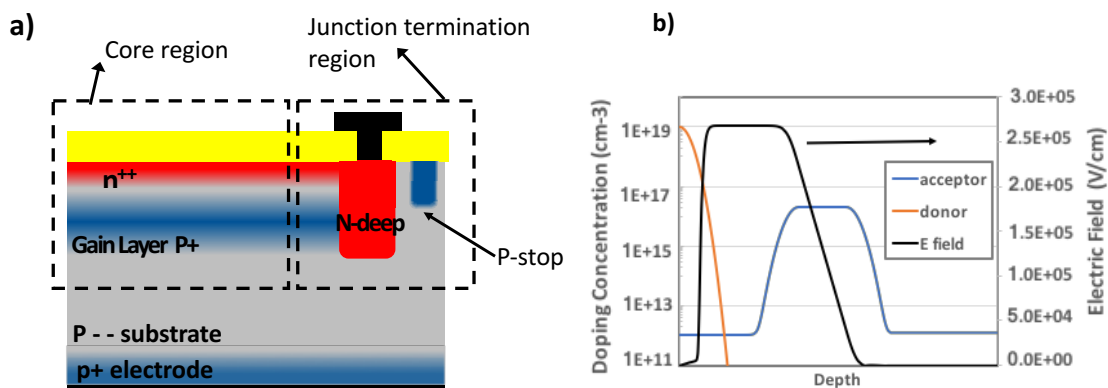


Figure 1. (a) Schematic cross section of the proposed junction structure (not to scale). b) Schematic representation of the doping profiles of the multiplication junction. The shallow n⁺⁺ profile is represented by the red line, the deep p⁺ by the blue one, while the black line represents the expected electric field.

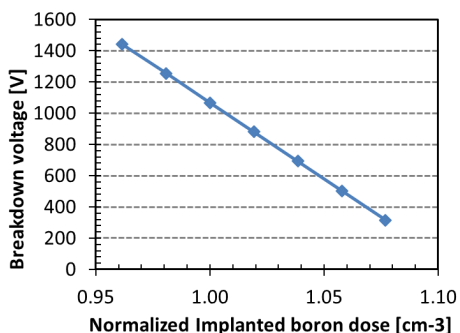


Figure 2. Simulated breakdown voltage as a function of the normalized implanted dose of the gain layer.

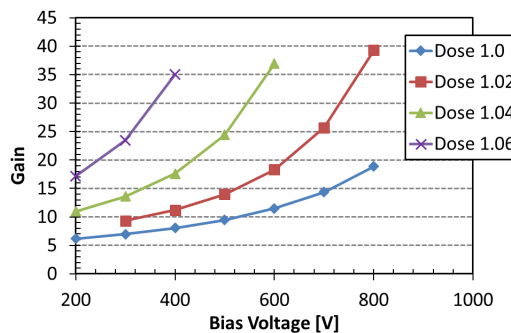


Figure 3. Simulated gain as a function of reverse bias voltage for samples with different boron dose of the gain layer.

the adjustment of the impurity profile of the p⁺ region is very critical, due to its effect on the gain and on the voltage capability of the detector. The implanted boron dose should be high enough to ensure a gain in the range of 10–30 but not too high to affect the voltage capability of the core region. Figure 2 shows the simulated breakdown voltage as a function of the boron dose of the gain layer, while figure 3 reports the gain as a function of the bias voltage for four boron doses, as obtained by simulating the collected charge in case the sensor is hit by a minimum ionizing particle (MIP). These results show that both the Gain and the Breakdown Voltage are very sensitive to the doping level of the gain layer. On the other hand, a correct tuning of the dose value allows to obtain a detector with correct gain and quite high breakdown voltage.

In the first production run we have manufactured 12 wafers, with 5 different doses of the gain layer implant, to investigate the performances of sensors with various levels of signal amplifications. In each gain split (GS) the implanted boron dose has been increased of the 2 %, as indicated in table 1:

Table 1. List of technological splits (GS) of the produced batch. In each split, the implanted boron dose has been increased by 2 %.

Gain Split	Normalised Boron implanted Dose
GS 1	1.00
GS 2	1.02
GS 3	1.04
GS 4	1.06
GS 5	1.08

2.2 Design of the detector peripheral region

The multiplication junction requires an optimised edge termination strategy in order to prevent premature breakdown also in case of highly irradiated detectors. In addition, the modification of the electric field distribution at the junction edges might compromise the uniformity of the multiplication, affecting the gain uniformity throughout the whole detector area.

A proper termination structure has been made of a deep n^+ region equipped with a metal filed plate, the so called Junction Termination Extention (JTE), as shown in figure 1a. This termination has actually been implemented also in multi-pad sensors around each pad, even those that are not at the physical edge of the sensor. The reason of implementing such protection ring around each pad is to ensure that the electron-hole pairs generated by particles hitting in between pads are not reaching after some drift the multiplication layer, generating a large, out-of-time signal, but that are absorbed on the pad periphery by the JTE implant.

In addition, a multiple guard-ring termination structure on the gain side has been adopted in order to prevent early breakdown at the periphery. The structure consists of a set of 12 floating n^+ regions equipped with metal field plates. The n^+ rings are isolated by patterned p^+ regions (p-stop). The first ring, close to the detector core region, is biased to collect separately the charge carriers generated outside the detector and thus decreasing the leakage current. Numerical simulations show that this multi guard-ring structure prevents lateral breakdown up to 1100 Volts also after high irradiation (a fixed charge density of 10^{12} cm^{-2} at the SiO_2/Si interfaces has been considered in simulations as a consequence of the radiation damage).

2.3 Tested detector layouts

The first UFSD run includes several segmented structures: strip detectors with different strip pitches, pixel detectors for different front-end chips and also single diodes structures with dimensions ranging from 0.5 mm to 5 mm. All the segmented structures have been produced in three different versions: i) front junction segmentation, ii) back side ohmic contact segmentation and iii) AC coupled.

The three different designs are represented in figure 4. The first one features a blank ohmic contact on the back side and a segmented read-out junction on the front side. In this approach both the n^{++} and the p^+ multiplication layers are patterned. A drawback of this structure is the low uniformity of the electric field at the junction edges which could lead to spatial non-uniformities of the signal multiplication. The second fabricated design (also named “reverse-LGAD”) is based on a double-sided structure having a large and uniform ($n^{++}/p^+/p^-$) multiplication junction on one

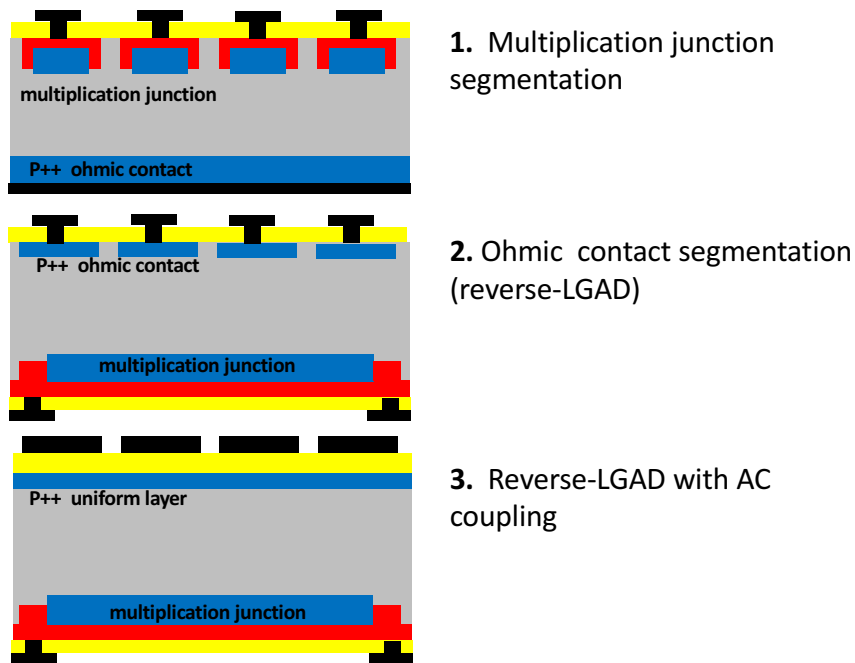


Figure 4. Schematic cross sections of the three implemented segmentation strategies. The first one features a segmented multiplication junction. The second scheme (reverse-LGAD) has a pixelated p^{++} ohmic contact connected to the read-out. The third design is based on the reverse-LGAD scheme where the read-out is AC coupled to a p^{++} uniform layer.

side and a segmented ohmic contact on the opposite side. This structure has been proposed and analysed in ref. [7], where TCAD simulation are also reported. It is worth noting that in this case a very uniform electric field is provided in the whole detector area, while keeping the possibility of fine pixel segmentation. The third fabricated design is based on the reverse-LGAD structure as well, but in this case the ohmic contact is also uniform and the spatial information is provided by a segmented metal layer, AC coupled with the uniform p^{++} layer. The resistivity of the ohmic p^{++} layer has been tailored so that the signal is AC induced to the read-out pads. The delicate aspect of this design is the capability of matching the p^{++} resistivity with the value of the coupling capacitance so that the signal will correctly be transferred to the electronics.

3 Experimental characterisation

3.1 Electrical characterisation under static conditions

The preliminary electrical characterisation of the sensors has been carried out at the Istituto Nazionale di Fisica Nucleare (INFN) and at the University of Turin. A characterisation under static conditions has been performed by acquiring I-V curves of the detectors under reverse bias conditions. The measurements were performed individually on the samples after dicing, in a controlled temperature environment. A reference detector, with identical layout but without gain layer has been characterised, as well.

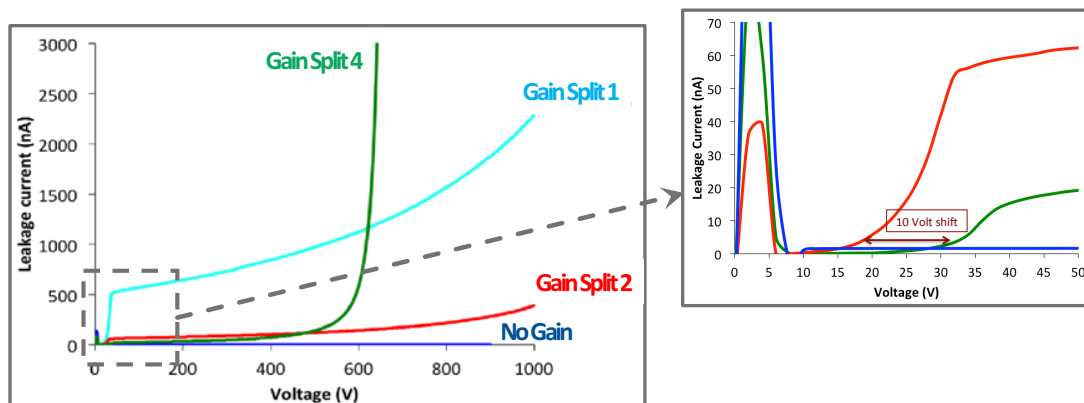


Figure 5. Leakage current as a function of reverse voltage for three samples referring to three different Gain Splits and for the reference diode without gain layer. A close-up of the IV curves at low voltages is reported in the inset.

Figure 5 reports the reverse I-V curves for detectors belonging to three different Gain Split (cyan line for *GS 1*, red line for *GS 2* and green line for *GS 4*) while the blue line represents the reference diode without gain. The two lower gain splits show break-down voltages above 1000 Volts, while the samples with higher dose, generating more gain, show a lower breakdown voltage (600 Volts in the case of *GS 4*). In the inset of figure 5 a close-up of the leakage current at low bias voltages is reported. At very low voltages (< 10 Volts) the leakage current is very high due to a non-complete depletion of the guard-ring structure, which allows charge injection from the border region of the detector. Whereas, the foot at 15–30 Volts indicates the depletion of the gain layer, and as expected, the voltage where the foot occurs increases as the doping level of the gain layer increases. It is worth noting that at higher voltages, the leakage current level is not directly correlated to the gain value of the detectors, due to the large variability in the leakage current experienced by different samples.

3.2 Gain and timing resolution

In order to estimate the gain value of the produced UFSD a measurement setup based on a 1064 nm picosecond laser and a broad-band amplifier has been used. The laser intensity has been tuned to reproduce the energy deposition of a MIP in the detector. Both the sensor and the amplifier are placed in a climatic chamber that allows a precise regulation of temperature and humidity. The gain is calculated as the ratio between the area of the signal produced by the UFSD sample and that of the reference p-in-n diode (without gain layer). Figure 6 reports the gain value for the three different gain splits as a function of the bias voltage. It can be seen that gain values in the order of 10 can be obtained at high voltages with the sample from *GS 2*. On the other hand, the *GS 1* sample features a maximum gain of about 5 at 900 Volts, while the *GS 4* sample shows an exponential growth of the gain, that is greater than 10 since very low voltages.

In order to get an estimation of the sensor timing capability, the time resolution has been assessed by means of the same laboratory setup used for the gain measurements. The time of a constant fraction of the signal peak is measured and the time resolution is defined as the standard deviation of the time distribution. Figure 7 reports the time resolution measured on the different gain splits as a function of the bias voltage. The timing resolution is a strong function of the gain

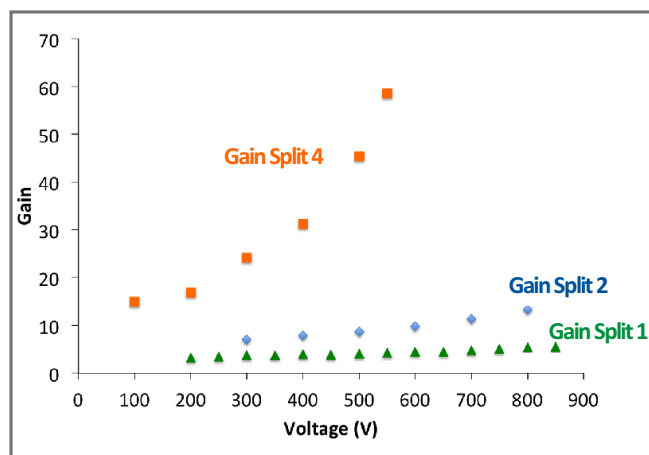


Figure 6. Experimental Gain measured with a 1064 nm IR picosecond laser as a function of the reverse bias voltage. The data of three samples relative to three different Gain Splits are reported.

value. For this reason, the resolution improves as the bias voltage or the doping level of the gain layer increase. In particular, the time resolution of the sensor *GS 4* reaches the notable value of 55 ps at about 500 Volts. In addition, the time resolutions remains better than 100 ps also for the detector from the *GS 2*, which features a moderate gain of about 10 at the maximum bias voltage.

These results are very promising by considering that a relative thick substrate has been used in this first production. As discussed in [1], as a general rule the timing performance of UFSD is proportional to the ratio of the gain value over the sensor thickness (G/d), therefore thin detectors with high gain provide the best time resolution. Since processing of 6" wafers thinner than 200 μm is not compatible with the automatic equipment of the clean room facility, we plan to use Si-on-Si wafers, where a 60 μm thick high resistivity FZ wafer is bonded to a low resistivity Czochralski (CZ) support wafer. The detector is fabricated on the thin FZ wafer while the support wafer is electrically inactive. Such a structure allows to produce UFSD with optimal thin substrates fulfilling at the same time the requirements of the laboratory equipment.

4 Conclusions

UFSD detectors have been fabricated for the first time at FBK Trento. We presented and discussed the fabrication technology and the design of the detectors, with particular attention to the design of the multiplication junction and of the detector peripheral region. In order to obtain a segmented detector, we have tested two main type of device layouts: one type where the read-out electrodes are connected to a segmented gain layer, the other type where a uniform gain layer is on one side and a ohmic pixellated contact on the opposite side (reverse-LGAD). Several technological splits have been included in the first production run to tune the implantation dose of the multiplication layer, which controls the gain value of the detector. The fabricated detectors have shown excellent breakdown performance and gain values in the range of 5–60, depending on the boron dose used to produce the multiplication junction. The detector timing resolution has been measured and a value of 55 ps has been extracted for the sample with higher gain.

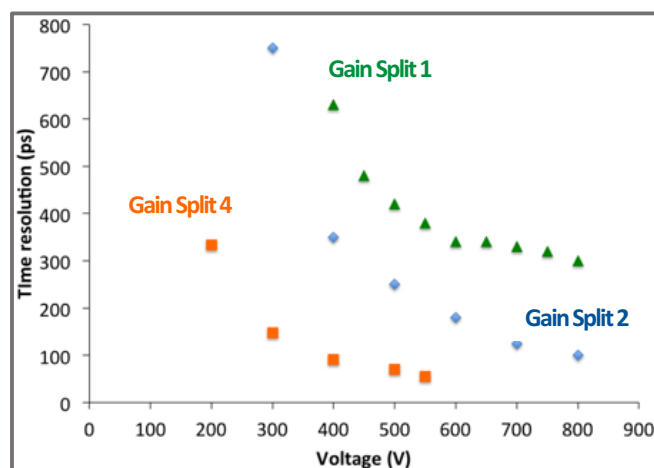


Figure 7. Timing resolution as a function of the reverse bias voltage, measured at 24 °C. The data of three detectors relative to three different Gain Splits are reported.

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