TIMING CAPABILITIES OF ULTRA-FAST SILICON DETECTORS*

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The development of Low-Gain Avalanche Diodes (LGADs) has made possible to manufacture silicon detectors with output signals that are about a factor of 10 larger than those of traditional sensors. This increased output brings many benefits such as the possibility of developing thin detectors with large enough signals, a good immunity towards low charge collection efficiency and it is key for excellent timing capabilities. In this paper, we report on the development of silicon sensors based on the LGAD design optimized to achieve excellent timing performance, the so-called Ultra-Fast Silicon Detectors (UFSDs). In particular, we demonstrate the possibility of obtaining ultra-fast silicon detectors with time resolution of less than 30 picosecond.

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1. Introduction

The possibility to use and control charge multiplication in un-irradiated silicon detectors has been the subject of intense study within the RD50 Collaboration [1]. Low-Gain Avalanche Diodes, as developed by CNM [2, 3], are $n-on-p$ silicon sensors with a high ohmic p bulk which have a p^+ implant extending several microns underneath the n-implant. Figure 1 shows the $n^{++}-p^+-p-p^{++}$ structure of an LGAD.

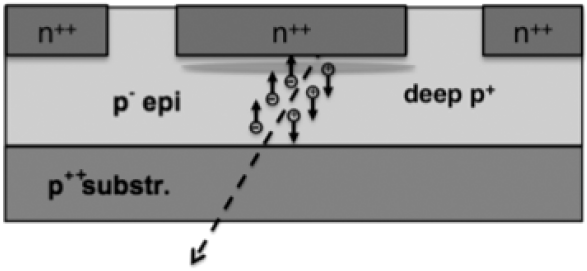

Fig. 1. Schematic of a Low-Gain Avalanche Diode. The extra deep p^+ layer creates a strong electric field that generates charge multiplication.

This implant generates a large local field at a depth of about 1–5 μm. The doping concentration of the p^+ implant is chosen to generate a gain of 10–20, in contrast to a gain of 10^4 or more in silicon photomultipliers (SiPM) and multi-pixel photon counters (MPPC). LGADs work by inducing multiplication for electrons, while holes multiplication, given the field and depth values involved, is insignificant. Therefore, LGADs do not have a positive feedback loop formed by the concurrent electrons and holes multiplication processes, present in SiPM, which causes dead time after the avalanche.

1.1. Ultra-Fast Silicon Detectors

The design of Ultra-Fast Silicon Detectors [4–6] exploits the effect of charge multiplication in LGADs to obtain a silicon detector that can concurrently measure with high accuracy time and space.

2. Time-tagging detectors

Figure 2 shows the main components of a time-tagging detector. For a review of current trends in electronics, see for example [7], a summary of the time performance of UFSDs can be found in [8]. The silicon sensor, shown in the picture as a current source with a capacitance C_d in parallel, is read out by a pre-amplifier that shapes the signal. The shaper's output is then compared to a fixed threshold to determine the time of arrival. In

the following we will use this simplified model to explore the UFSDs timing capabilities, while we will not consider more complex and space-consuming approaches such as waveform sampling.

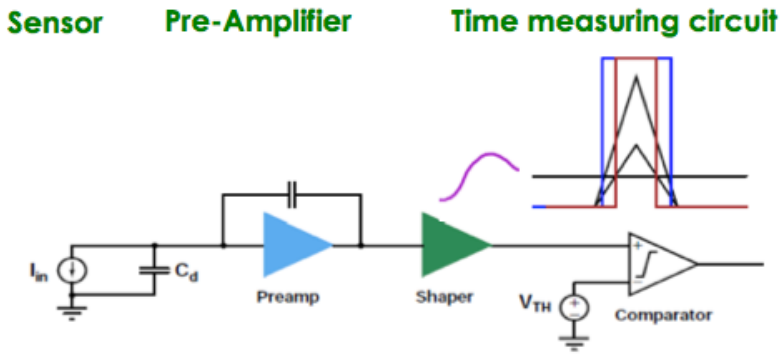

Fig. 2. Main components of a time-tagging detector. The time is measured when the signal crosses the threshold.

The time resolution σ_{t} can be expressed as the sum of three terms: *(i)* Time Walk , *(ii)* Jitter, and *(iii)* TDC binning

$$\sigma_{\mathrm{t}}^2 = \sigma_{\mathrm{TW}}^2 + \sigma_{\mathrm{J}}^2 + \sigma_{\mathrm{TDC}}^2 \,. \tag{1}$$

TDC binning introduces a fix uncertainty equal to $\sigma_{\mathrm{TDC}} = \mathrm{TDC_{bin}}/\sqrt{12}$. As the performance of TDCs becomes faster and faster [7], we assume $\mathrm{TDC_{bin}} = 20$ ps and thus this effect will not be important.

Using the explicit expressions of σ_{TW}, σ_{J} and σ_{TDC}, equation (1) can be rewritten as

$$\sigma_{\mathrm{t}}^2 = \left(\left[\frac{V_{\mathrm{th}}}{S/t_{\mathrm{r}}} \right]_{\mathrm{RMS}} \right)^2 + \left(\frac{N}{S/t_{\mathrm{r}}} \right)^2 + \left(\frac{\mathrm{TDC_{bin}}}{\sqrt{12}} \right)^2 . \tag{2}$$

This parametrization requires the following quantities:

- $\boldsymbol{d}$: Detector thickness [micron].
- $\boldsymbol{l}$: Pixel pitch (assuming square pixels) [micron].
- $\boldsymbol{C_{\mathrm{Det}}}$: Detector capacitance: $C_{\mathrm{Det}} = \epsilon\epsilon_o \frac{l*l}{d} + 0.2 * 4l + 50$ fF.
  The first term accounts for the capacitance to the back-plane, the second for the contribution from the neighbours, and the third one for constant stray contributions.
- $\boldsymbol{N}$: Noise: $N \propto \frac{C_{\mathrm{Det}}}{\sqrt{t_{\mathrm{r}}}}$.
  We assume that it is dominated by the voltage term.

$\boldsymbol{S}$: Signal amplitude.

$\boldsymbol{t_r}$: Preamplifier rise time, set equal to the charge collection time.

$\boldsymbol{V_{th}}$: Comparator threshold. Set to 10 times the noise level: $V_{\rm th} = 10 \times N$.

$\mathbf{TDC_{bin}}$: TDC bin width. We consider a value of 20 ps.

2.1. State of the art

With the assumptions outlined above, the state of the art of timing capability in silicon sensors is shown in Fig. 3. The picture shows $\sigma_{\rm t}$, and its two parts $\sigma_{\rm TW}$ and $\sigma_{\rm J}$, for a $l = 300$ pixel sensor as a function of detector thickness. The contribution from time walk has been reduced by a factor of three to mimic the effect of the use of a Time over Threshold (ToT) or a Constant Fraction Discriminator (CFD). The secondary x-axis at the top shows the amplifier shaping time used in the simulation.

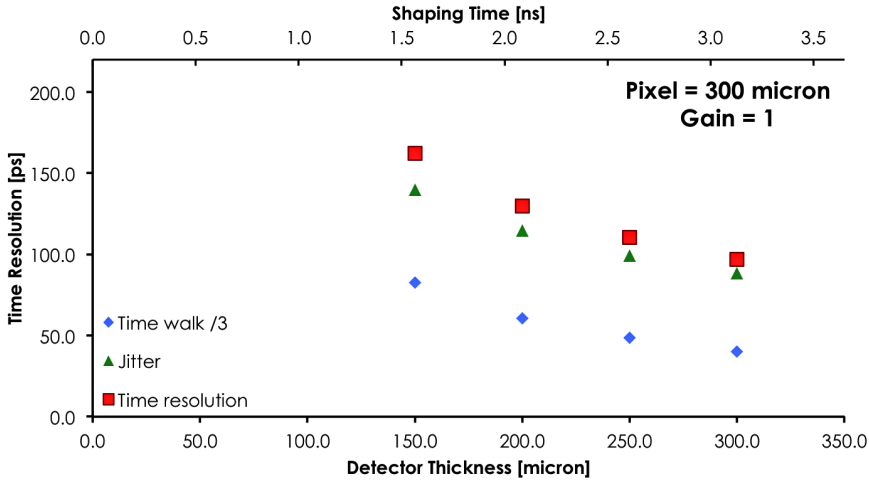

Fig. 3. The time resolution $\sigma_{\rm t}$, and its two parts $\sigma_{\rm TW}$ and $\sigma_{\rm J}$, for a 300 μm pixel sensor as a function of detector thickness.

Our parametrization shows that the best time resolution is obtained for small pixels on thick sensors, while larger pixels on thin sensors have worse time resolution due to their higher capacitance. We find $\sigma_{\rm t} \sim 100$ ps for a $l = 300$ μm pixel sensor of 250–300 μm thickness. This result is consistent with the time resolution obtained by the NA62 GigaTracker electronics.

3. Weightfield2: a simulation program for silicon detectors

To evaluate the performance of UFSDs, we have developed a simulation program called Weightfield2 [9]. The program is completely configurable using a graphic user interface, as shown in Fig. 4.

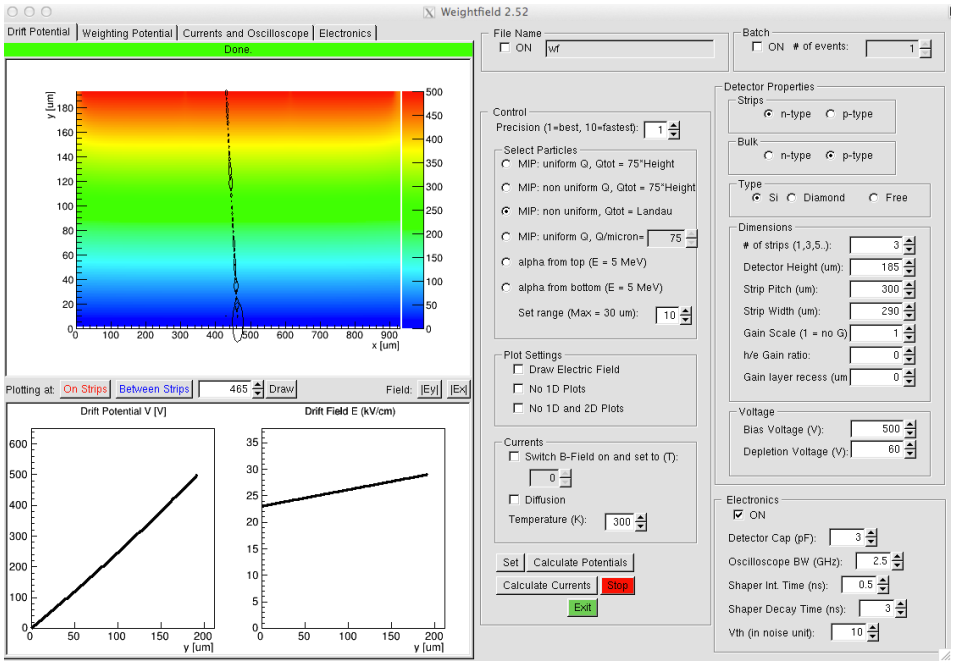

Fig. 4. Weightfield2 graphic user interface.

The interface is divided into several sub-panels that allow selecting among many possibilities:

- Incident particle (ideal MIP, MIP, alpha from top and bottom);
- Presence of an external B-field, ambient temperature and the effect of thermal diffusion;
- Type of silicon detector (strips and bulk);
- Sensor geometry;
- Operating conditions;
- Oscilloscope and front-end electronics.

To facilitate the comparison of the program output to measured signals, the program simulates the response of an oscilloscope with a configurable bandwidth, and that of a shaper, also with configurable parameters. Likewise, the program can simulate silicon sensors with internal gain such as

LGADs, and it separates the generated current into the component due to the initial electrons and holes and that due to the electrons and holes from the multiplication mechanism.

3.1. Comparison with laboratory measurements

We have performed several laboratory tests to validate the output of the simulation program. In particular, using laser signals of different wavelengths to reproduce the energy depositions of MIPs (1064 nm) or that of alpha particles (400 nm), we have compared the output of the simulation to the measured signals as a function of the applied bias voltage and internal gain.

Figure 5 shows the comparison between data and simulation for 3 types of signals (MIP, alpha from the top, alpha from the bottom) as a function of the applied bias voltage. In each plot the solid/black line shows the measurement while the dashed/red line the simulated output obtained using Weightfield2. As the various plots show, the program is able to correctly reproduce all measurements.

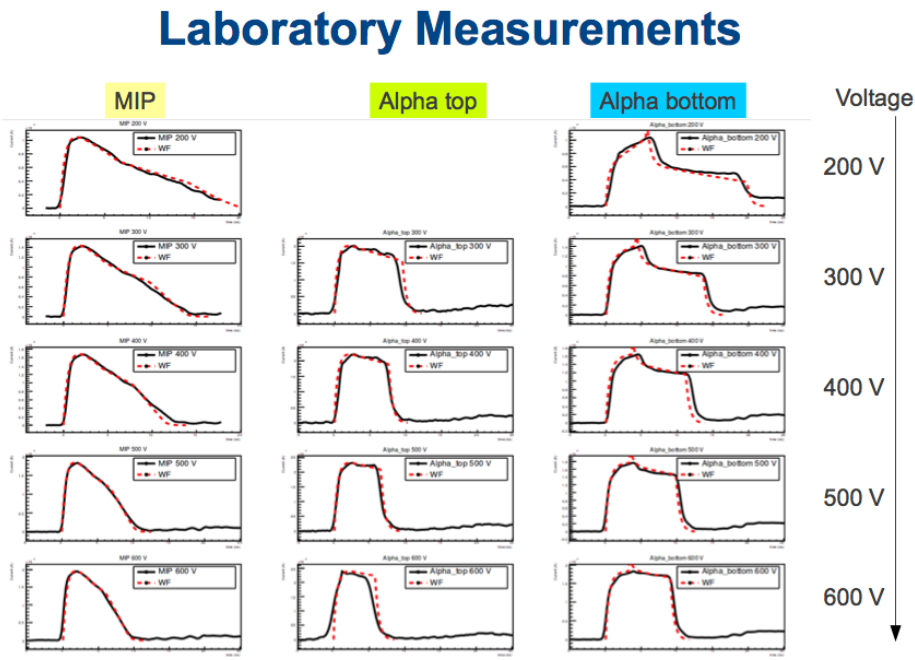

Fig. 5. Data-simulation comparison for signals generated by MIP and alpha particles at different bias settings. In each plot, the solid/black line shows the measurement, while the dashed/red line the simulated output obtained using Weightfield2.

4. Timing capabilities of UFSDs

Using the parametrization described in equation (2), that is able to correctly reproduce the timing capabilities of state of the art silicon detectors, and the simulation program Weightfield2, which has been validated using laboratory data, as shown in Fig. 5, we are in a position to predict the timing capabilities of UFSDs.

Figure 6 shows the predictions of the time walk and jitter values for UFSDs with different pixel sizes and substrate thicknesses. The values shown are those obtained by the simulation applying a single threshold for the jitter and no time walk compensating circuits.

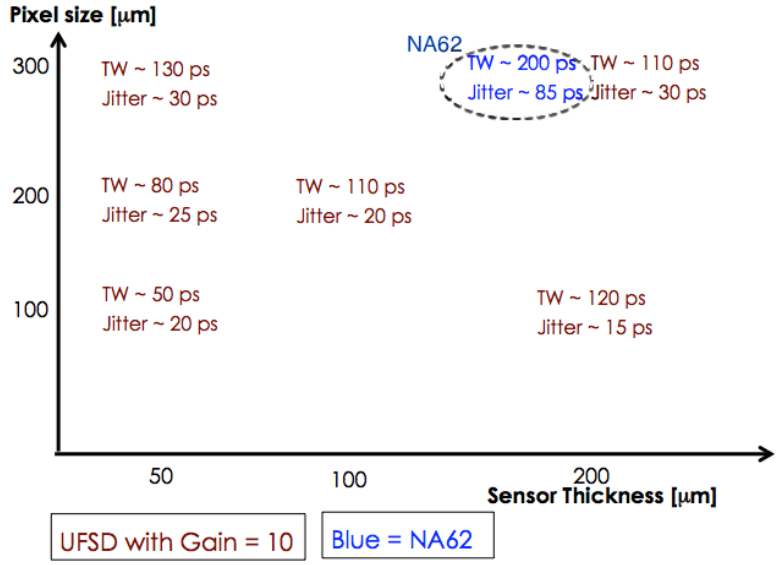

Fig. 6. Simulation predictions of the time walk and jitter values for UFSDs of gain 10, with different pixel sizes and substrate thicknesses. The time walk contribution can be lowered by using a compensating circuit such as a CFD or a ToT, while the jitter contribution can be decreased using multiple points to determine the time at which the signal reaches the threshold value.

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The plot also shows that UFSDs improve on the current values obtained by NA62, for a pixel size of 300 micron and a substrate thickness of 200 micron, by a factor of about 3 in jitter and a factor of about 2 in time walk.

5. Conclusion

The development of silicon detector with internal gain, LGADws, has opened up the possibility to use silicon detectors for precision timing. Using the performance of state-of-the-art detectors, we have developed a parametrization of the time resolution in silicon detectors. Concurrently, we have developed the simulation code Weightfield2, validated with laboratory measurements, to predict the signal shape and timing capabilities of LGAD-based silicon detectors optimized for timing performance, the so-called Ultra-Fast Silicon Detectors (UFSDs). Combining these two tools, we have predicted the timing capabilities of UFSDs, and we found that they can achieve a precision of 30 ps using existing electronics. The development of custom ASIC chips using the 65 nm technology will considerably lower this value.

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