FAST: a front end readout ASIC for high flux and time resolution applications with UFSD

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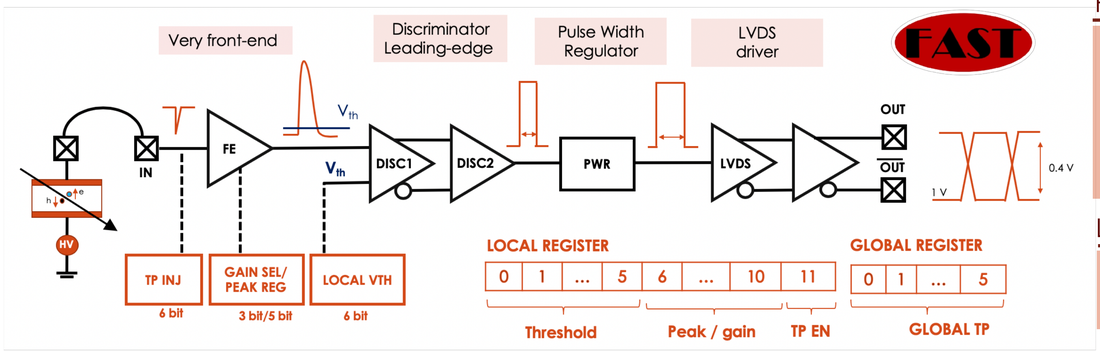
J.Olave [a,*] **F. Fausti** [a,*]; Nicolo Cartiglia [a]. a) Istituto Nazionale di Fisica Nucleare, sez. di Torino, Italy; *) ASIC designer

Abstract

The possibility of measuring the time of passage of charged particles with a pico-seconds accuracy while maintaining very good spatial resolution (~100 micron) is a very important development in the field of charged particle tracking. The Ultra-Fast Silicon Detector(UFSD) group of INFN-Turin is involved in this challenge, developing both fast Silicon sensors and the dedicated read-out electronics. In this context a new **readout front-end electronics with 3 different flavors**, has been designed using the 110 nm CMOS technology. The figure of merit of this chip, called FAST, is the capability to keep **the jitter below 20 ps and to deal with rates up to 300 MHz.** In this poster the description of the ASIC is provided with some simulation results and very preliminary tests. FAST has been submitted to the foundry in May 2019 and an extensive characterization campaign is ongoing.

The Front-End Electronics



Pulse width regulator

- Pulse duration(MPV): **2-4 ns**
- This block can increase the discriminator output length to make it compatible with **commercial TDCs**

LVDS driver

- It allows compatibility with **commercial TDCs and FPGAs**

The very front end

- **Three** architectures: REGULAR, EVO1 and EVO2
- Power limited to **1.5 mW/CH**
- Designed for **1 proton MIP in 50 µm** thick UFSD sensor
- Sensor cap: **1 pF – 6 pF**

Ancillary circuitry

- **Test Pulse injection system:** a global 6 bit register is used to inject charge among 0.3 -18 fC
- **Selectable gain (EVO) or peaking time (REGULAR):** 3 bits/5bits used to select 8 different gains in EVO or for the peaking time tuning in REG. The last regulation is meant to minimize noise
- **Local threshold regulation:** the threshold can be locally regulated up to 30 mV with 6 bits DAC
- **Pulse width regulation:** it allows to add a fixed Δt to the pulse duration.

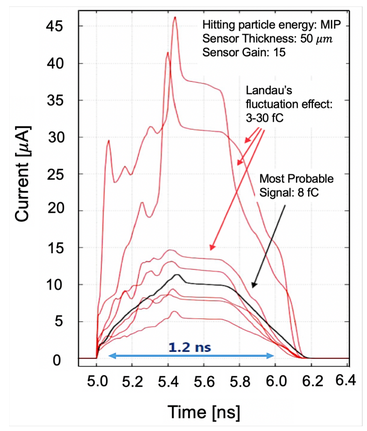
Discriminator

- Two stage leading-edge differential discriminator
- Power < **0.6 mW/CH**
- **time walk** → offline corrected

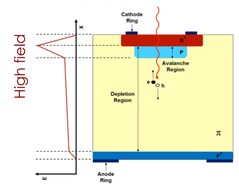
Signal shaping in UFSD (I)

- The signal amplitude in silicon sensors follows the **Landau distribution**
- Non-uniform ionization along the track generates distortion in the collected charge. This effect is responsible of the sensor contribution in the time resolution
- **These effects can be modelled** with good accuracy and the use of these models allows to simulate every custom readout electronics with much more accuracy

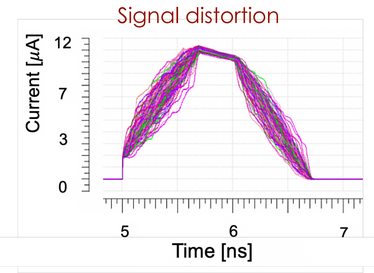
Landau's statistical fluctuations



UFSD sensor



Signal distortion



Design approach

$$\sigma_t^2 = \overbrace{\sigma_{LANDAU\ NOISE}^2 + \sigma_{DISTORTION}^2}^{\text{sensor}} + \overbrace{\sigma_{JITTER}^2 + \sigma_{TDC}^2 + \sigma_{TIME\ WALK}^2}^{\text{readout electronics}}$$

- The front-end amplifiers of FAST have been optimized and simulated by using a **system level** approach which aims to take into account each term in the time resolution formula
- **Sensor contribution**: this information is included by means of Weightfield2. It allows to introduce in the simulations effects of Landau distribution, distortion and effects of radiation in silicon.
- **Electronics simulations**: this contribution is evaluated by using transient noise simulations in EDA tools. Parasitics (R-C-CC) in the ASIC are extracted by using two different tools and they are included in the simulations. In these simulations time walk is corrected with the ToT technique.

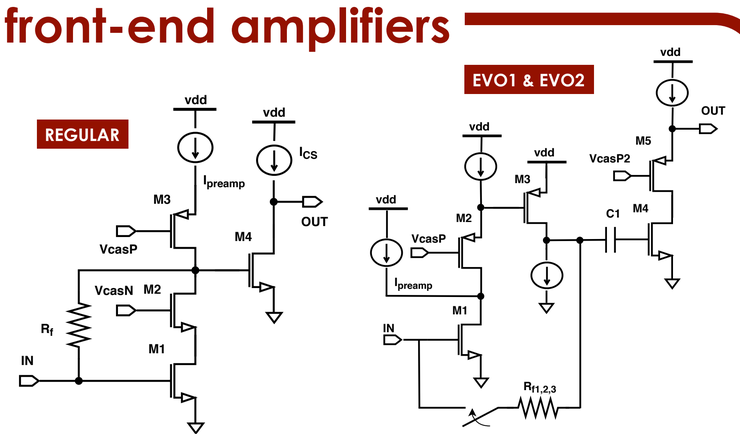
Very front-end amplifiers

REGULAR CHANNEL

- **Limited bandwidth to 100 MHz**
- Gain: ~ 60 mV/fC
- **Noise: ~310 e⁻**
- Power consumption: ~1.2mW/CH
- SNR (MIP): ~ 160
- Max hit rate: 50 MHz

EVO CHANNEL

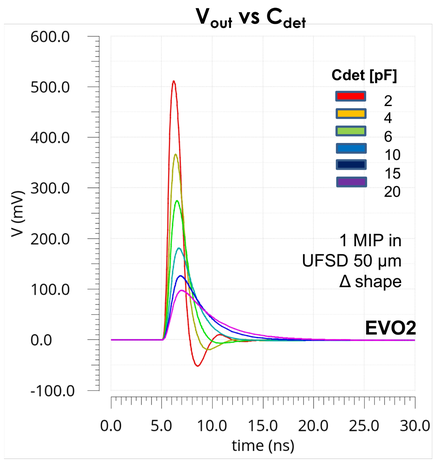
- **Larger bandwidth: ~ 400 MHz**
- Gain: ~ 31 mV/fC (8 regulations)
- **Noise: ~640 e⁻**
- Power consumption: ~1.2mW/CH
- SNR(MIP): ~75
- Max hit rate: 300 MHz
- AC coupling to reduce mismatch
- 2 topologies: standard CMOS & RF



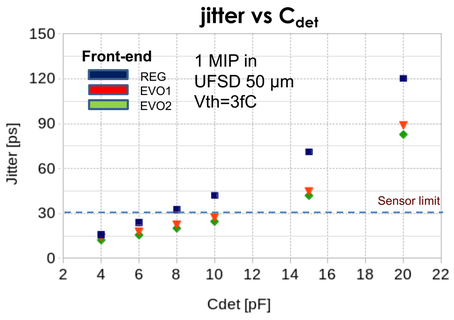
Simulation results

Effects of C_{det}

V_{out} vs C_{det}



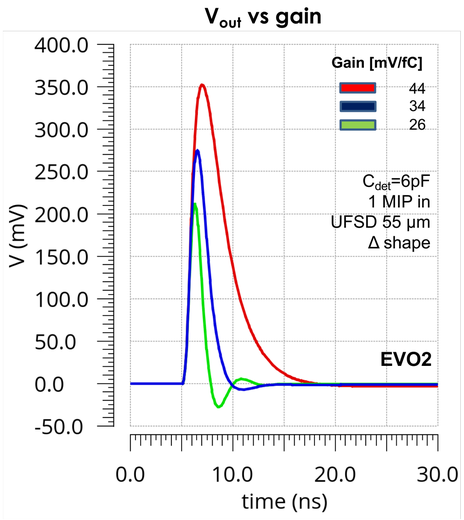
jitter vs C_{det}



- Analog output (amplitudes and duration) changes with the C_{det}
- Amplifiers are designed to reach 30 ps with 6 pF UFSD sensor
- Sensor cap ↓ → Time resolution ↑ Max rate ↑

Effects of gain

V_{out} vs gain

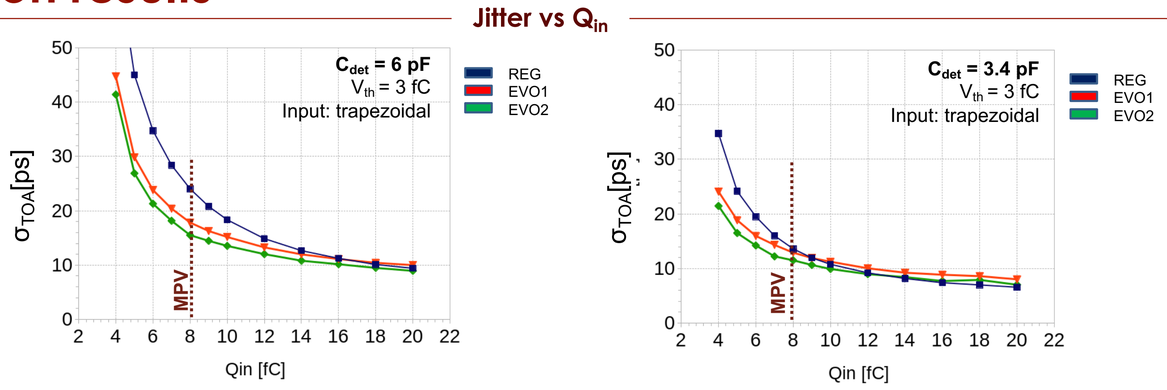


jitter and rate vs gain

Gain [mV/fC]	Amplitude [mV]	Jitter [ps]	Noise [e-]	Max rate [MHz]
26	211	19.8	779	300
34	274	18.5	610	227
44	352	19.8	493	128

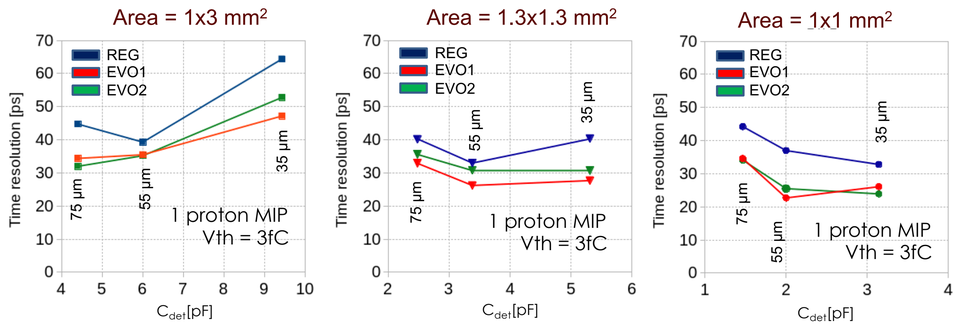
- Gain does not affect significantly the timing performances
- Generally noise decreases with gain
- Gain ↓ → max rate ↑

Jitter vs Q_{in}



- The MPV in 50 µm A UFSD sensor with a gain of 15 is 8 fC. For this charge, jitter is below 20 ps for EVO channels and around 25 ps for REGULAR
- Jitter for the three flavors is less than the expected sensor contribution which is 30 ps (in 50 µm UFSD)
- Jitter is reduced if C_{det} decreases. With a 3.4 pF sensor, jitter in the three cases is less than 15 ps
- Jitter becomes negligible (about 10 ps) for high values of Qin

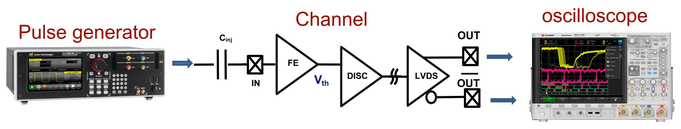
Time resolution vs sensor geometry vs sensor thickness

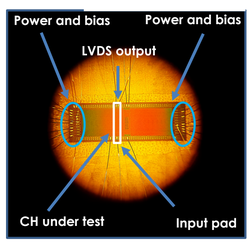


- 3 geometries
- 3 thicknesses
- 3 front-ends

- Area=1x3mm²: time resolution depends on the sensor thickness. **Larger pads require thicker sensors**
- Area=1.3x1.3mm²: good balance between sensor and electronics contribution. In this case time resolution does not depend on the sensor thickness
- Area=1x1mm²: the best time resolution is obtained with thin sensors.

First test setup





Power consumption

Domain	Expected	Measured
Anag & Dig 1.2V	62 mA	60 mA
IO 2.5 V	18 mA	20 mA

Preliminary channel functionality test: Voltage response to an injected pulse

Outlooks

- The three flavors characterization campaign is ongoing
- Test with different UFSD sensors: laser and active sources
- Test beam with protons is planned in 2020
- A 65 nm design porting is planned for the selected version while a TDC solution will be studied (both FPGA and ASIC embedded) for a full channel ASIC tape-out (3rd-4th quarter 2020)

References: [1] G. Paternoster et al., "Developments and first measurements of Ultra-Fast Silicon Detectors produced at FBK", JINST 12 (2017) C02077 ;

Contact: olave@to.infn.it