4D-tracking: LGAD and fast Timing Detectors

N. Cartiglia

VCI2022

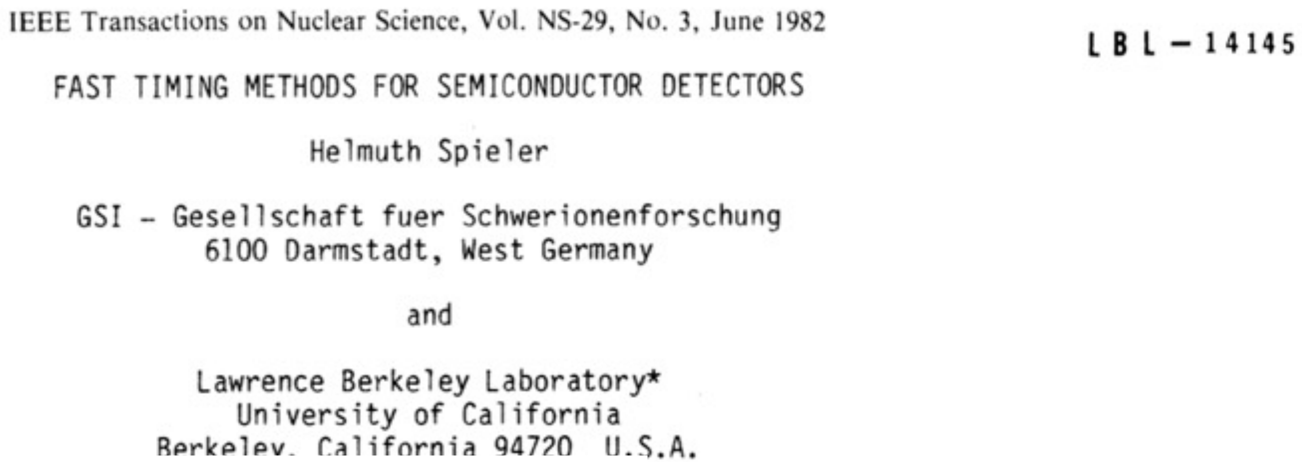
Silicon sensors as accurate timing detectors

Up to about 10 years ago, silicon sensors were not considered mainstream MIP timing detectors.

Presently, they are considered the most likely (only?) solution for 4D trackers.

In the presentation, I will outline this evolution

Two inspiring early papers



IEEE Transactions on Nuclear Science, Vol. NS-29, No. 3, June 1982

LBL-14145

FAST TIMING METHODS FOR SEMICONDUCTOR DETECTORS

Helmuth Spieler

GSI - Gesellschaft fuer Schwerionenforschung
6100 Darmstadt, West Germany

and

Lawrence Berkeley Laboratory*
University of California
Berkeley, California 94720 U.S.A.

404 IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 58, NO. 2, APRIL 2011

Increased Speed: 3D Silicon Sensors;
Fast Current Amplifiers

Sherwood Parker, Angela Kok, Christopher Kenney, Pierre Jarron, Jasmine Hasi, Matthieu Despeisse,
Cinzia Da Via, and Giovanni Anelli

Setting the stage: the ECFA report

The European Committee of Future Accelerators (ECFA) has identified as fundamental for future research programs several detectors R&D (Susanne's talk on Monday).

Sensors for 4D-tracking

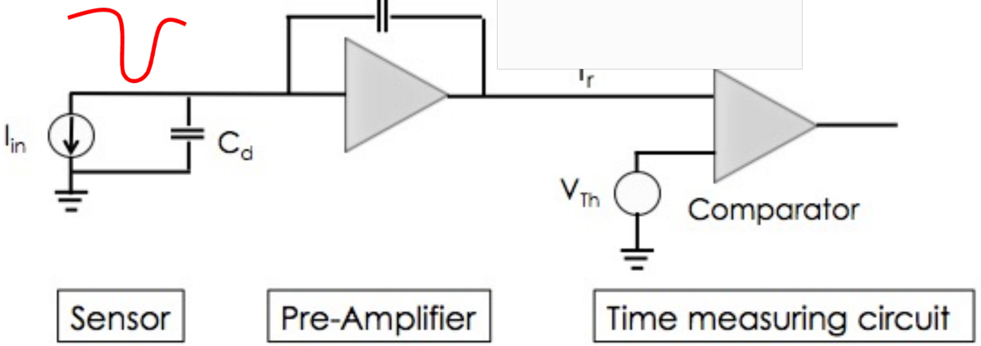
- Understand the ultimate limit of precision timing in sensors with and without internal multiplication;
- Develop sensors with internal multiplication with 100% fill factors and pixel-like pitch;
- Investigate production of sensors with internal multiplication in a monolithic design;
- Increase radiation resistance, push the limit of 3D sensors and explore LGAD and MAPS capabilities;
- Investigate the use of BiCMOS MAPS, exploiting the properties of SiGe.

This is therefore the outline of my talk (even though not in this order)

I will pick examples of various R&D projects (not inclusive)

Silicon time-tagging detector

- Sensors produce a current pulse
- The read-out measures the time of arrival



Sensors and read-out are two parts of a single object, sometimes even on the same substrate (monolithic option).

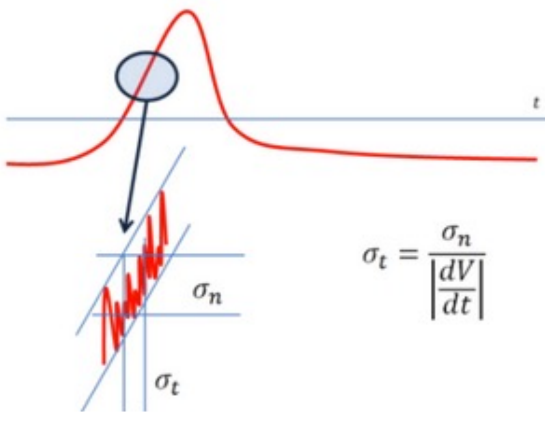
Sensors and electronics succeed (or eventualy fail) together

In “timing circuits”, things can go wrong very rapidly (quote stolen from a chip designer)

==> this is not a simple evolution of what we know how to do.

Temporal resolution

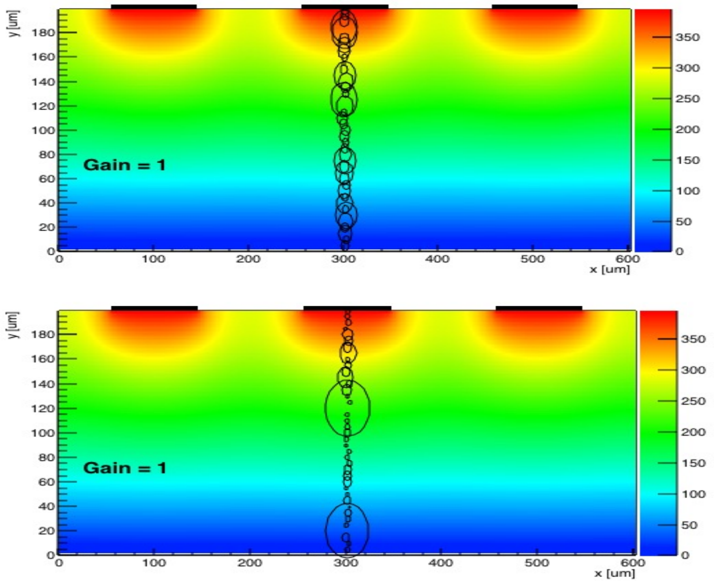
$$\sigma_t^2 = \left(\frac{Noise}{dV/dt}\right)^2 + (\Delta ionization)^2 + (\Delta shape)^2$$



“Jitter” term

Small noise ==> choice of electronic technology

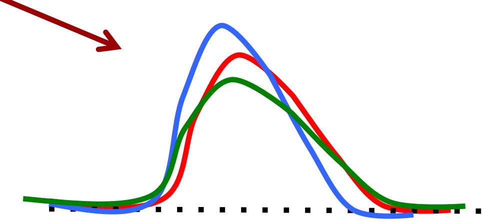
Large dV/dt ==> use sensors with internal gain



Amplitude variation ==> corrected offline (time walk)

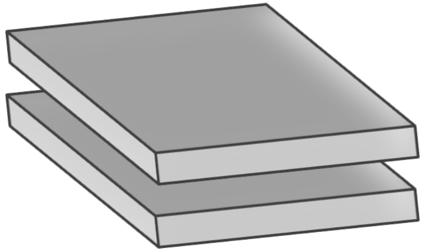
Non-homogeneous energy deposition ==> variation of signal shape

Cannot be corrected, minimized by design



Signal shape is determined by Ramo’s Theorem

$$i \propto qvE_w$$



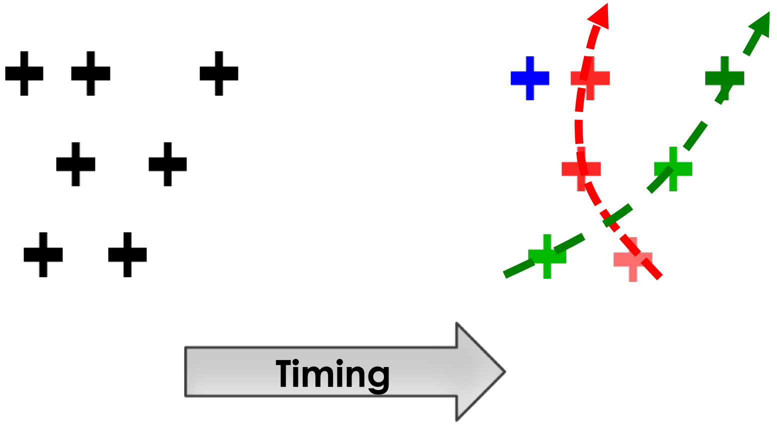
Saturated drift velocity v everywhere in the sensor volume

Uniform weighting field E_w

==> Needs parallel plate geometry

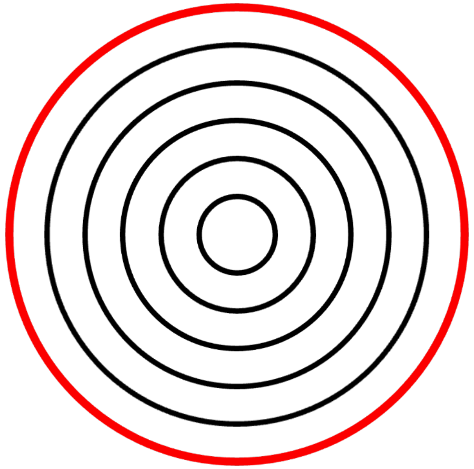
Timing layers and 4D tracking

By "**4D tracking**" we mean the process of assigning a spatial and a temporal coordinate to a hit.



Timing can be available at different levels of the event reconstruction:

1) Timing in a single point (timing layer ATLAS,CMS)



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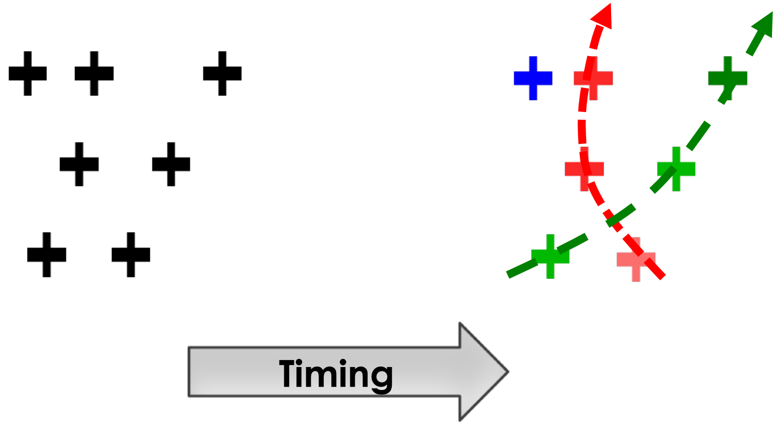
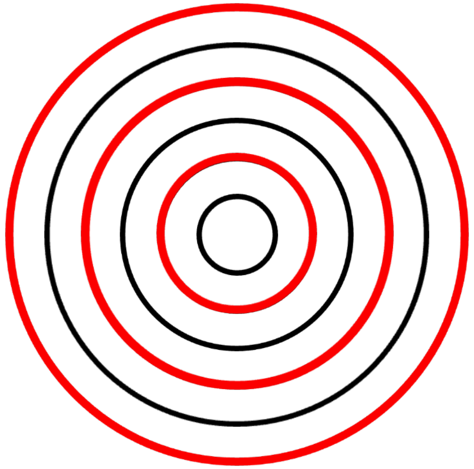


Timing can be available at different levels of the event reconstruction:

1) Timing in a single point (timing layer ATLAS,CMS)
2) Timing at some points along the track



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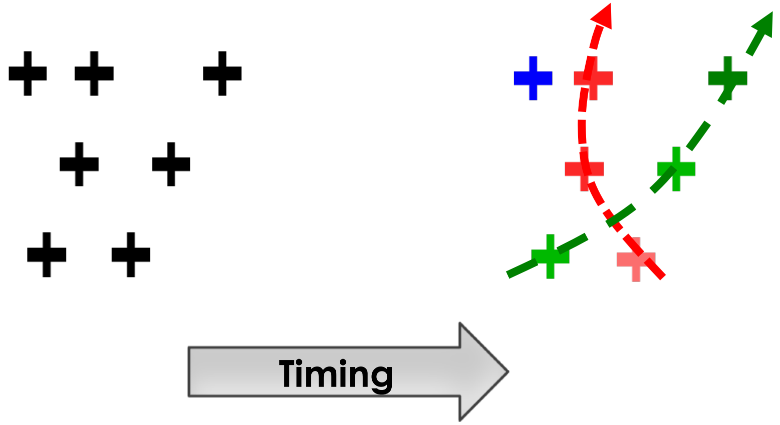
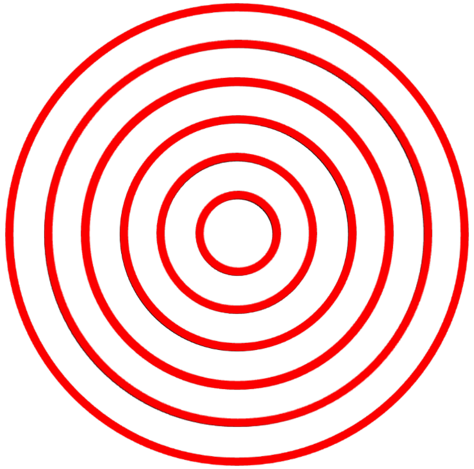


Timing can be available at different levels of the event reconstruction:

1) Timing in a single point (timing layer ATLAS,CMS)
2) Timing at some points along the track
3) Timing at each point along the track



Timing layers and 4D tracking

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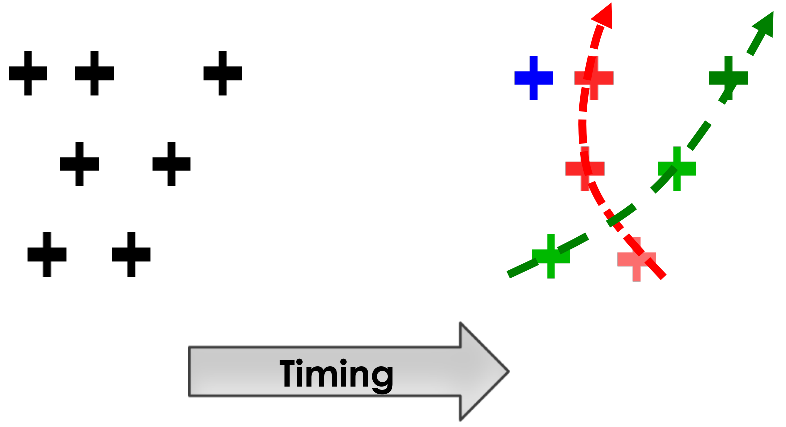

Timing can be available at different levels of the event reconstruction:

1) Timing in a single point (timing layer ATLAS,CMS)
2) Timing at some points along the track
3) Timing at each point along the track

Many timing coordinates per track yield to better performing detectors, but require much more complex read-out systems.

Some projects will be perfectly fine with having a limited set of timing points

Systems designed for accurate timing - I

In a large detector system, good temporal resolution has many parts:

1. **The sensor**
2. **The design of the ASIC:**
   - Technology (process, BW..)
   - Money
   - Power available
2. **Detector design:**
   - Cabling, module quality, noise rejection
   - quality of power supply etc
3. **Infrastructure:**
   - Clock distribution
   - Cooling
   - Data transfer

ECFA recommendations:

Electronics for 4D-tracking

- High-performance sampling (TDC, ADC)
- High-precision timing distribution

4D tracking detectors need very strong R&Ds in many additional aspects

(these challenges are now faced by the ATLAS and CMS timing layers)

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ECFA recommendations:

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need very strong R&Ds in

ional aspects

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ing layers)

Personal view: the design of the electronics is much harder than the design of the sensors.

(that is why I work on sensors!)

As the community gain experience from present projects, in the next few years we will witness strong evolution of the electronics

Interplay of power, pixel size, and electronics

The Pixel size, the temporal and the spatial resolutions are interlinked,
==> each application will need a specific optimization

	Temporal precision	Spatial precision
Pixel size	**relevant**	**Very relevant**
Area needed by electronics	**Larger**	**Smaller**
Power consumption	**Very high**	**Rather low**

Interplay of power, pixel size, and electronics

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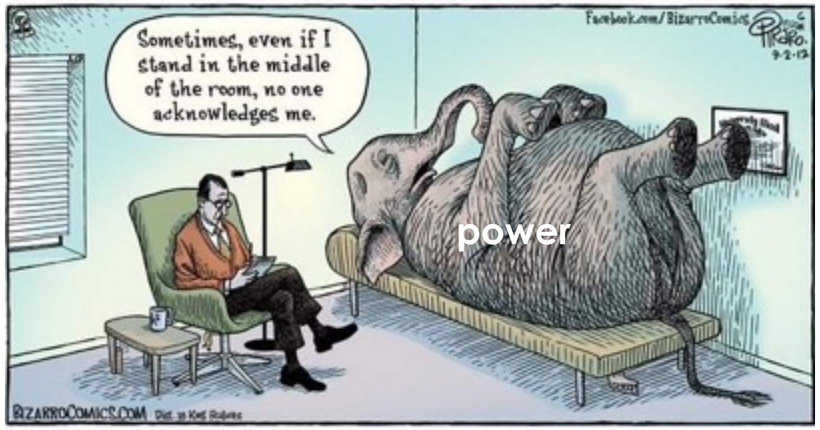
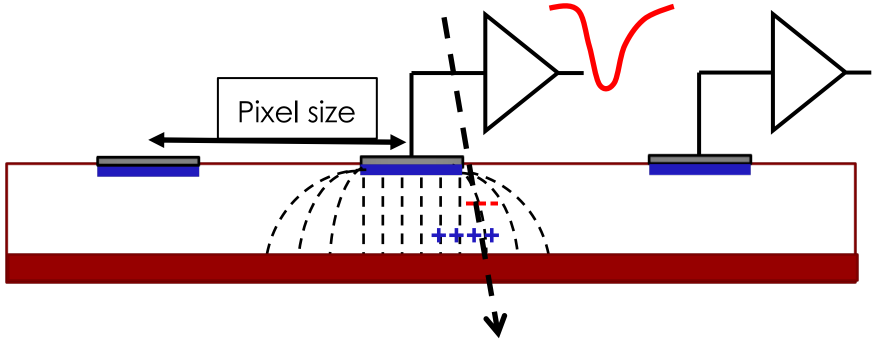
Power will determine the architecture of 4D tracking detectors.
Power density limits the pixel size and the temporal precisions



Spatial precision: single and multi pixels read-out

Single pixel

where the charge is collected in one pixel



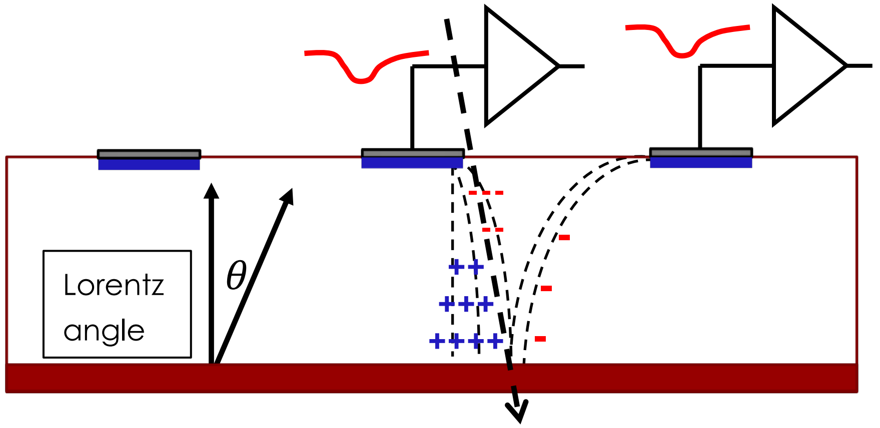
$$\sigma_x = k\,\frac{pitch}{\sqrt{12}},\ k \sim 0.5 \text{ - } 1$$

- $\boldsymbol{\sigma_x}$ **depend on the pixel size**

  pixel = 100 $\boldsymbol{\mu m}$ ➔ $\boldsymbol{\sigma_x = 20\ \mu m}$

Multi pixels

where the charge is collected in a few pixels



$$x_i = \frac{A_i x_i}{\sum_1^2 A_l x_l}$$

- $\boldsymbol{\sigma_x}$ **<< pixel size**
- Sensors have to be thick to maintain efficiency
- Need B field (or floating electrodes) to spread the signal

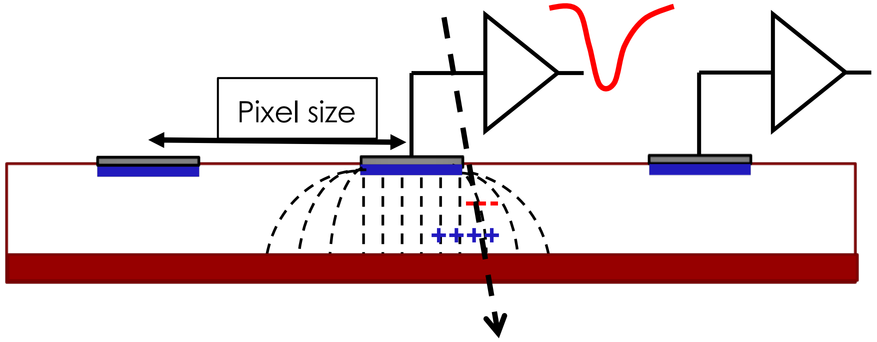
Spatial precision: single and multi pixels read-out

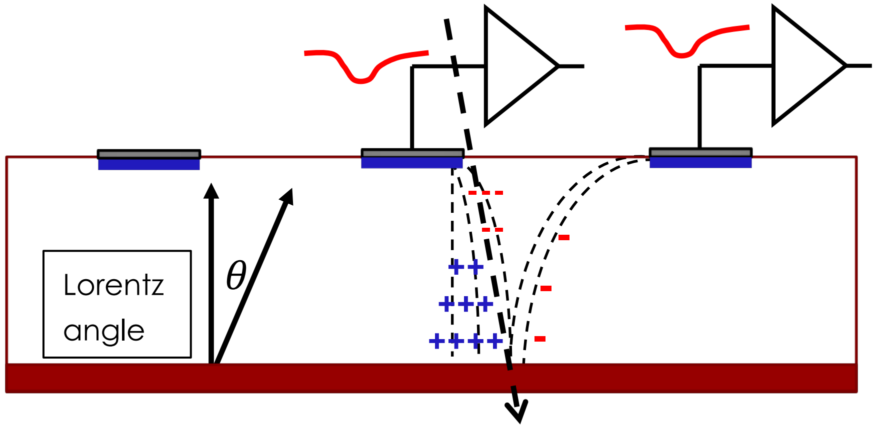
Single pixel

where the charge is collected in one pixel

Multi pixels

where the charge is collected in a few pixels





$$\sigma_x = k\,\frac{pitch}{\sqrt{12}},\ k \sim 0.5 - 1$$

$$x_i = \frac{A_i x_i}{\sum_1^2 A_l x_l}$$

- σ_x **depend o**

  pixel =

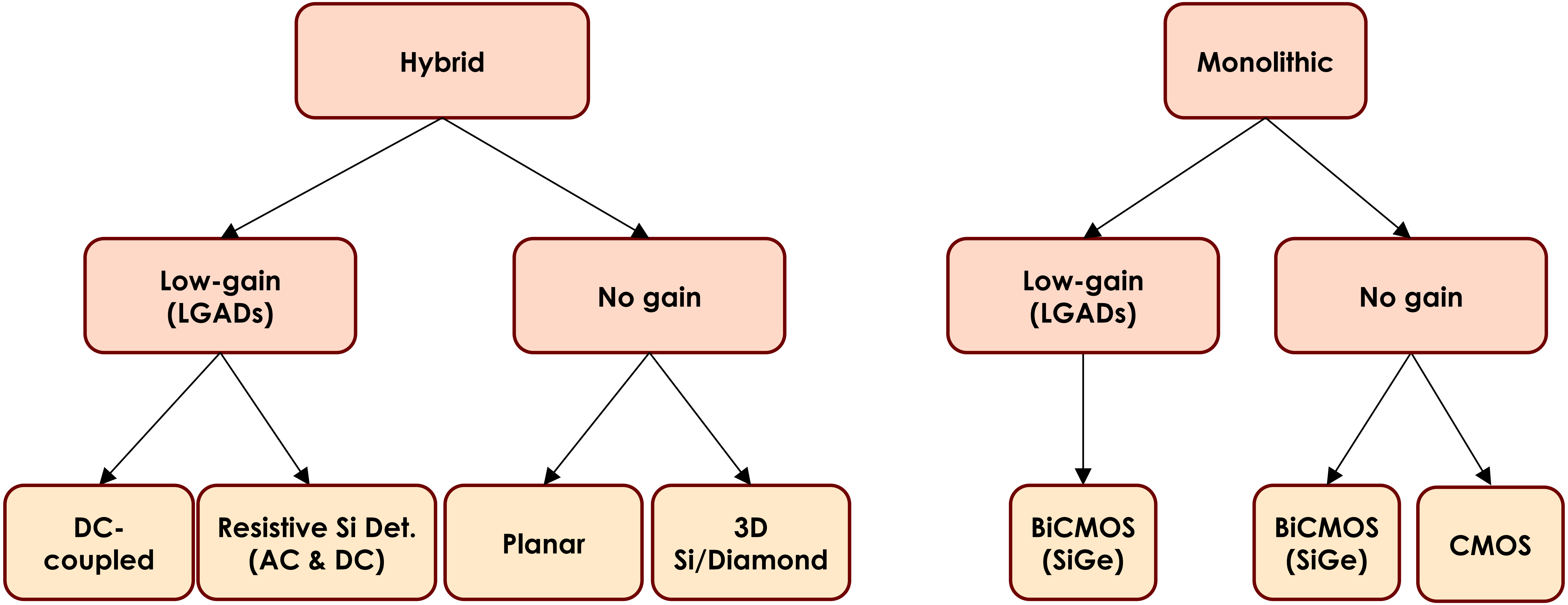
y

- Need B field (or floating electrodes) to spread the signal

If the single pixel design is choosen, the number of pixels becomes very large, the electronics has very little space available, and the power consumption increases steeply, probably to unmanageble levels

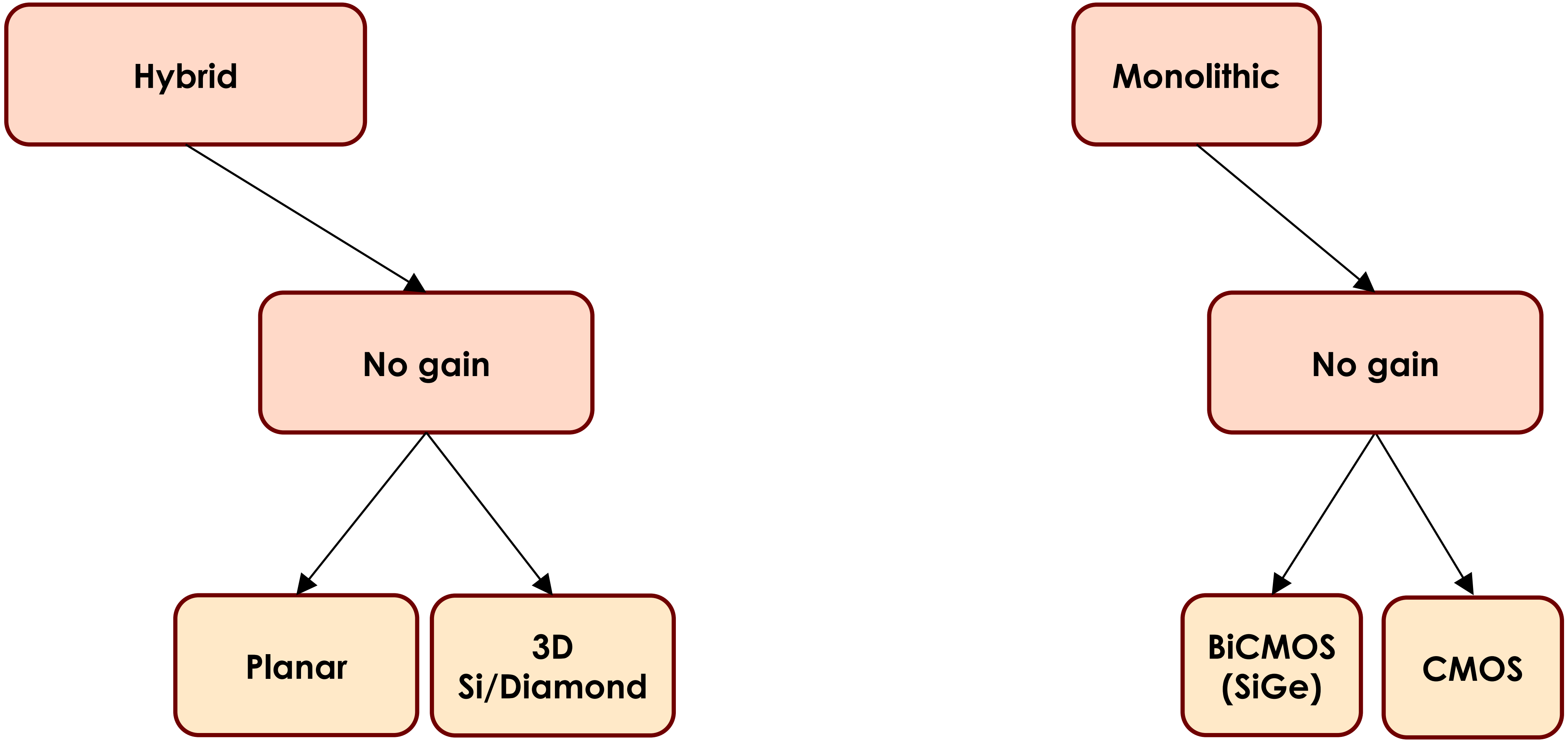
Presently explored options

The present R&D in position sensitive timing detectors shows the same variety that is present in standard silicon sensors. In the following, I will cover a few examples from this chart.



- **Hybrid**
  - **Low-gain (LGADs)**
    - **DC-coupled**
    - **Resistive Si Det. (AC & DC)**
  - **No gain**
    - **Planar**
    - **3D Si/Diamond**
- **Monolithic**
  - **Low-gain (LGADs)**
    - **BiCMOS (SiGe)**
  - **No gain**
    - **BiCMOS (SiGe)**
    - **CMOS**

Sensors without internal gain



Hybrid

No gain

Planar

3D
Si/Diamond

Monolithic

No gain

BiCMOS
(SiGe)

CMOS

Sensors without internal gain

Hybrid

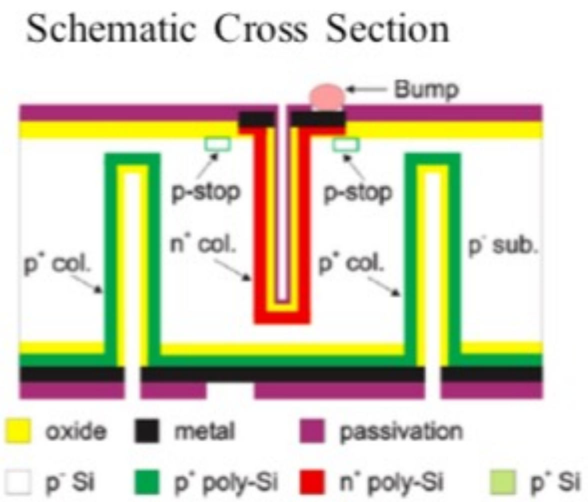
No gain

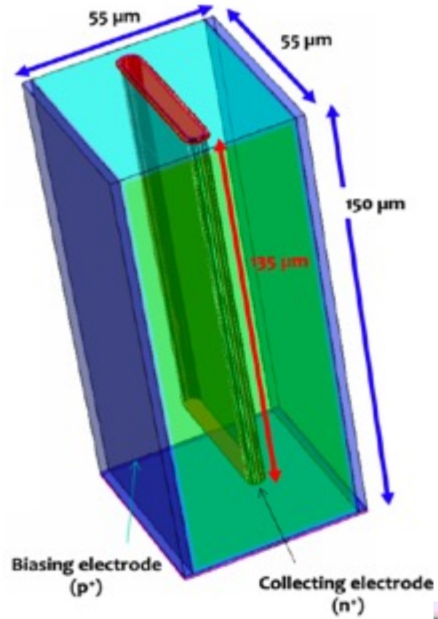
3D Si/Diamond

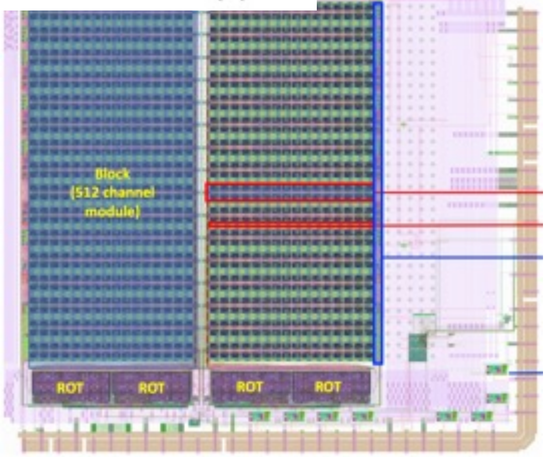
Two possible options:

- Column
- Trenches
- The amount of charge is controlled by the sensor thickness (~1-2 fC)

Both requires small pixels to achieve good temporal precision
==> very good position resolution





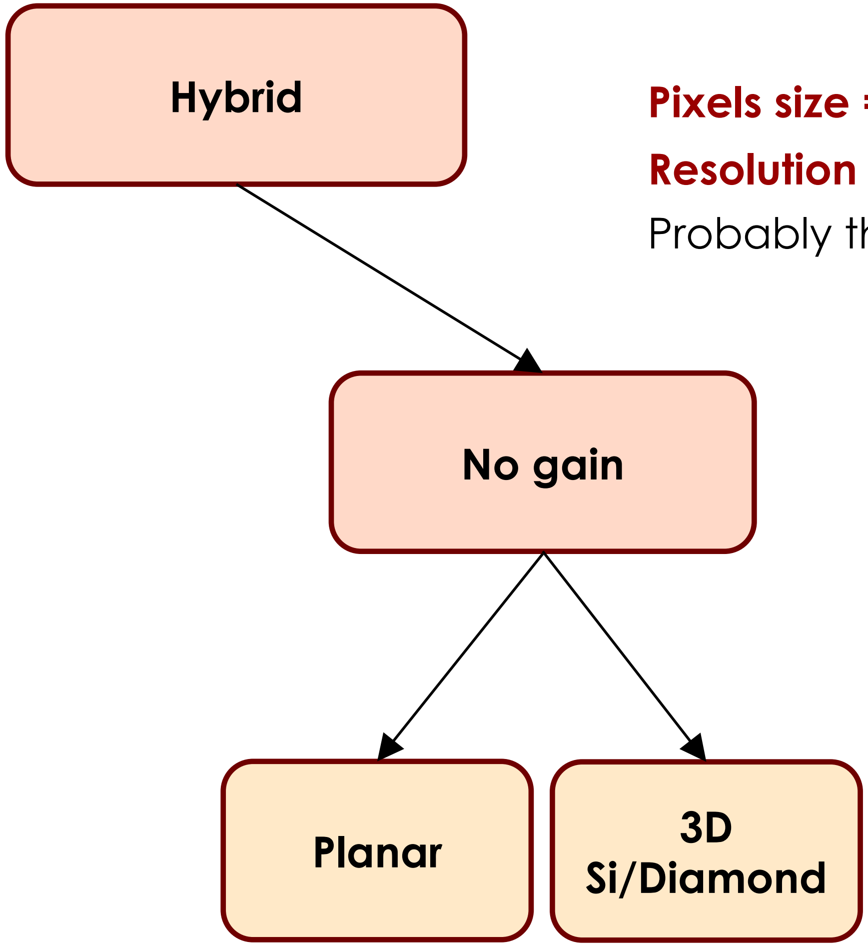


Timespot1: 28 nm ASIC

Pixels size = 55 μm
Resolution ~ 30 ps for single channel

See M. Veltri "4D diamond detector", VCI2022 Friday morning

Sensors without internal gain



The ASIC Timepix family

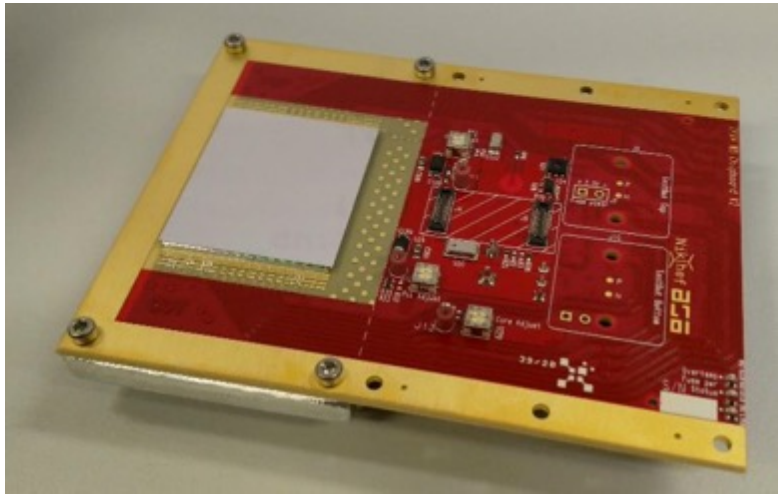
The latest addition: Timepix4

==> 65 nm ASIC, 512 x 448 pixels

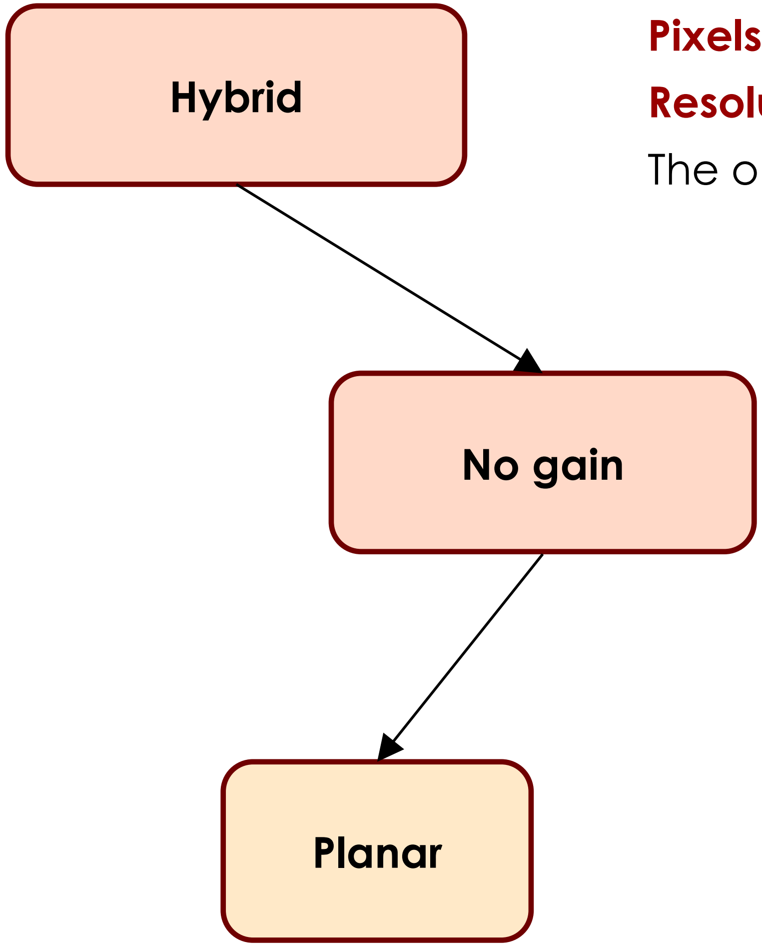
Pixels size = 55 μm

Resolution in line with expectations ~ 200 ps RMS

Probably the best example so far of a full 4D tracking system

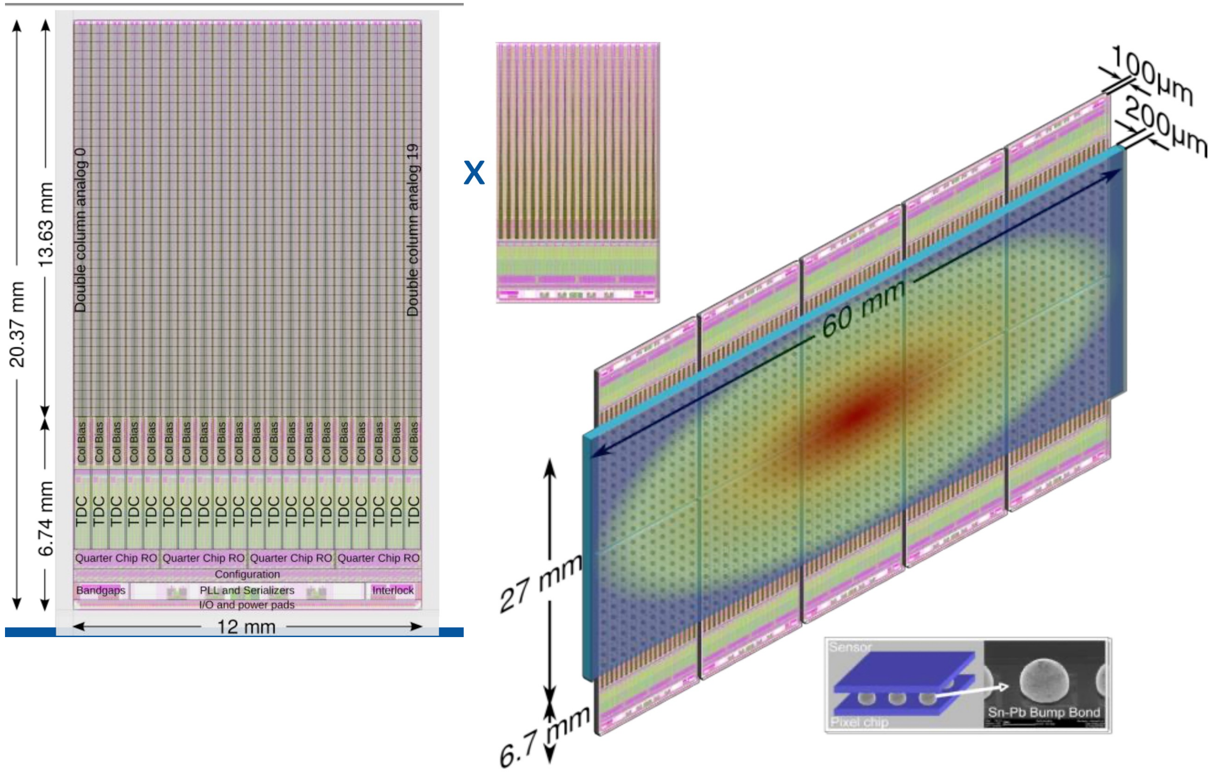


Sensors without internal gain



The TDCpix ASIC of the NA62 Gigatracker
==> 130 nm ASIC, 45 x 40 pixels

Pixels size = 300 x 300 μm^2
Resolution ~ 120 ps RMS
The only 4D tracking system on a working experiment



Sensors without internal gain

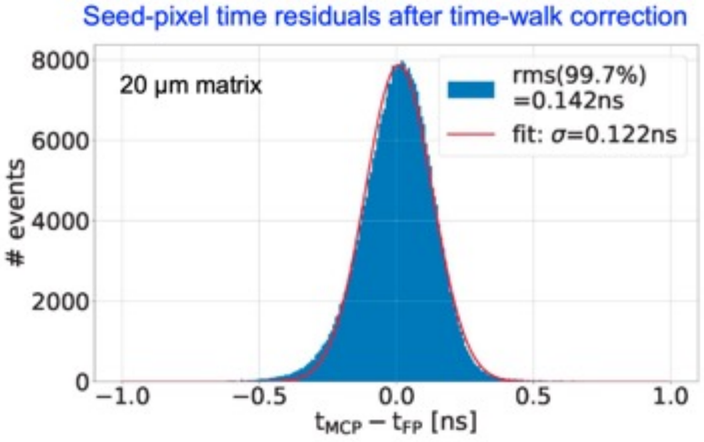
FASTPIX is a 180 nm CMOS monolith project

aiming at combining temporal stamping with excellent position precision

Lateral doping gradient leads to accelerated charge collection

Resolution of about ~ 120 ps,

Very small pixels

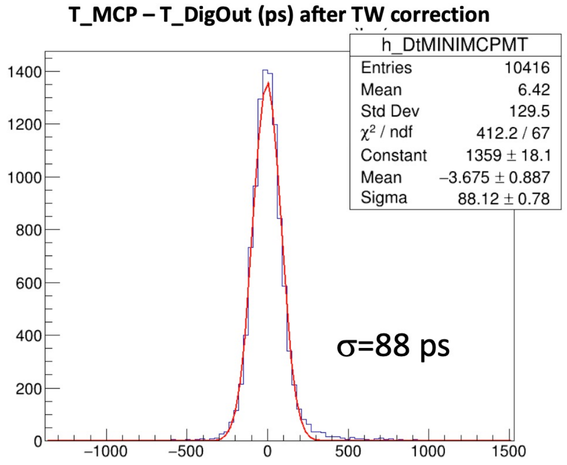


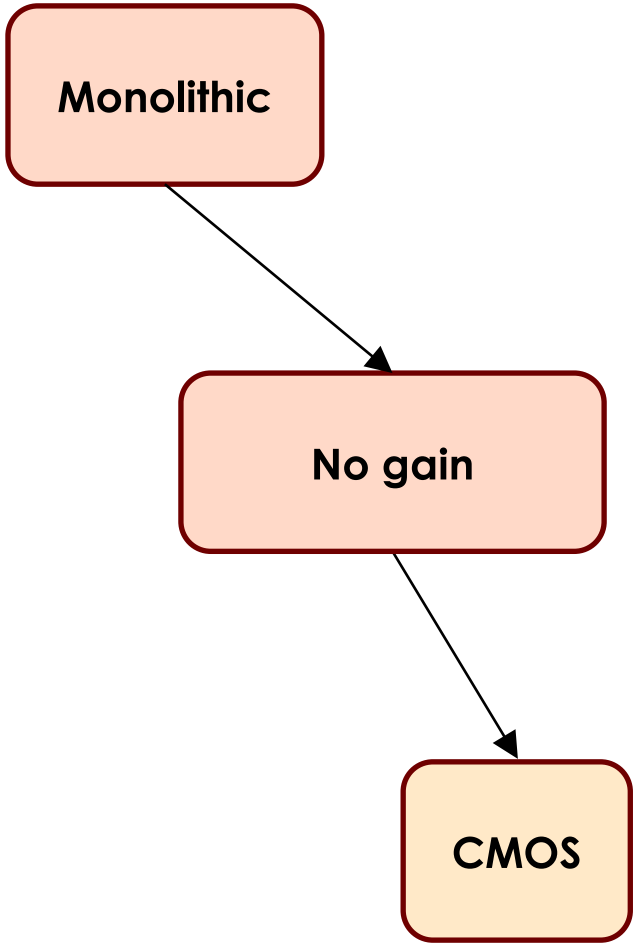
MiniCACTUS is a 150 nm CMOS monolith project

Front-end mostly optimized for 1 mm^2 pixels with peaking time of 1-2 ns @ 1-2pF

Resolution of about ~ 90 ps,

Large pixel, 0.5 x 1 mm^2





See

D. Dannheim ”Silicon pixel detector R&D for future lepton colliders”, VCI2022 Thursday morning

Y. Degerli “Development of radiation hard depleted CMOS timing sensors”, VC2022, recorded

Sensors without internal gain

MonPicoAD project

Exploit SiGe performances

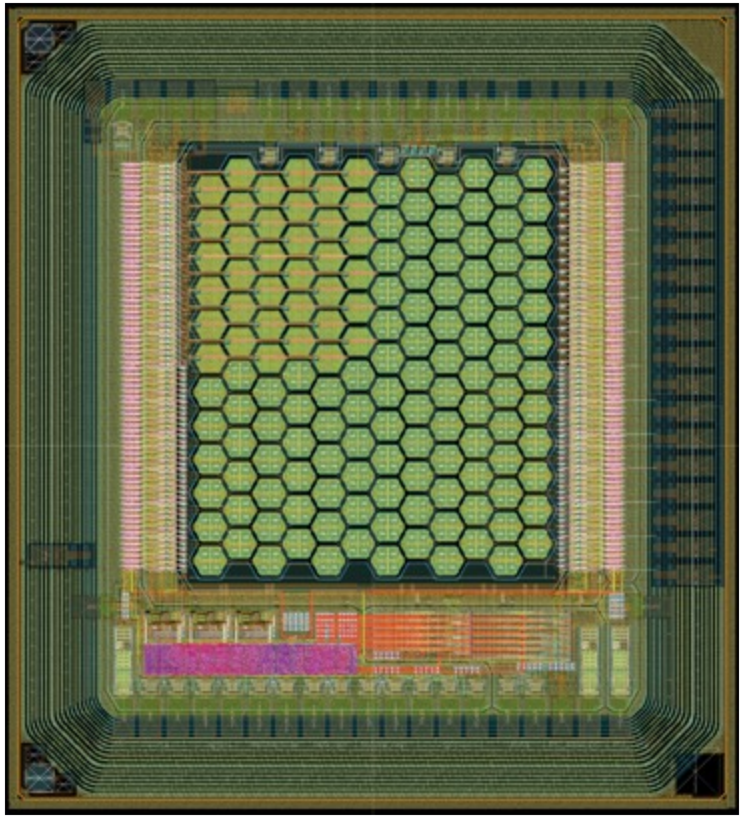
Exagonal pads, 65 μm

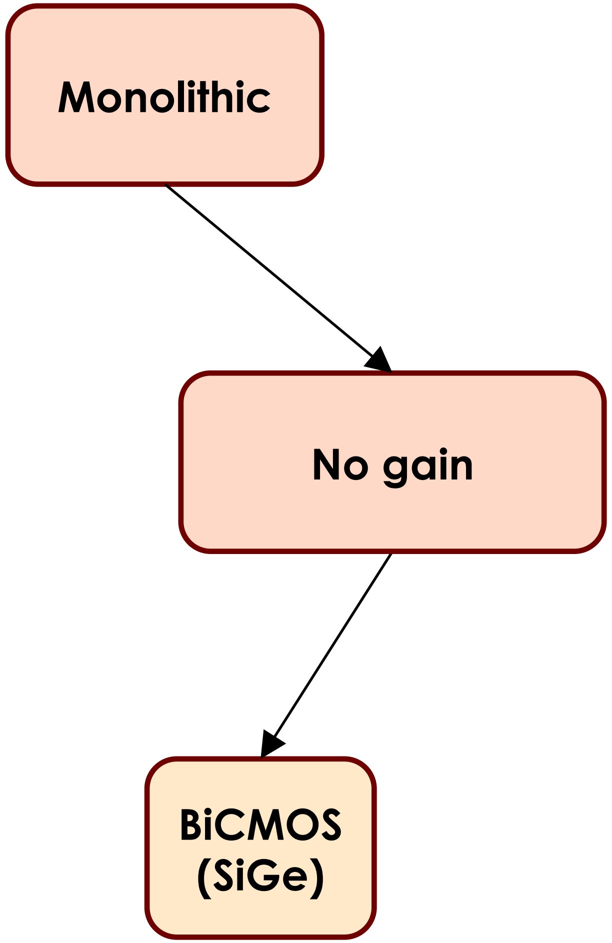
About 25 μm depletion

Thinned to 60 μm

Resolution of about ~ 36 ps,

Very small pixels





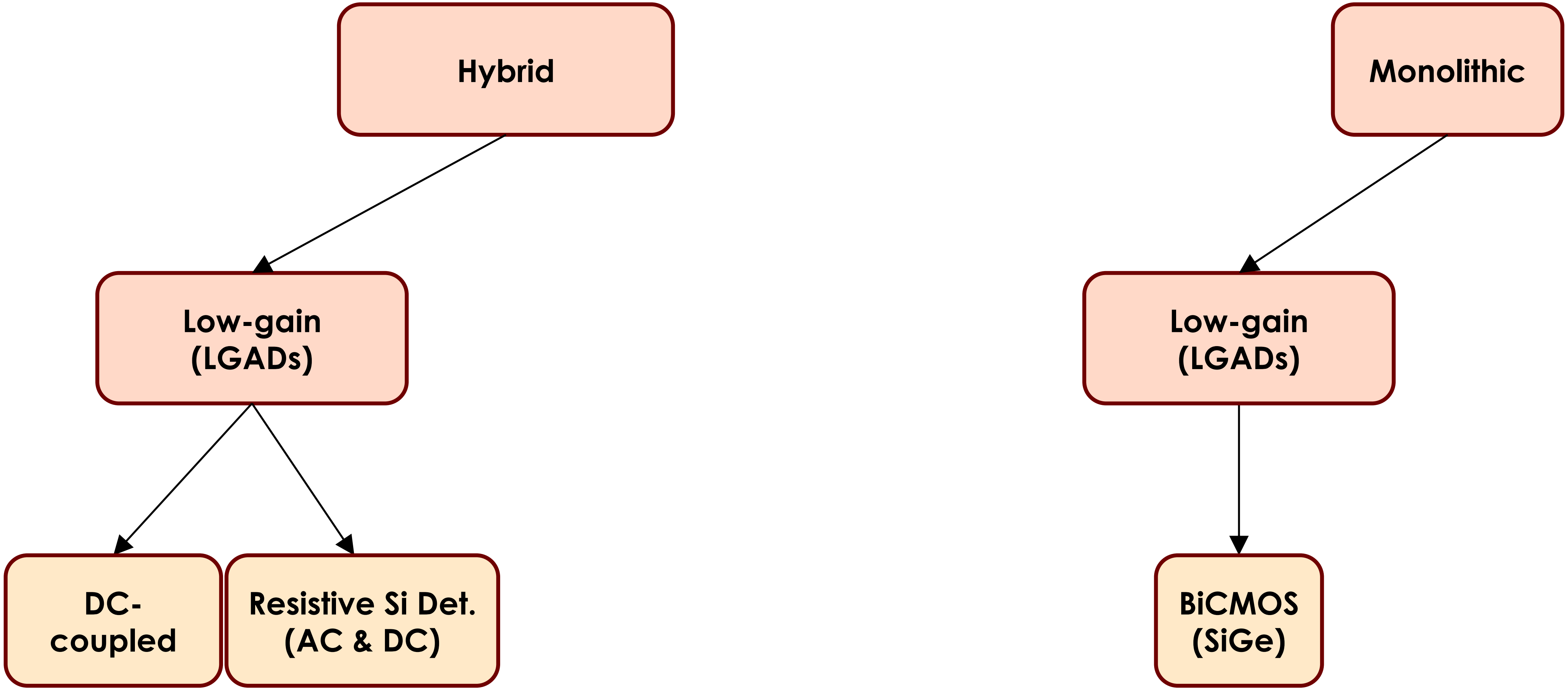
Monolithic

No gain

BiCMOS (SiGe)

See R. Cardella "Monolith", VCI2022 Thursday afternoon

Sensors with internal gain



Hybrid

Low-gain (LGADs)

DC-coupled

Resistive Si Det. (AC & DC)

Monolithic

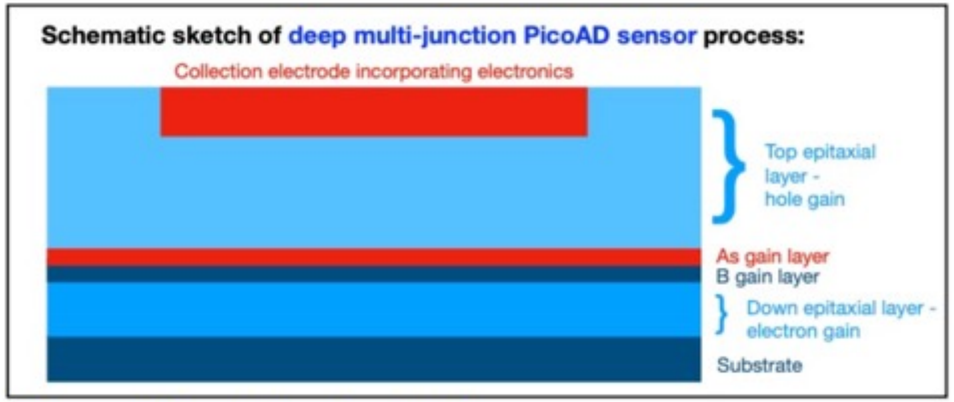
Low-gain (LGADs)

BiCMOS (SiGe)

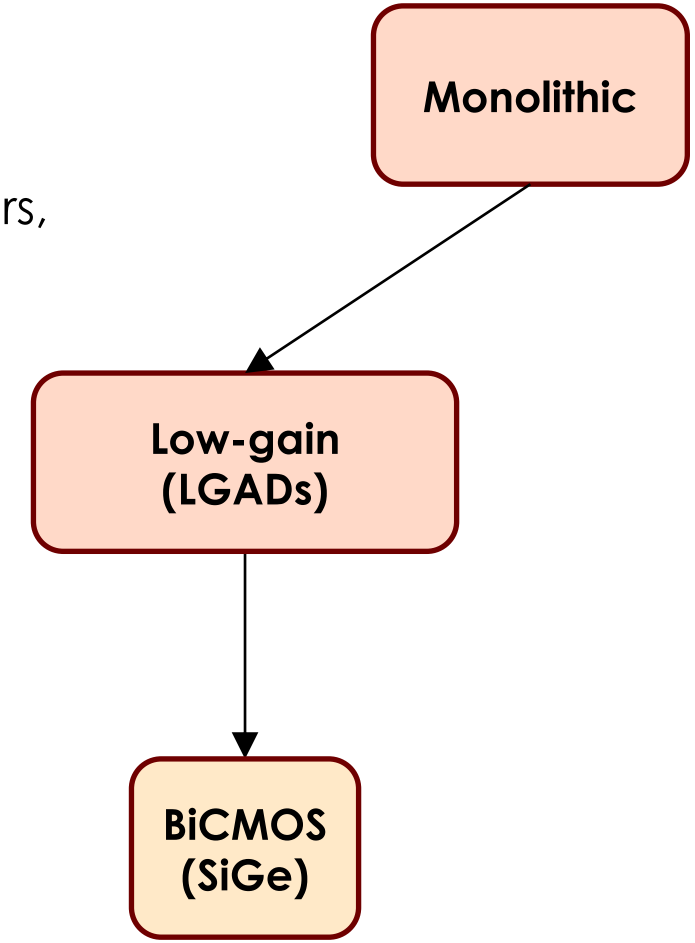
Sensors with internal gain

This is a very powerful research path pursued by the **“Monolith” project.**

Monolith merges low noise from SiGe with high dVdt from multiplications.
It aims at reducing the Landau term by using very thin sensors, and high pixelation by buring the high-field avay form the surface junction

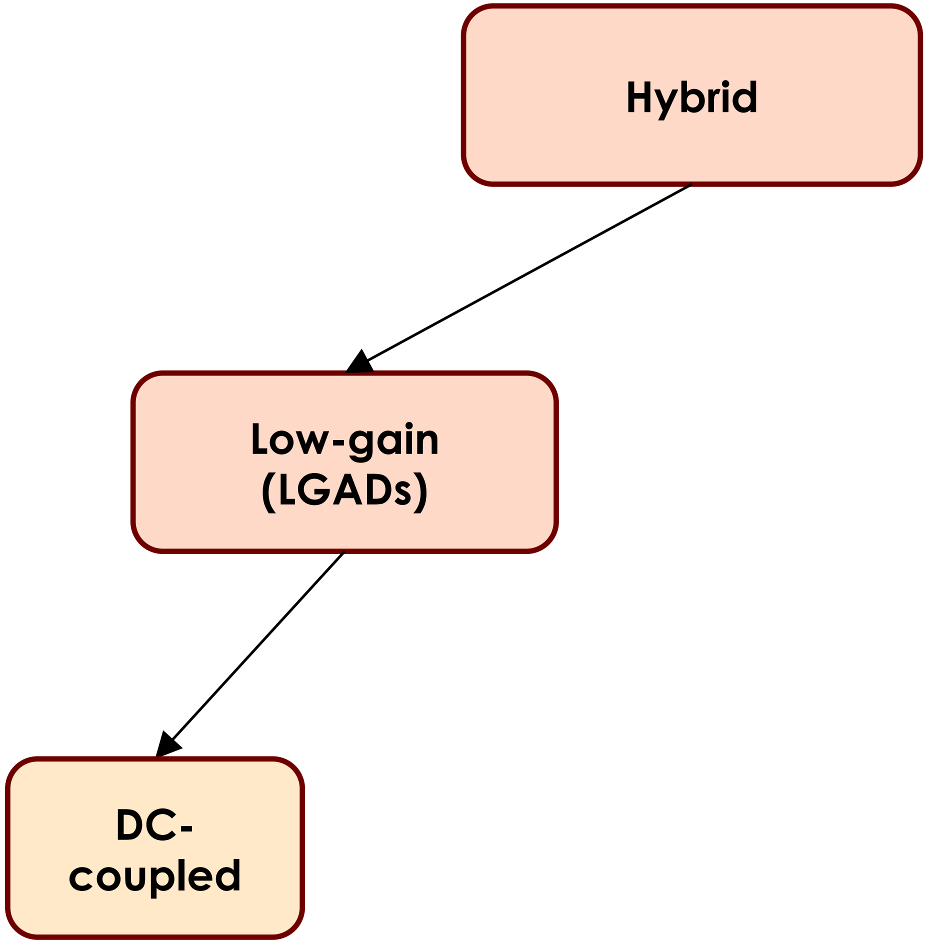


Placement of gain layer deep inside sensor:
De-correlation from pixel implant size/geometry —> high pixel granularity possible (*spatial precision*)
Only small fraction of charge gets amplified —> reduced Landau charge fluctuations (*timing precision*)



See R. Cardella ”Monolith”, VCI2022 Thursday afternoon

Sensors with internal gain: Ultra-Fast Silicon Detectors

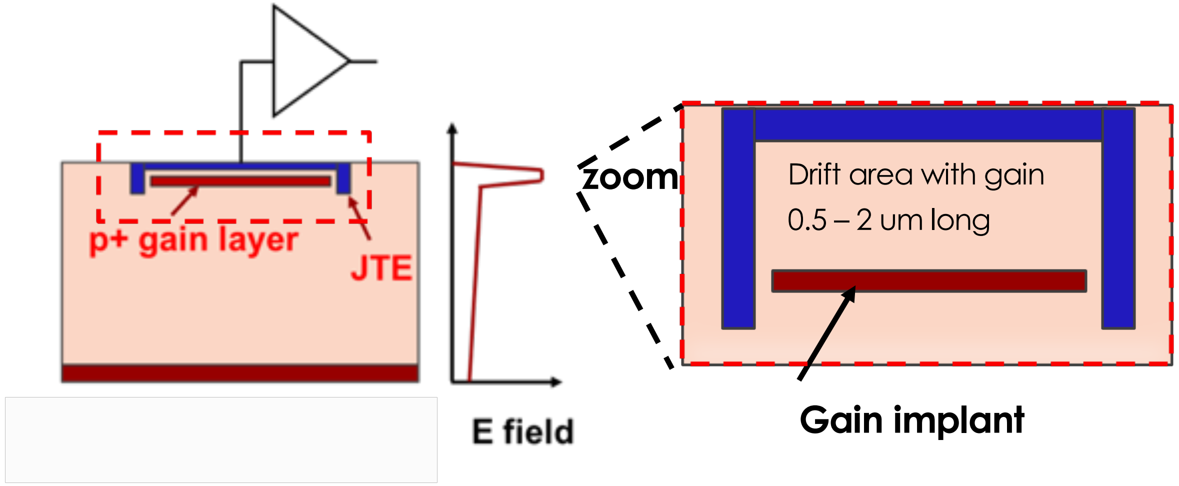


Hybrid

Low-gain (LGADs)

DC-coupled

First design innovation: low-gain avalanche diodes



- The low-gain mechanism (LGAD), obtained with a moderately doped p-implant, is the defining feature of the design.
- The low gain allows segmenting and keeping the shot noise below the electronic noise, since the leakage current is low.

Low gain minimizes jitter, it is the key ingredient to good temporal resolution

Nomenclature:

- UFSD are DC-LGAD optimized (drift velocity, weighting field, gain levels, edges) for timing

UFSD temporal resolution limit

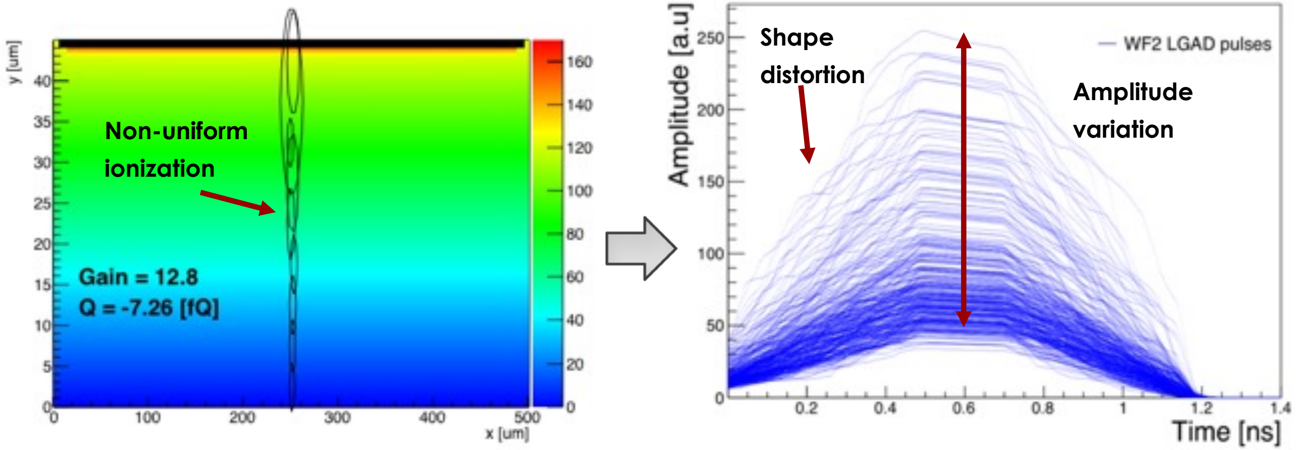
$$\sigma_t^2 = \left(\frac{Noise}{dV/dt}\right)^2 + (\Delta ionization)^2$$

Large dV/dt,
➔ small jitter

Non uniform ionization:

Physical limit of UFSD sensors

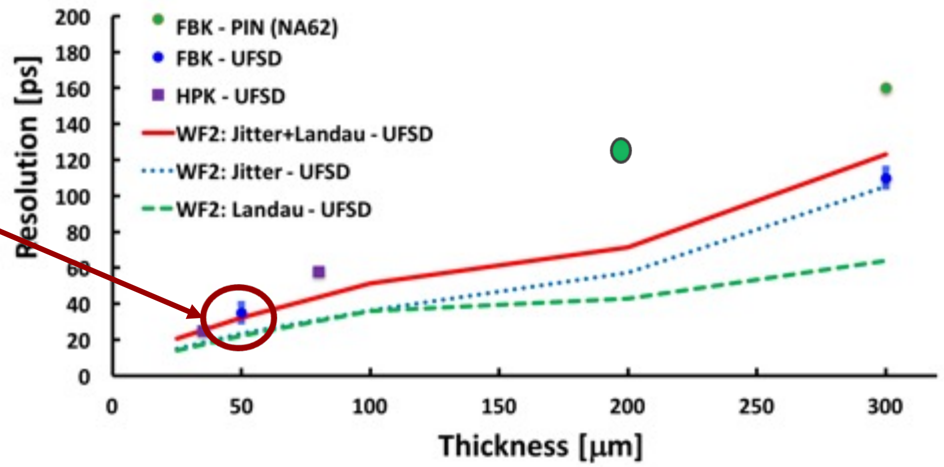
Simulation of signals in 50-um LGAD



There are now hundreds of measurements on 45-55 μm-thick UFSDs

➔ Sensor choice for the ATLAS and CMS forward timing layers

Comparison WF2 Simulation - Data
Band bars show variation with temperature (T = -20C - 20C), and gain (G = 20 -30)

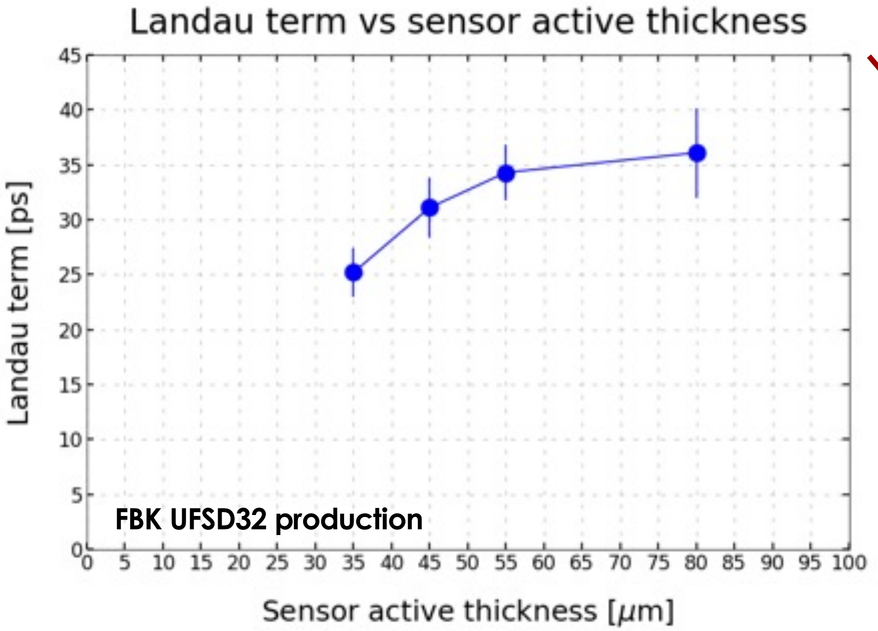


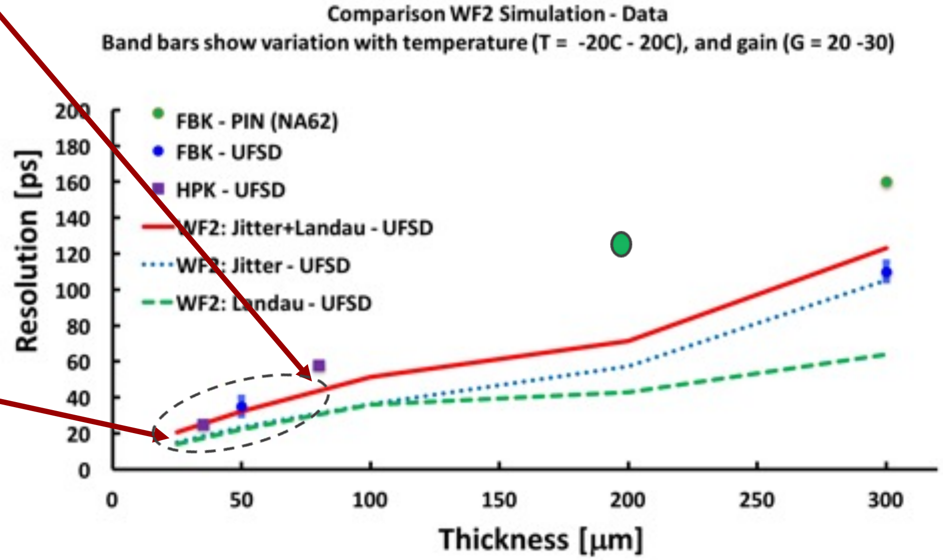
UFSD temporal resolution in thinner sensors

UFSD temporal resolution improves in thinner sensors:

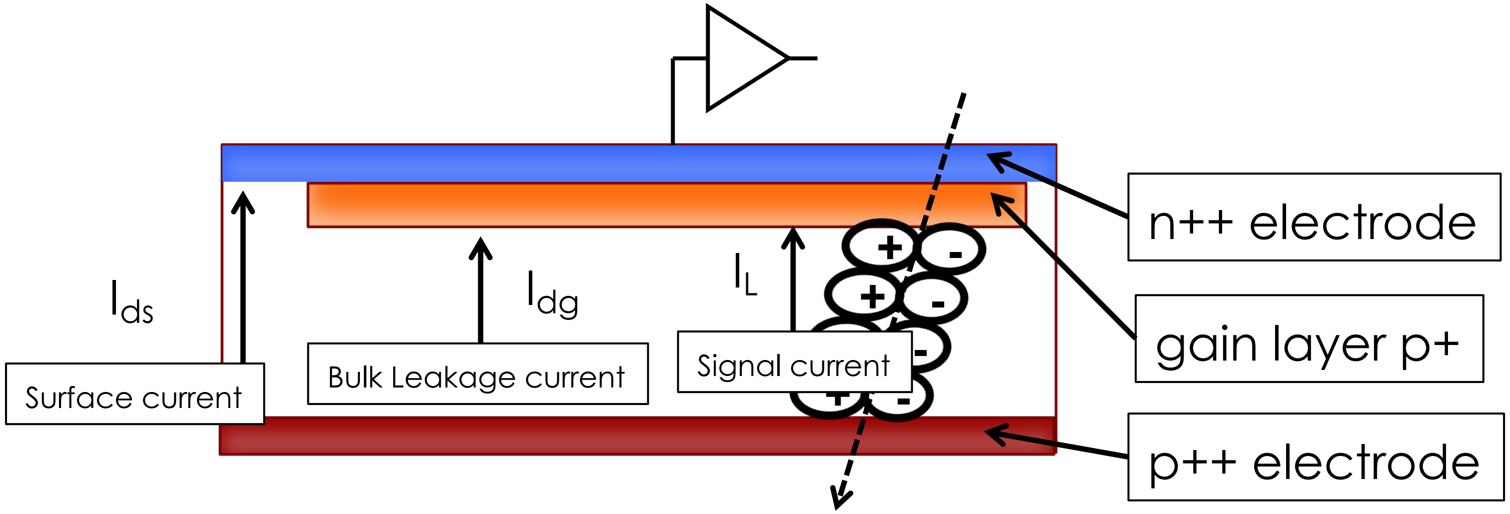
==> reasonable to expect 10-20 ps for 10-20 μm thick sensors.

Be aware: very difficult to do timing with small signals… power consumption increases





Extra: Current noise in UFSD



I_{ds}

Surface current

I_{dg}

Bulk Leakage current

I_L

Signal current

n++ electrode

gain layer p+

p++ electrode

$$i^2_{Shot} = 2eI_{Det} = 2e\left[I_{Surface} + (I_{Bulk} + I_{Signal})M^2F\right]$$

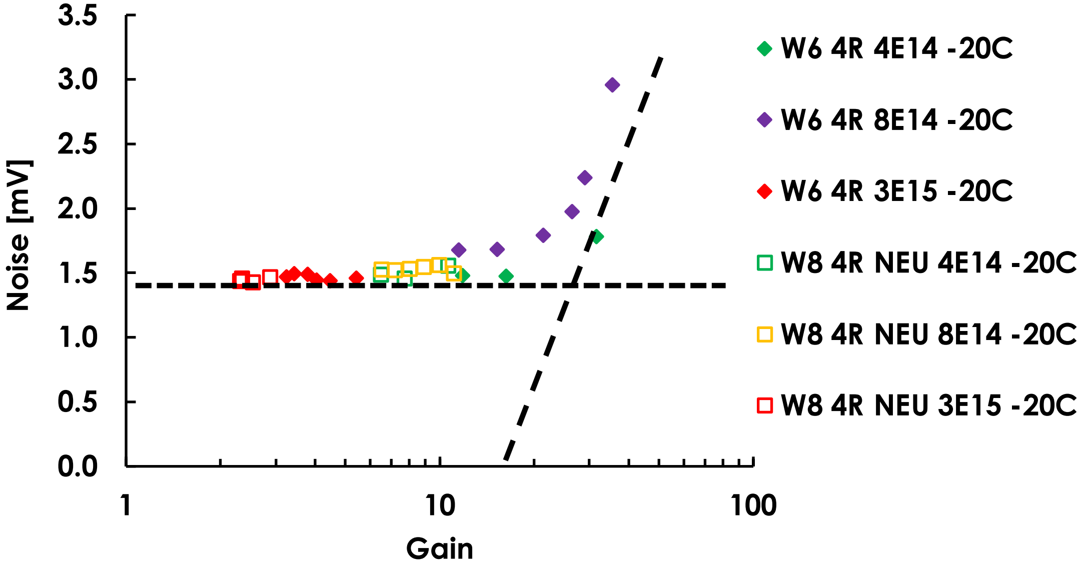
Excess noise factor:
Correction factor to the standard Shot noise,
due to the noise of the multiplication mechanism

$$F = Mk + \left(2 - \frac{1}{M}\right)(1-k)$$

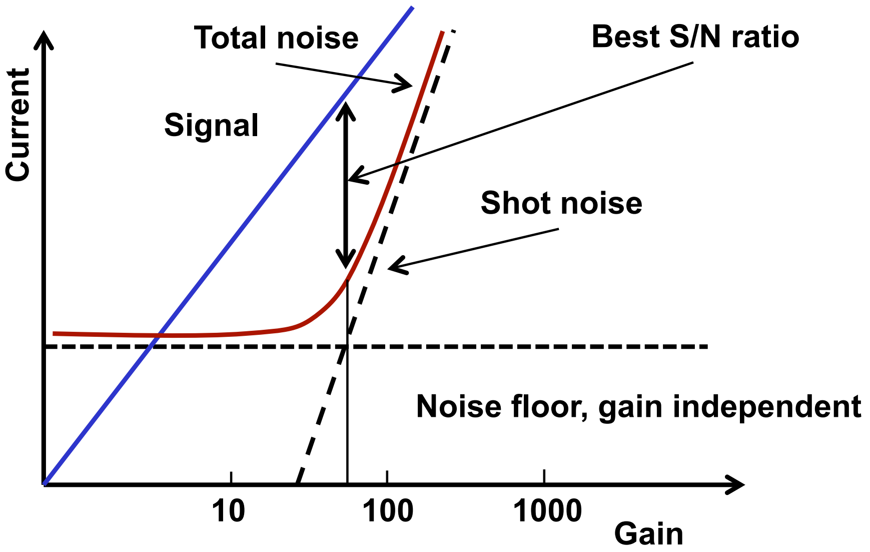
$$F \sim M^x$$

k = e/h ionization rate
x = excess noise index
M = gain

Extra: Noise increase as a function of fluence and gain

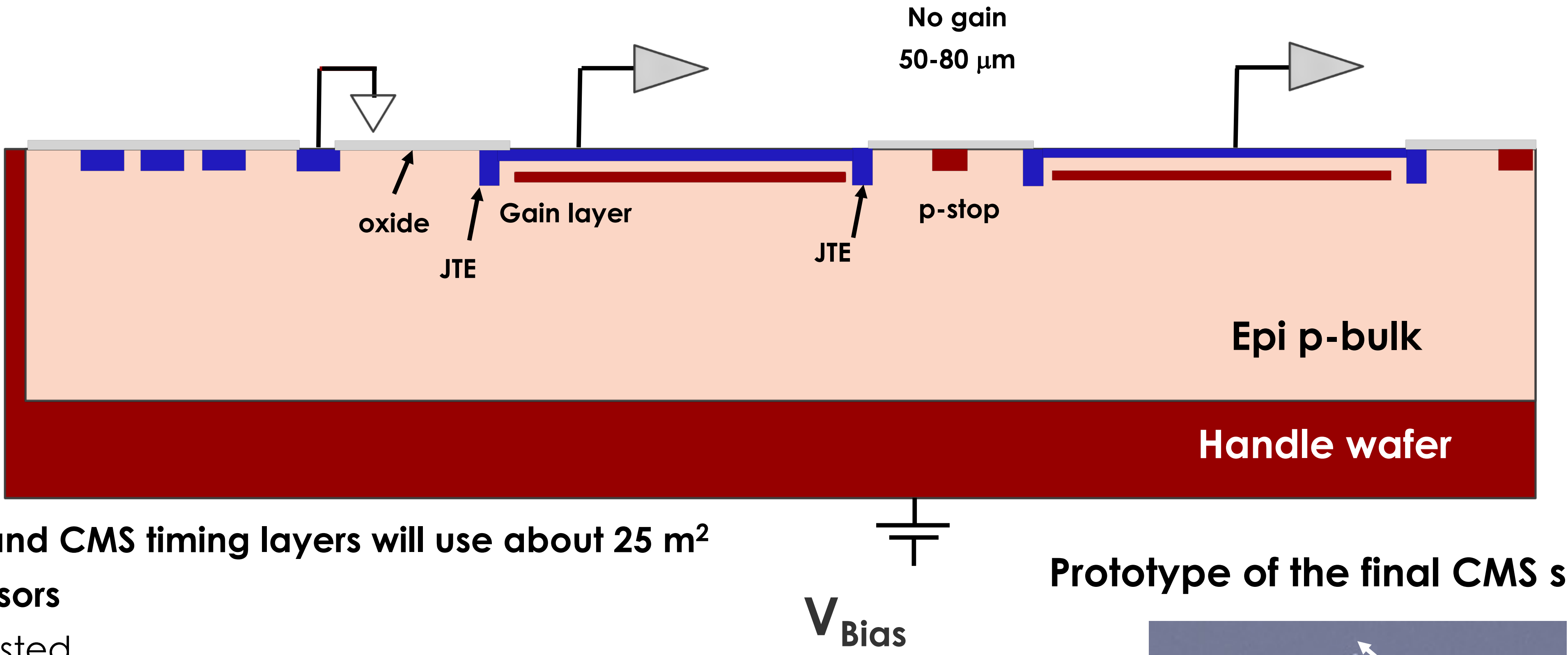


Data and model look similar.



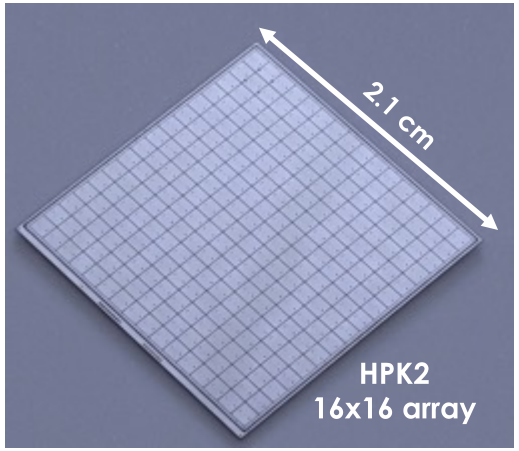
Goal: the noise from Silicon current should stay below that of the electronics

State-of-the-art: sensors for ATLAS and CMS



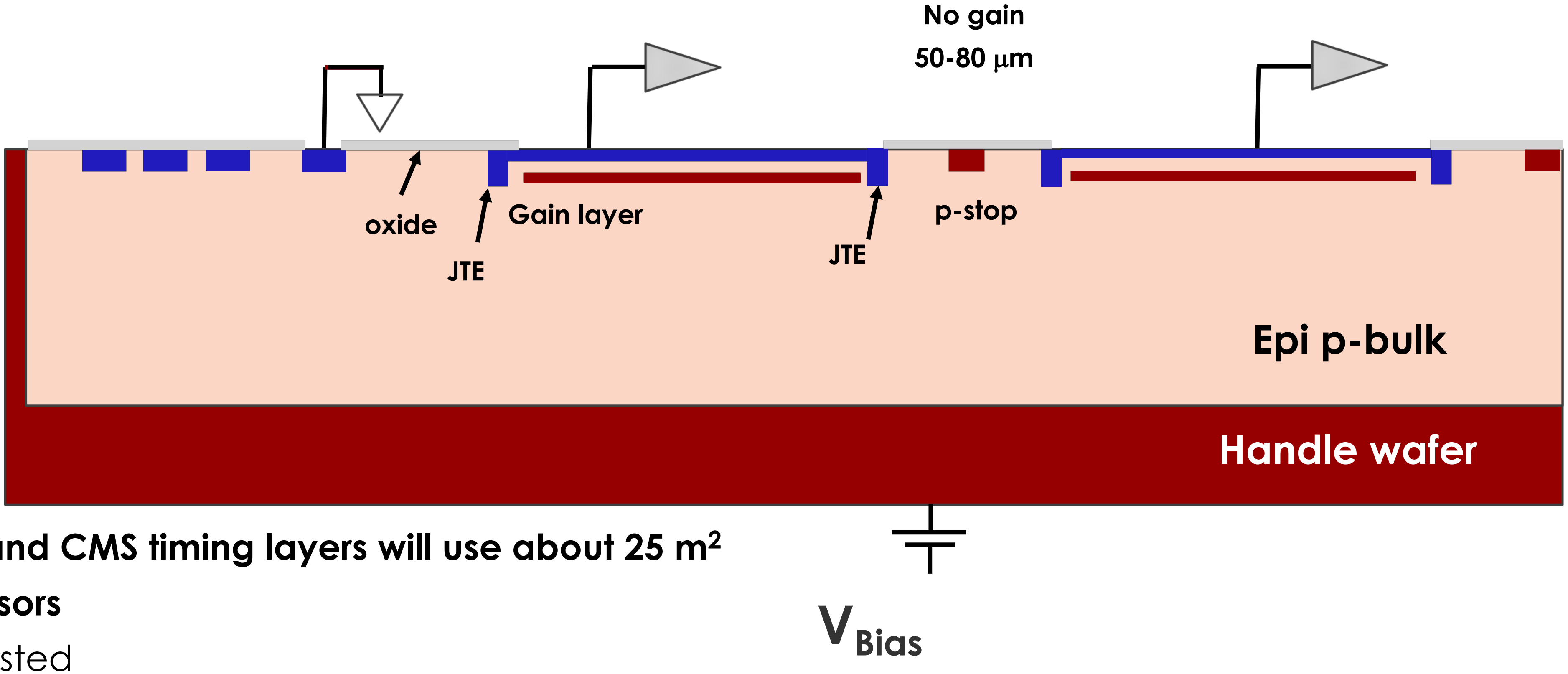
- **The ATLAS and CMS timing layers will use about 25 m^2 of UFSD sensors**
- Very well tested
- Will be used up to ~ 2 E15 n_{eq}/cm^2
- Gain ~ up to 40 when new ==> up to 20 fC
- Signal duration ~ 1 ns
- Low noise
- Rate ~ 50-100 MHz
- Excellent production uniformity

Prototype of the final CMS sensor



See D. Spitzbart, F. Filthaut
VCI2022 Wednesday morning

State-of-the-art: sensors for ATLAS and CMS



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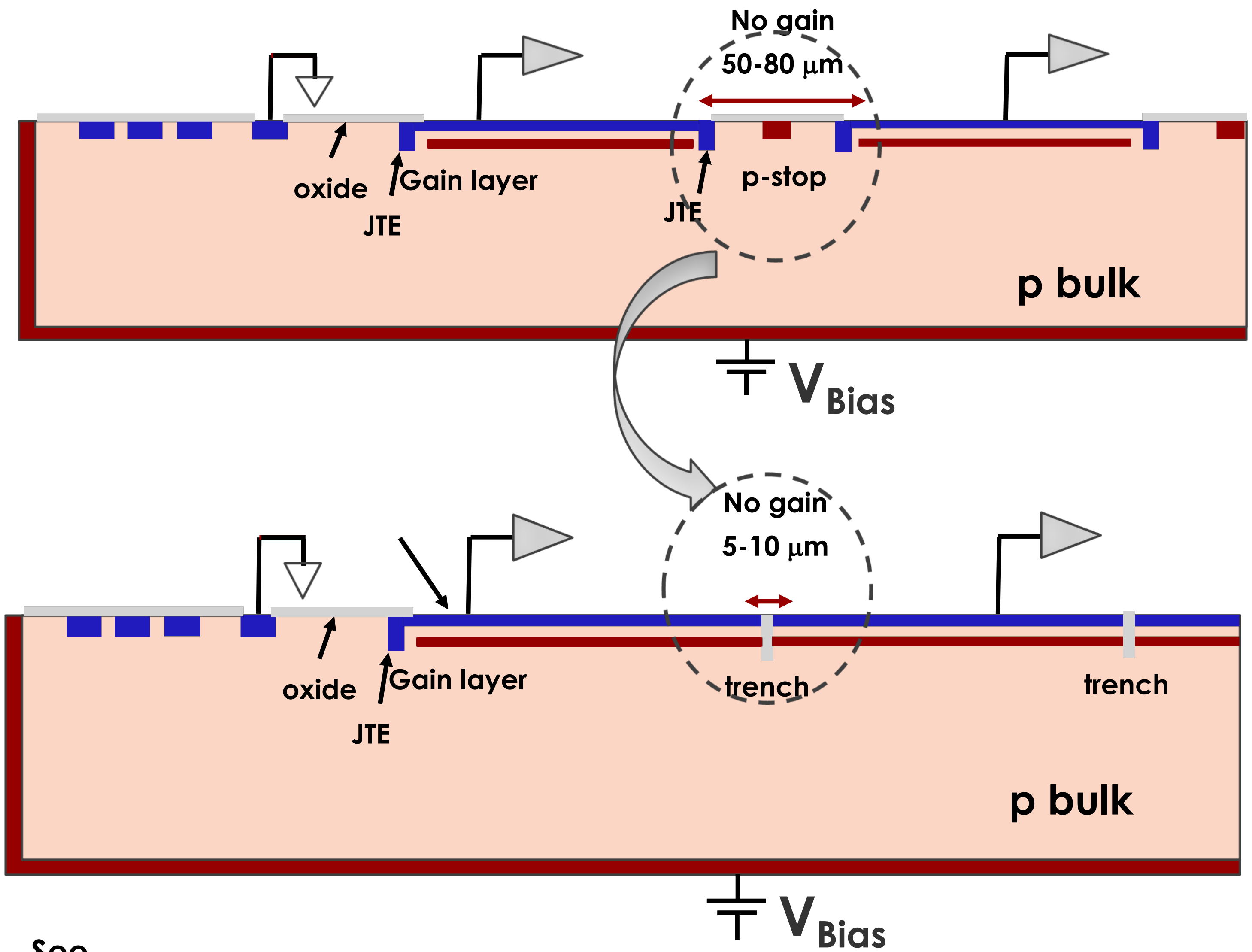
- Signal duration ~ 1 ns
- Low noise
- Rate ~ 50-100 MHz
- Excellent production uniformity

Shortcomings:

- **Large no-gain area between pads ==> not suitable for 4D tracking**
- **Intrinsic temporal resolution ~ 25-30 ps due to Landau noise**
- **Poor spatial resolution**

LGAD Trench Isolated: enabling small pixels



No-gain region ~ 50-80 µm

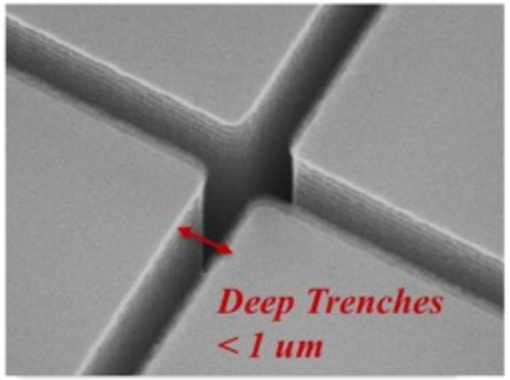
➔ cannot use for small pixels

Solution: use trenches for pad isolation

➔ No-gain region ~ 0 – 10 µm

RD50 TI-LGAD FBK production

Interpad design	Interpad distance [µm]
V1_1TR	2.7 ± 0.2
V2_1TR	6.5 ± 0.2
V3_1TR	7.9 ± 0.1
V4_1TR	10.6 ± 0.2
V2_2TR	8.9 ± 0.2
V3_2TR	10.3 ± 0.1



See

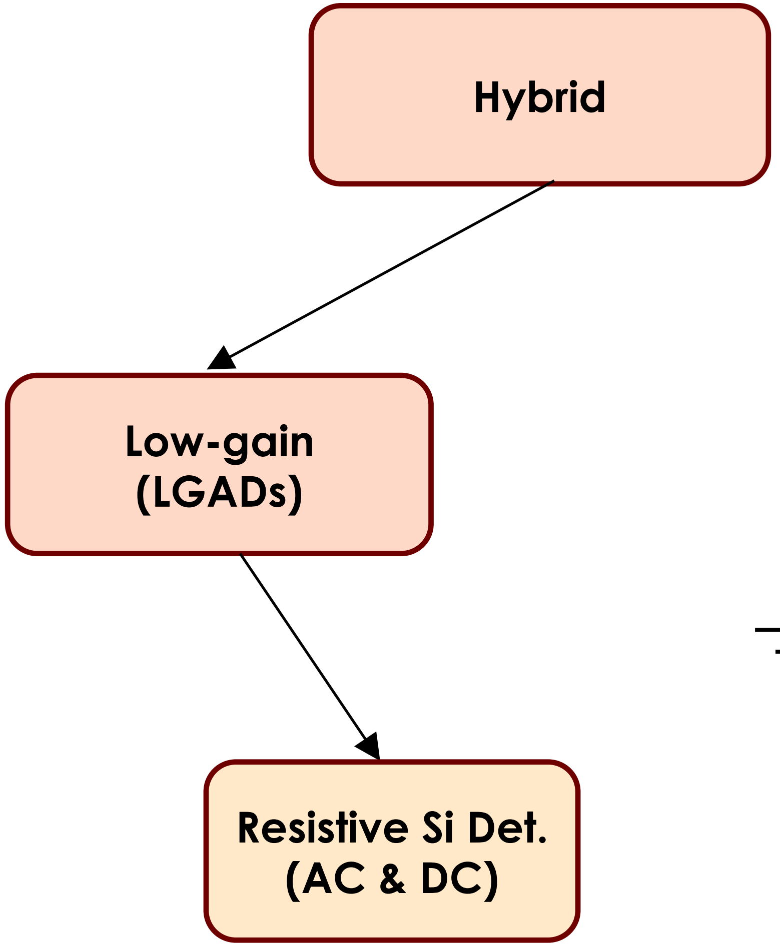
M. Senger "Time and space characterization of novel TI-LGAD", VCI2022 Friday morning

M C. Vignali "Development of LGAD at FBK", VCI2022 Friday morning

Sensors with internal gain: Resistive Silicon Detector

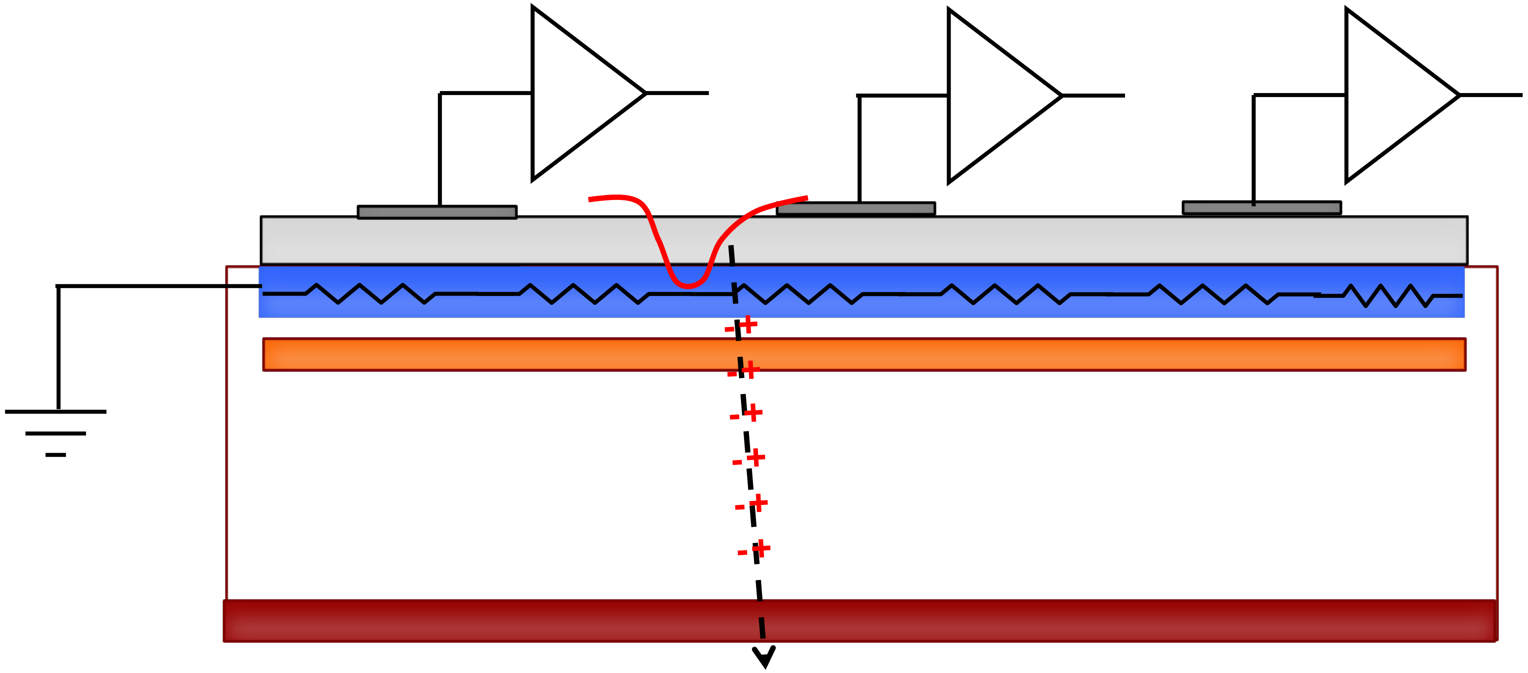
Second design innovation: resistive read-out

The signal is formed on the n+ electrode


Hybrid

Low-gain (LGADs)

Resistive Si Det. (AC & DC)

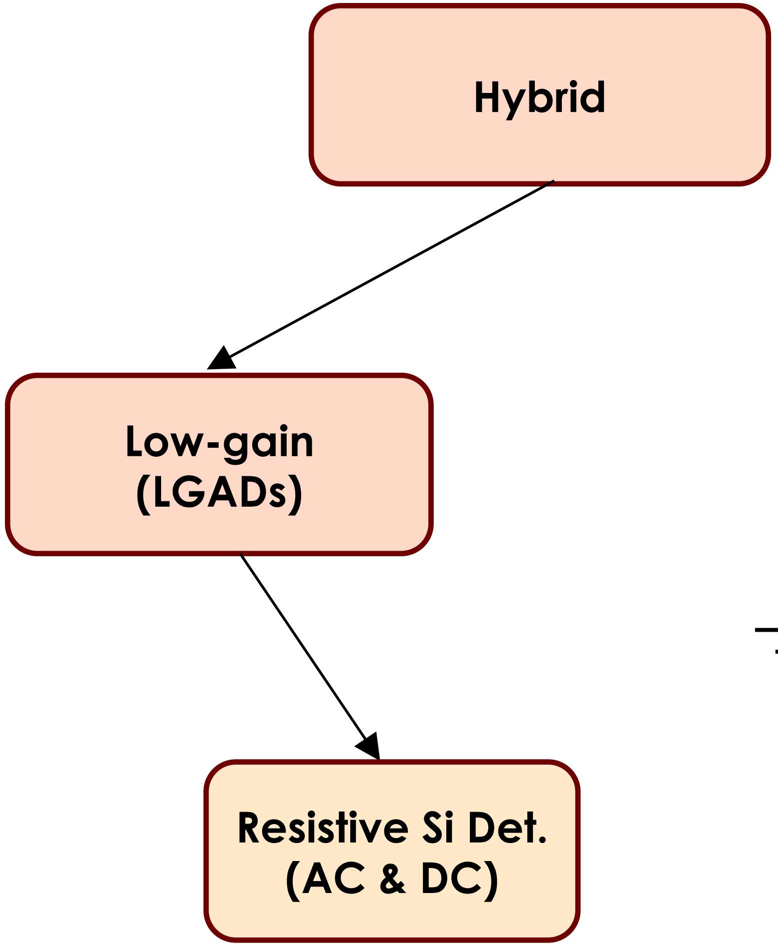


Sensors with internal gain: Resistive Silicon Detector

Second design innovation: resistive read-out

The signal is formed on the n+ electrode

The AC pads offer the smallest impedance to ground for the fast signal



Hybrid

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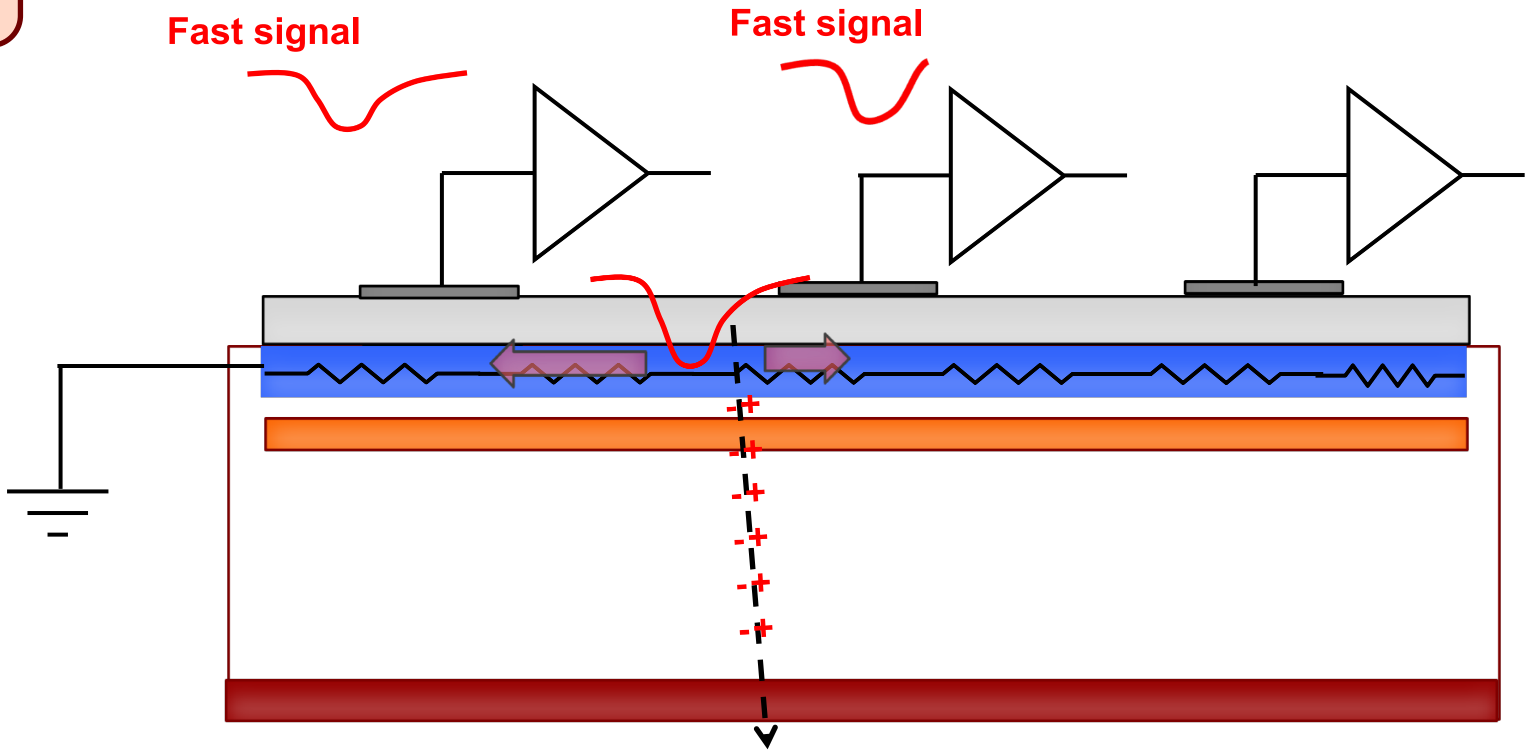

Sensors with internal gain: Resistive Silicon Detector

Second design innovation: resistive read-out

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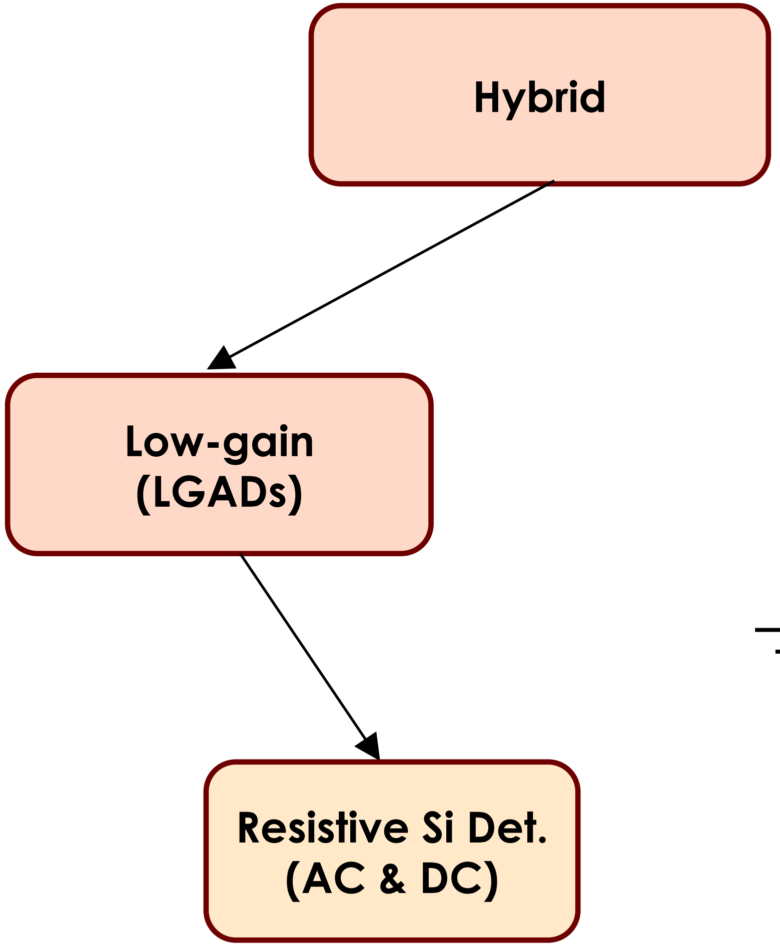
The AC pads offer the smallest impedance to ground for the fast signal

The signal discharges to ground



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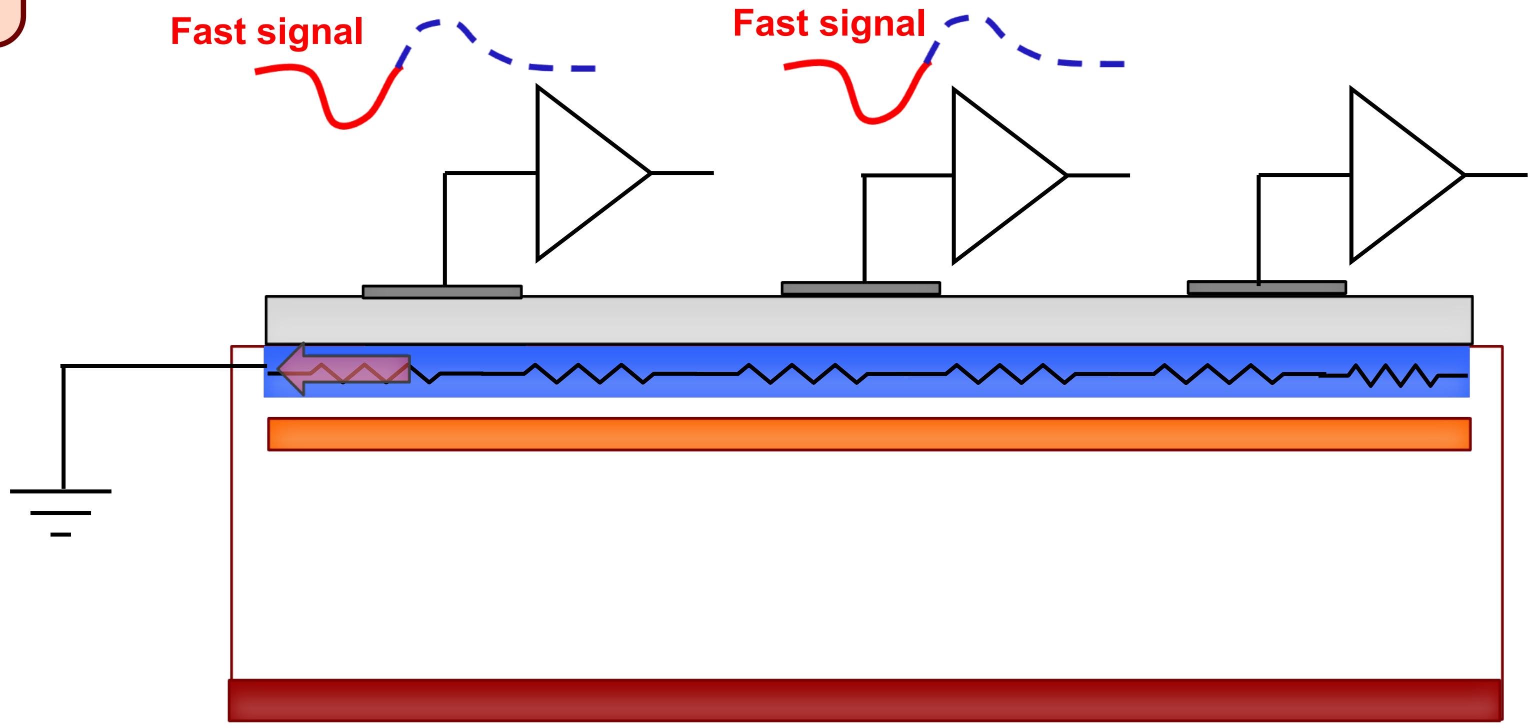
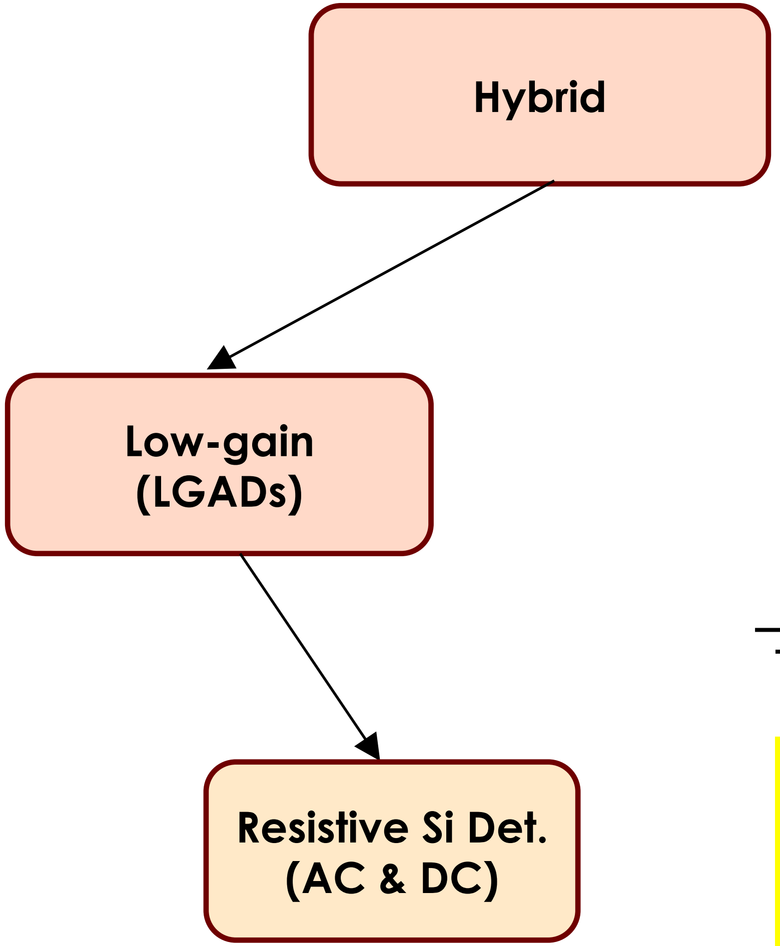


Sensors with internal gain: Resistive Silicon Detector



Hybrid

Low-gain (LGADs)

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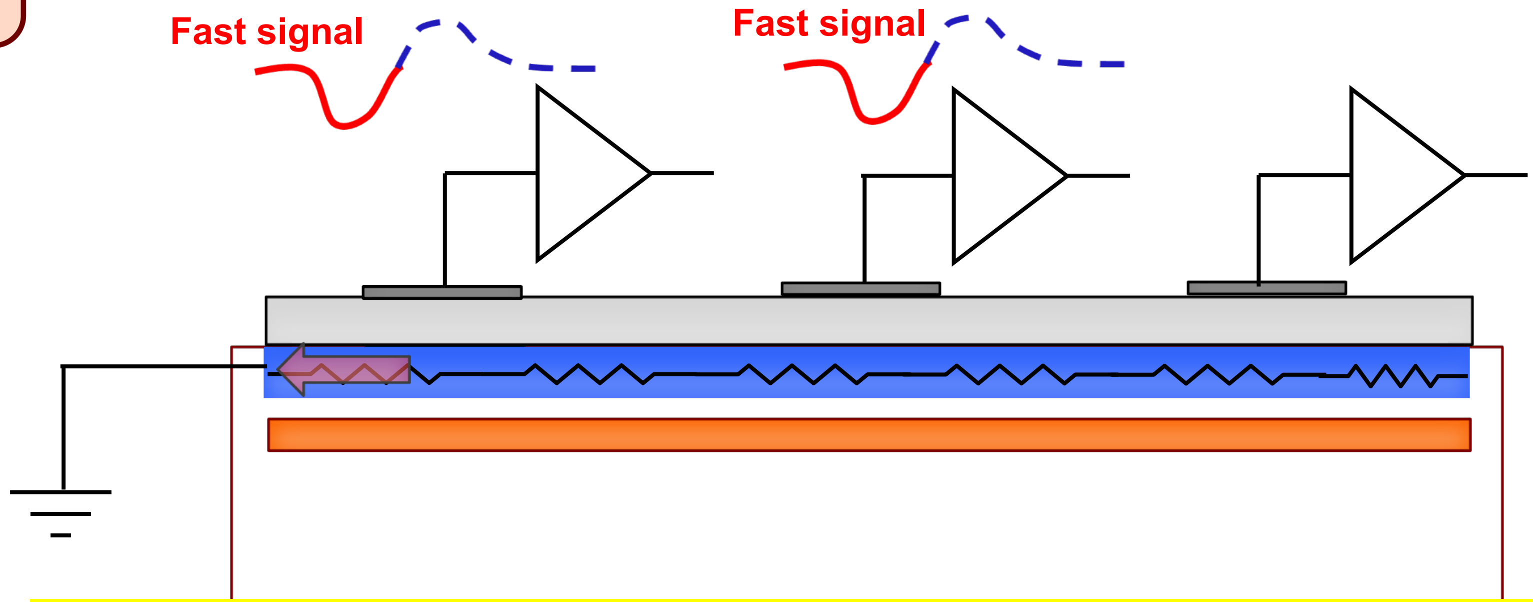
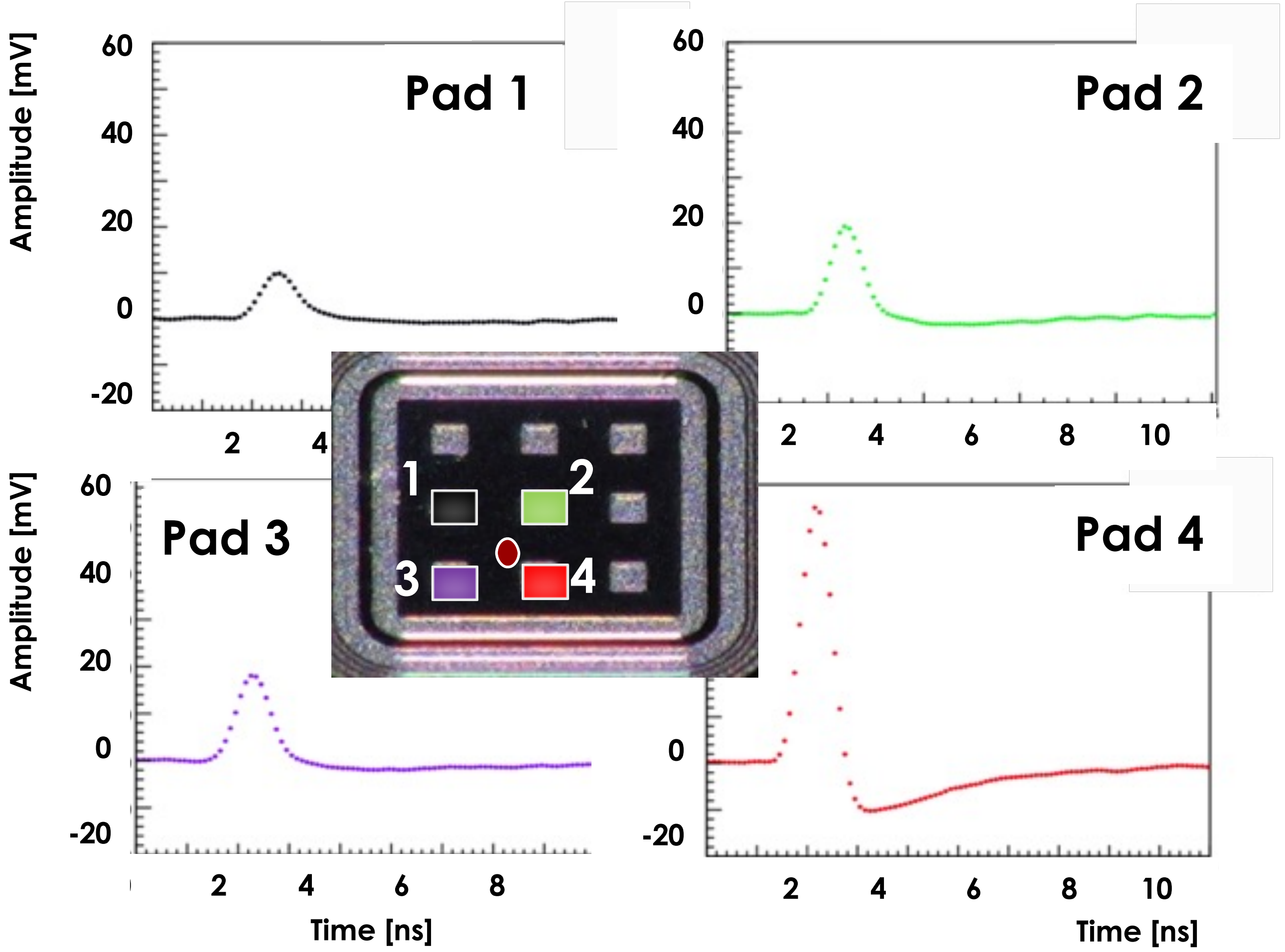


In resistive readout, the signal is naturally shared among pads (4-6) without the need of B field or floating pads
Thanks to the internal gain, full efficient even with sharing

Resistive Silicon detector: example of signal sharing

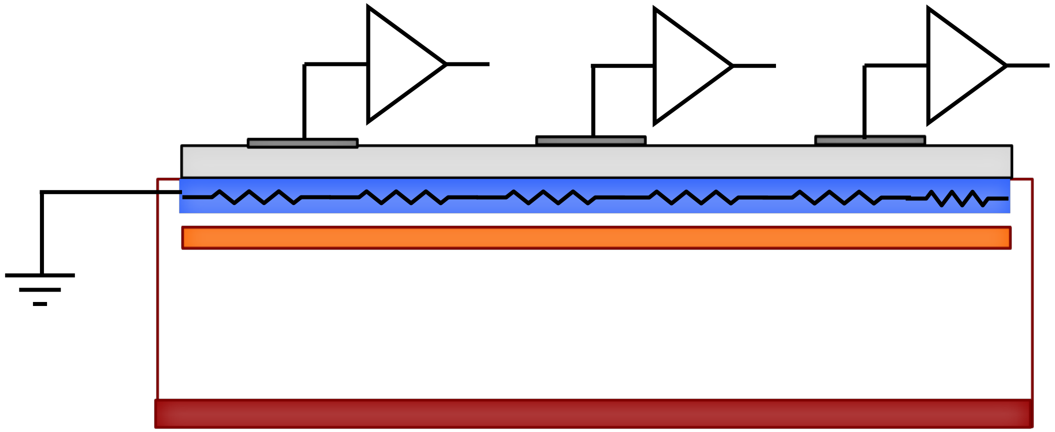
50-mm thick FBK RSD, Gain ~ 20



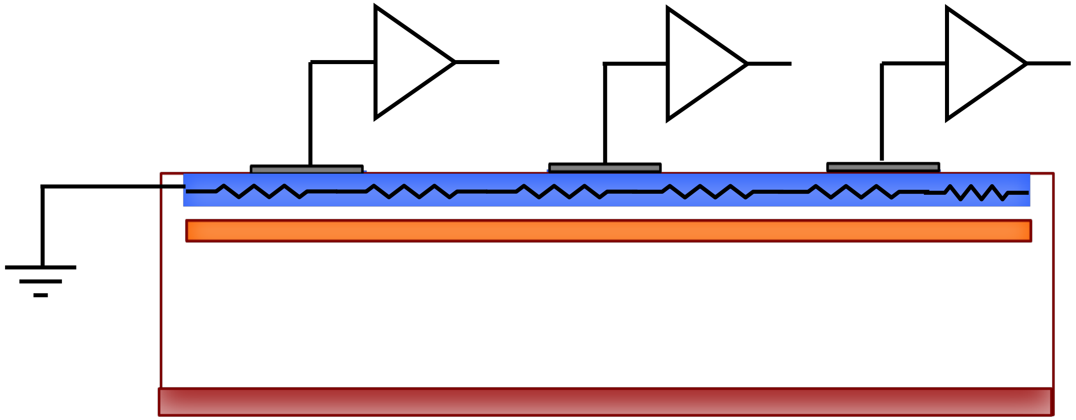
The laser is shot at the position of the red dot: the signal is seen in 4 pads

AC- and DC- resistive silicon sensor

AC-RSD



DC-RSD



Presently produced by FBK, HPK, BNL

Possible choice for TOF in EIC

Evolution of the AC- design, to limit signal spread and baseline fluctuations

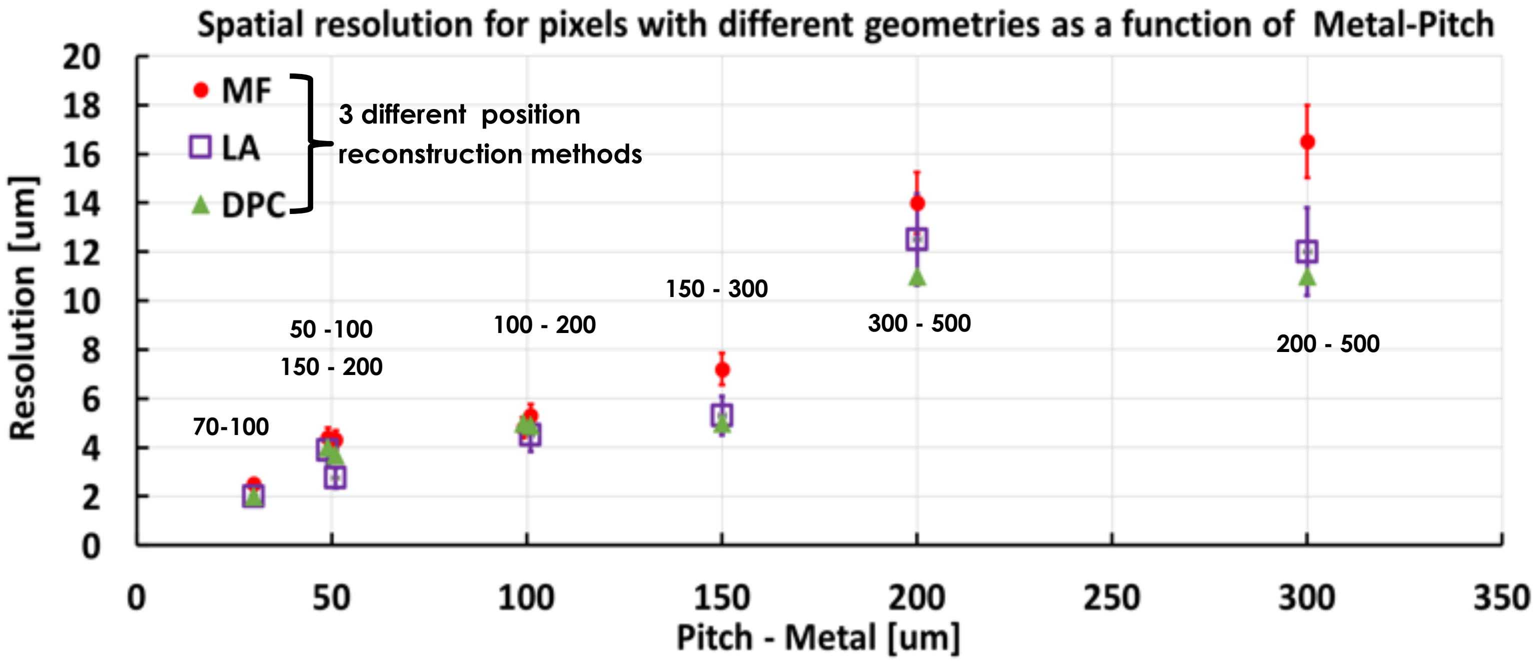
See

T. Ullrich "Requirements and R&D for detectors at the future Electron-Ion-Collider (EIC), VC2022, Monday morning

L. Menzio "DC-coupled resistive silicon detectors for 4D tracking", VCI2022 Recorded

J. Ott "Investigation of signal characteristics and charge sharing in AC-LGADs", VCI2022, Recorded

Spatial precision of resistive read-out



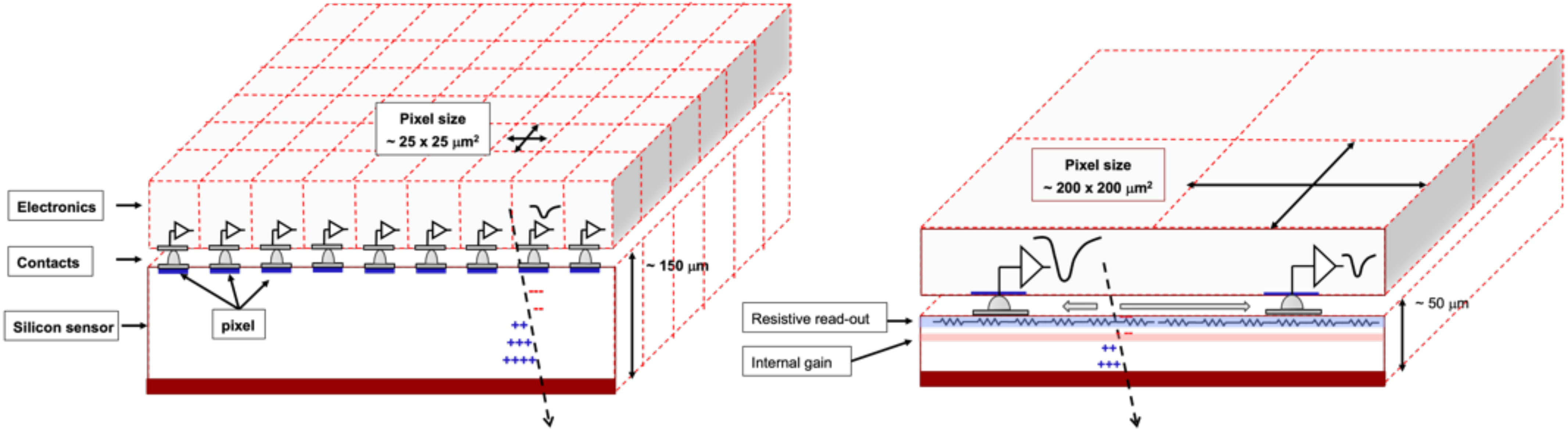
RSDs reach a spatial resolution that is about 5% of the inter-pad distance

➔ ~ 5 μm resolution with 150 μm pitch

RSDs have the “usual” UFSD temporal resolution of 30-40 ps

See F. Siviero ”Spatial resolution of RSD pad arrays”, VCI2022 Friday morning

Why is resistive read-out relevant?



Traditional sensors **Resistive read-out**

- It reduces the number of pixels by a large factor (~ 50)

  An RSD sensor with a 200 µm pitch has the same spatial precision of a traditional sensor with 25 µm pitch
- The pixel size is determined by occupancy
- Large area for the electronics, much more power per pixel available
- Low material budget

Radiation hardness of the gain implant

Irradiation decreases the active doping in the gain layer

Acceptor removal,
Gain layer deactivation

$$N(\emptyset) = N(0) * e^{-c\emptyset}$$

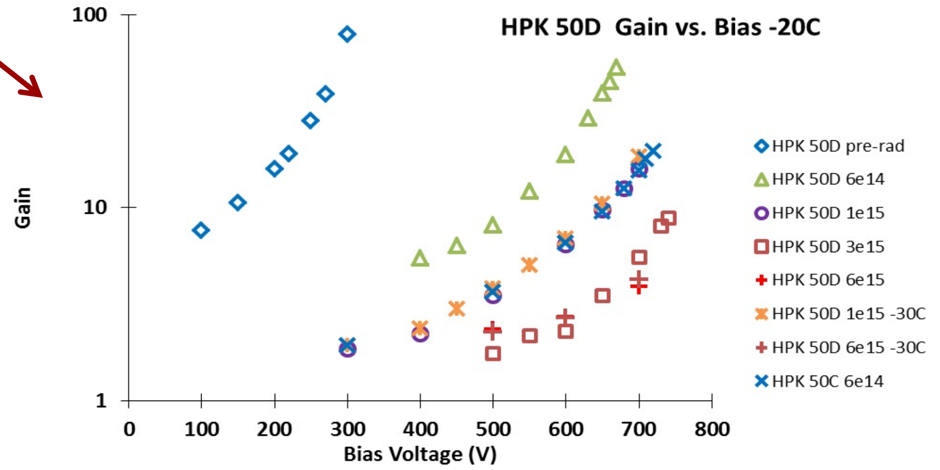
Concluded R&D

Defect Engineering of the gain implant

- Carbon co-implantation mitigates the gain loss after irradiation

Modification of the gain implant profile

- Narrower Boron doping profiles with high concentration peak are less prone to be inactivated



Future R&D

Compensation: gain implant obtain as difference of p- and n- doping

- Concurrent acceptor and donor removal might limit the disappearance of effective doping

Carbon shield:

- A deep implant of carbon might prevent defects to reach the gain implant

See V. Sola "Silicon sensors for extreme fluences", VCI2022 Thursday afternoon

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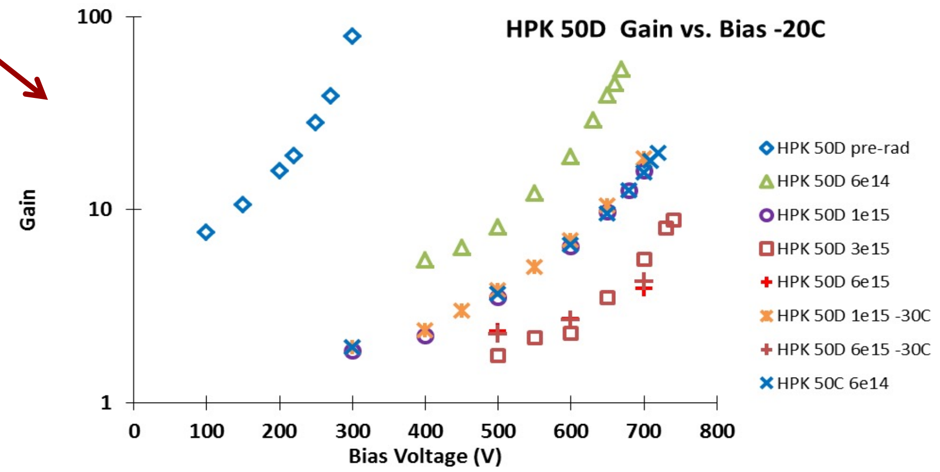

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Compensation: gain implant obtain as difference of p- and n- doping

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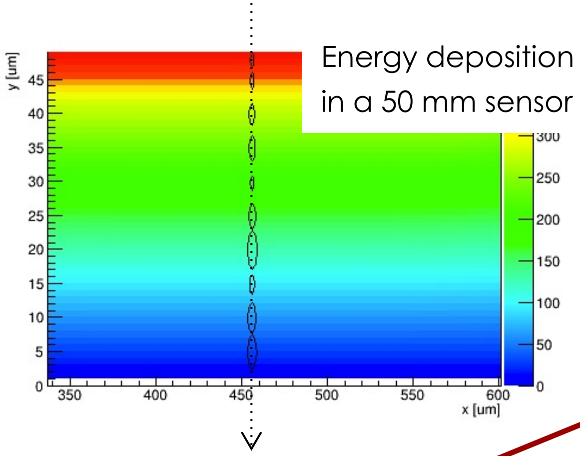
Presently, LGAD works up to about 10^{15} n_{eq}/cm^2
Future R&D might push this limit higher

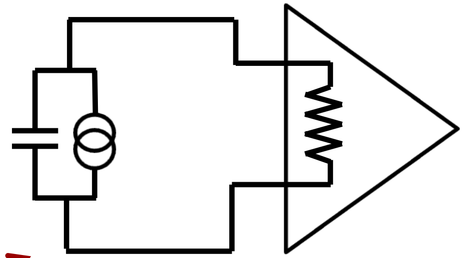
See V. Sola "Silicon sensors for extreme fluences", VCI2022 Thursday afternoon

Brief considerations about electronics: pre-amp design

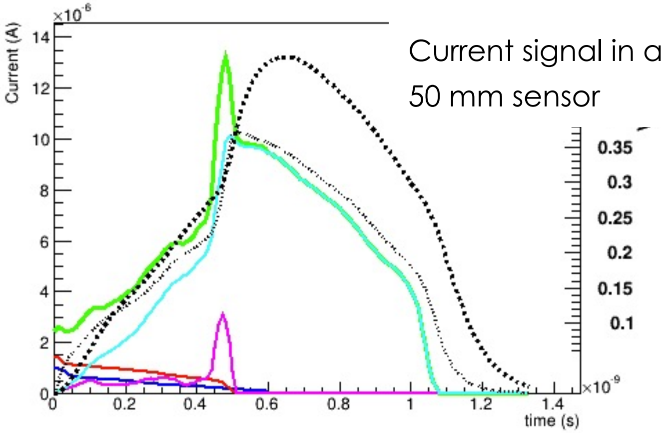


Energy deposition in a 50 mm sensor

Current Amplifier

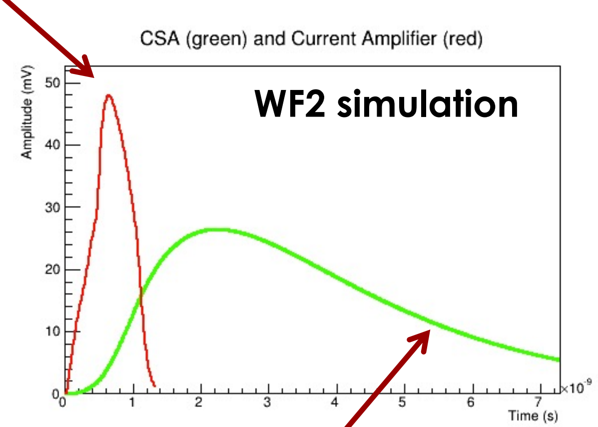


- Fast slew rate
- Higher noise
- Sensitive to Landau bumps

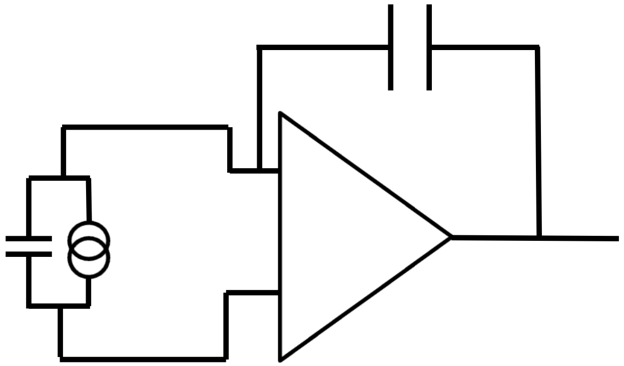


Current signal in a 50 mm sensor

WF2 simulation



Charge Sensitive Amplifier



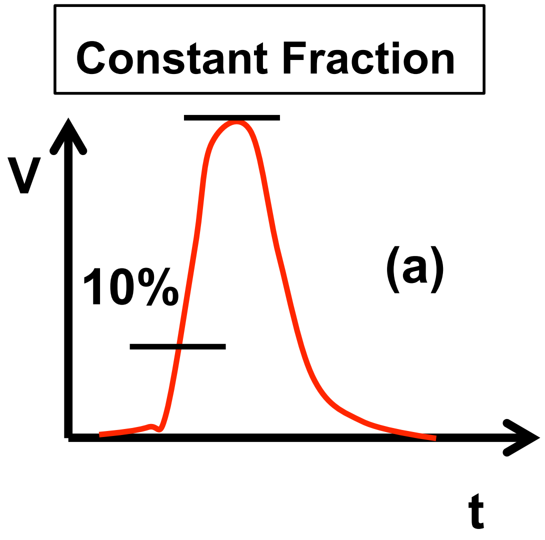
- Slower slew rate
- Quieter
- Integration helps the signal smoothing

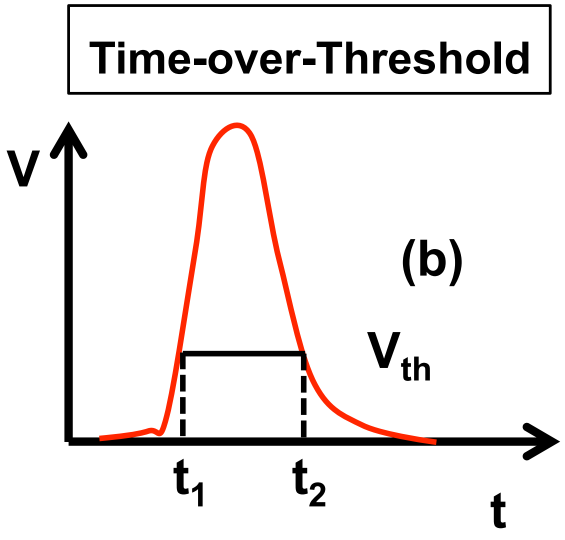
NOT MY TALK!!

Experts in the room…

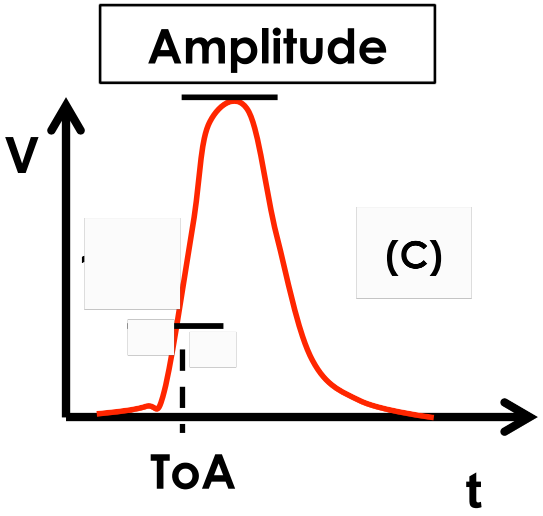
Brief considerations about electronics: Time walk corrections

On paper both seem feasible,
in practice
ToT is much easier to implement





My favorite: **ToA and Amplitude**
➔ The tail of the signal is prone to changes due to charge trapping



Brief considerations about electronics: power

Name	Sensor	node	Pixel size	Temporal precision [ps]	Power [W/cm^2]
ETROC	LGAD	65	1.3 x 1.3 mm^2	~ 40	0.3
ALTIROC	LGAD	130	1.3 x 1.3 mm^2	~ 40	0.4
TDCpic	PiN	130	300 x 300 μm^2	~ 120	0.45 (matrix) + 2 (periphery
TIMEPIX4	PIN, 3D	65	55 x 55 μm^2	~ 200	0.8
TimeSpot1	3D	28	55 x 55 μm^2	~ 30 ps	5-10
FASTPIX	monolithic	180	20 x 20 μm^2	~ 130	40
miniCACTUS	monolithic	150	0.5 x 1 mm^2	~ 90	0.15 – 0.3
MonPicoAD	monolithic	130 SiGe	25 x 25 μm^2	~ 36	40
Monolith	LGAD monolithic	130 SiGe	25 x 25 μm^2	~ 25	40

Brief considerations about electronics: power

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FASTPIX	monolithic	180	20 x 20 μm²	~ 130	40
miniCACTUS	monolithic	15			
MonPicoAD	monolithic	130 SiGe	25 x 25 μm	20	40
Monolith	LGAD monolithic	130 SiGe	25 x 25 μm²	~ 25	40

For small pixels, presently the power consumption is too high
==> need a breakthrough

Present and future

Under construction:

The two large timing layers (25 m^2) of the ATLAS-CMS collaboration

1.3 x 1.3 mm^2 pads UFSD, ALTIROC & ETIROC ASICs, 200-300 mW/cm^2, resolution ~ 45 ps/hit

Advanced prototypes:

Timepix4 soon to be coupled with TI-LGAD

TIMESPOT1 with trenched detectors

Demonstrators:

FASTPIX (CMOS), MonPicoAD (SiGe), miniCACTUS (CMOS), Resistive readout (large pixels, excellent spatial and temporal resolution)

New kids on the block:

Monolith (SiGe+LGAD)

Wrap-up

4D tracking is a very young booming field. Hybrid and monolithic approaches are yielding very good results

The paste of innovation is very fast (especially considering that silicon sensors is a very mature field)

Several demonstrators with temporal precision of about 30 ps are available. Not unreasonable to expect 10-15 ps in the next few years.

In my view, the most difficult part is in the design of the electronics.

Temporal resolution degrades very quickly if the whole system is not “perfect”

It is very difficult to combine very good position precision, <5 μm, with good temporal resolution using the “single-pixel design”. Charge sharing might be the key to solve this problem.

It takes a village

The path to 4D tracking is complex, with many different communities working on various aspects. Their contributions are of fundamental importance to reach the end goal.

Acknowledgement

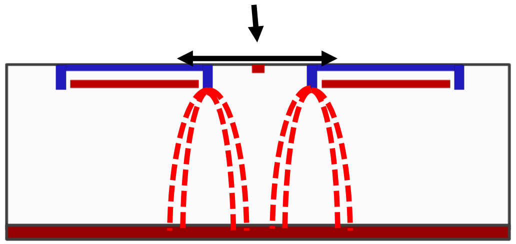
We kindly acknowledge the following funding agencies, collaborations:

- RD50 collaboration
- INFN - Gruppo V, UFSD and RSD projects
- INFN – FBK agreement on sensor production (convenzione INFN-FBK)
- Dipartimenti di Eccellenza, Univ. of Torino (ex L. 232/2016, art. 1, cc. 314, 337)
- Ministero della Ricerca, Italia , PRIN 2017, progetto 2017L2XKTJ – 4DinSiDe
- Ministero della Ricerca, Italia, FARE, R165xr8frt_fare

Collection of extra sides

UFSD Summary: more gaining and more sharing

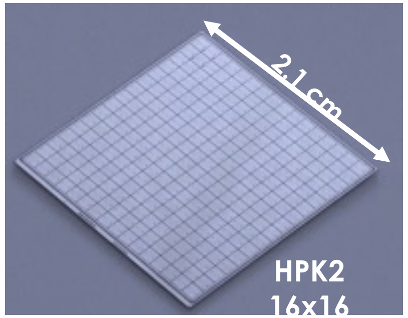
No gain area ~ 50 um



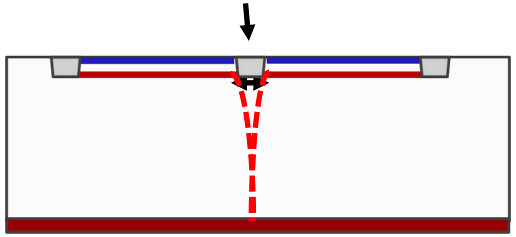
JTE + p-stop design

JTE/p-stop UFSD

- CMS && ATLAS choice
- Signal in a single pixel
- Not 100% fill factor
- Very well tested
- High Occupancy OK
- Rate ~ 50-100 MHz
- Rad hardness ~ 2-3E15 n/cm2



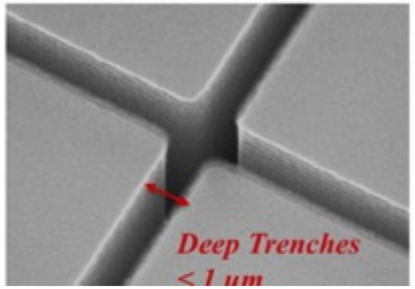
No gain area ~ 5 um

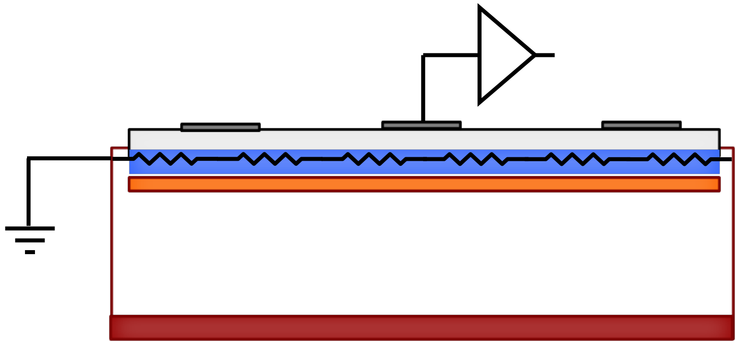


Trench-isolated design

UFSD evolution: use trenches

- Signal in a single pixel
- Almost 100% fill factor
- Temporal resolution (50 μm) : 35-40 ps
- High Occupancy OK
- Rate ~ 50-100 MHz
- Rad hardness: to be studied

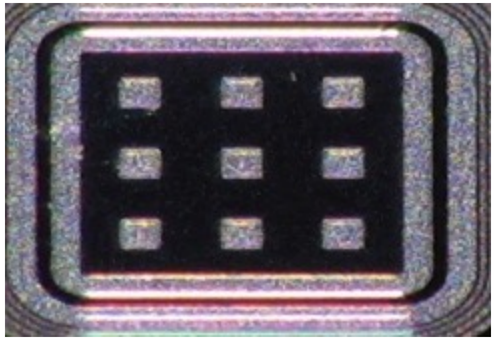




RSD -- AC-LGAD

RSD evolution: resistive readout

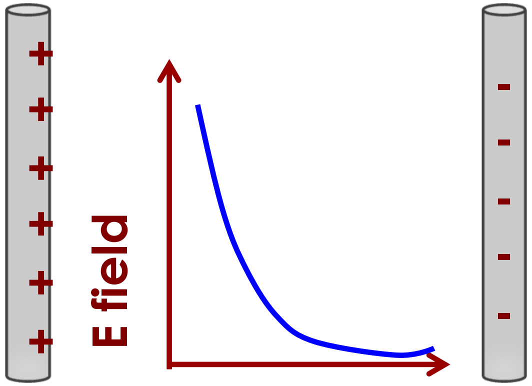
- Signal in many pixels
- 100% fill factor
- Excellent position resolution:
  ~ 5 μm with large pixels
- Temporal resolution (50 μm) : 35-40 ps
- Rate ~ 10-50 MHz
- Rad hardness: to be studied



3D sensors for timing applications

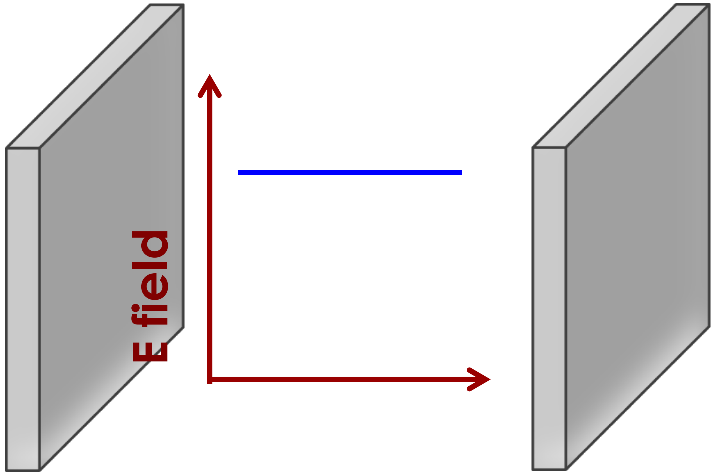
3D sensors for timing have the same underlying features of standard 3D detectors: very good radiation resistance

The design in insensitive to non-uniform charge deposition



CNM-Ljubliana studies: use column geometry

In their "column" geometry, they cannot, the Efield is not uniform enough



Timespot approach

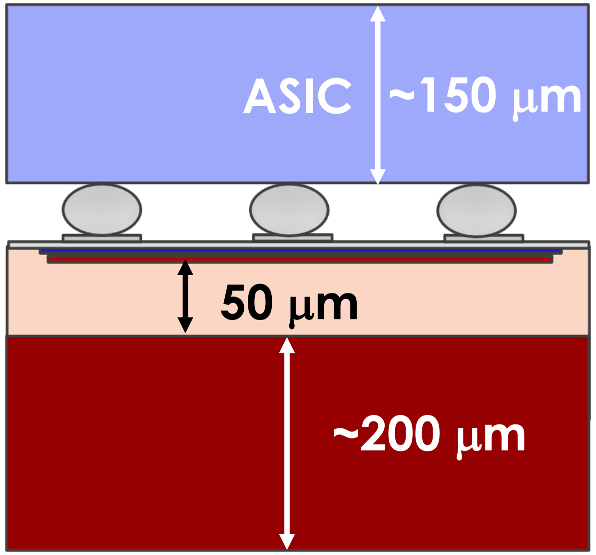
using trenches gives a parallel plate geometry,
and a weighting field ~ 1/d

Reduced material budget

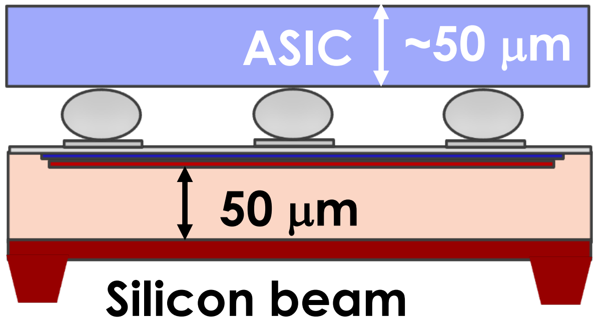
The active thickness of UFSD sensor is rather small ~ 50 um.

In the present prototypes, the active part is attached to a thick “handle wafer”

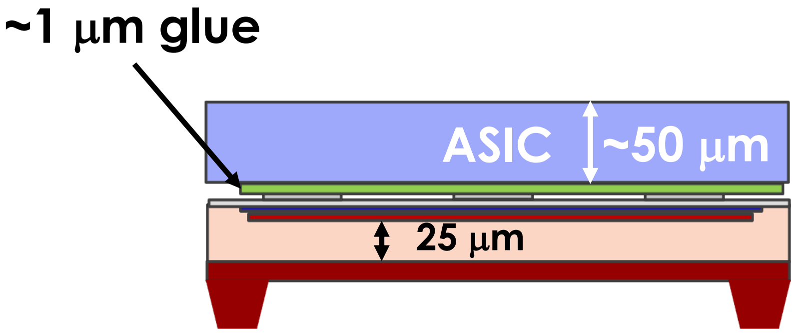
There is a clear path leading to < 100 μm material:



Present design: no material budget optimization



- Thinned handle wafer:
  500 um ➔ 10-20 um

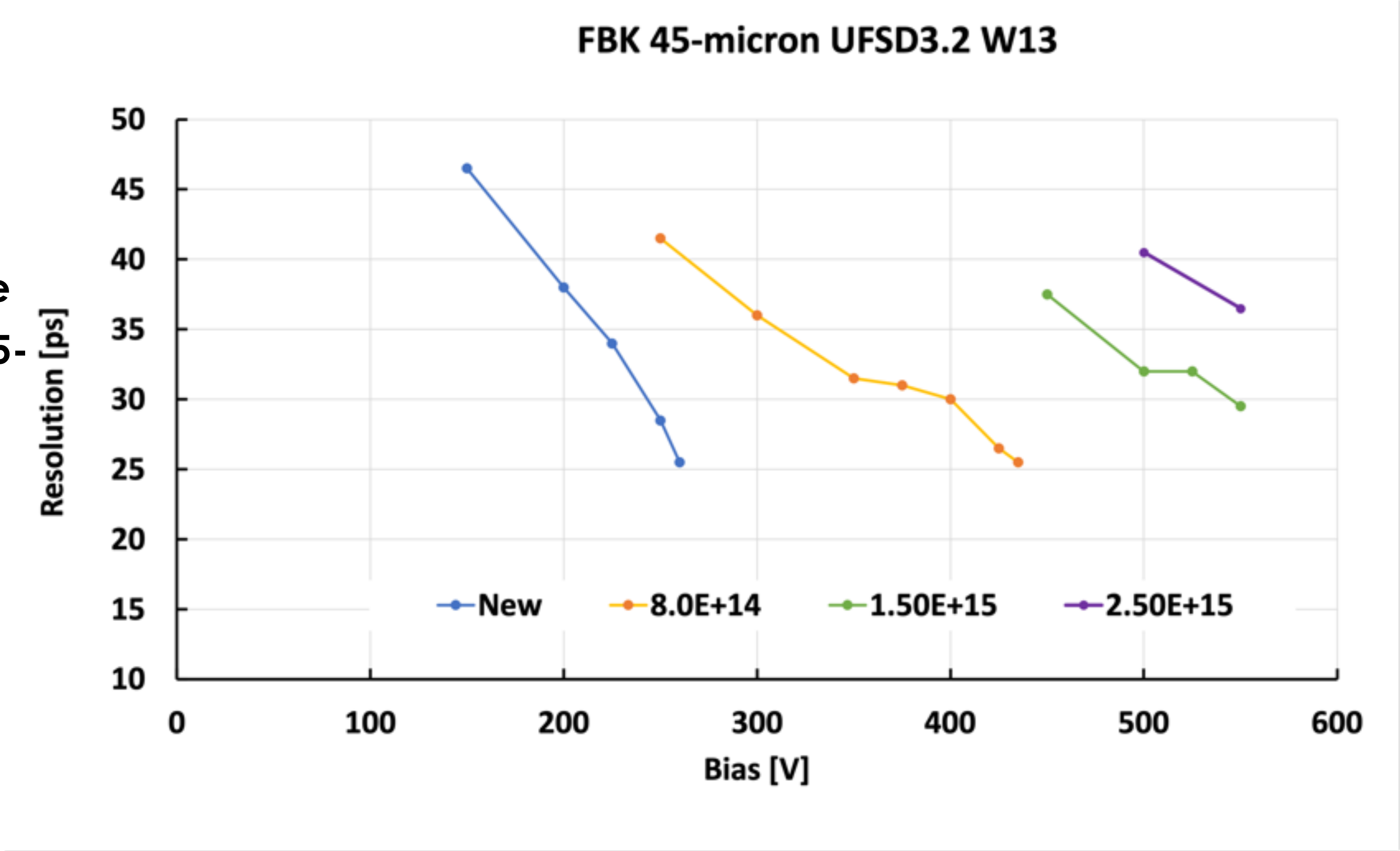


- Thinned handle wafer:
  500 um ➔ 10-20 um
- Thinned active area:
  50 um ➔ 25 um
  50 ps ➔ 25 ps

Nicolo Cartiglia, INFN, Torino, VCI2022, 25/02/22

UFSD radiation hardness

Evolution with radiation of the biasing working point for a 45-micron thick LGAD with a carbonated gain layer

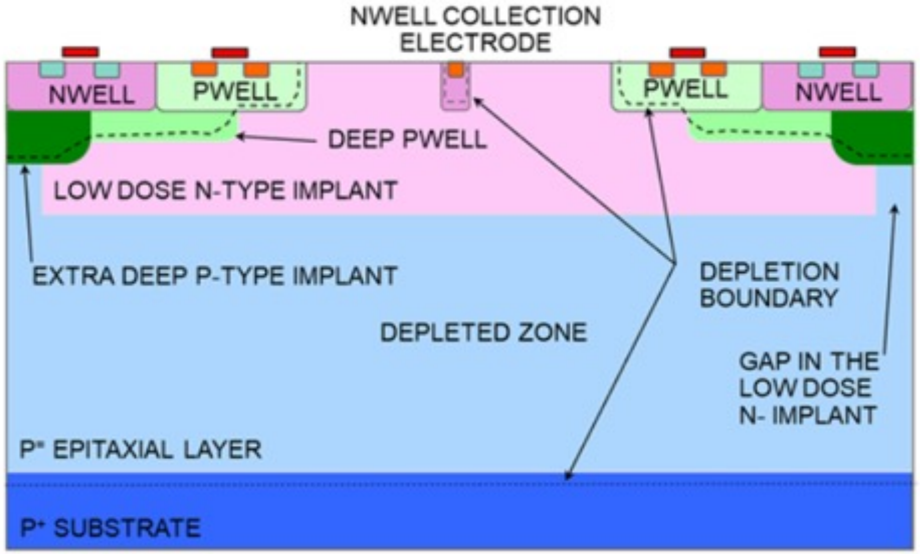


Present LGAD design assures better than 40 ps up to 2.5E15 n_{eq}/cm^2

FASTPIX approach

"In the ATTRACT project FASTPIX we investigate monolithic pixel sensors with small collection electrodes in CMOS technologies for fast signal collection and precise timing in the sub-nanosecond range."

- Evolution of the process used for MALTA: speeding up the electron lateral drift
- Small pixel pitches (~10 μm)
- Very low electrode capacitance (< 1fF)
- Expected jitter (electronics): 20ps @ Q_{in} =1000 e^-
- Estimated resolution: sub-ns (a few hundred ps)



T. Kugathasan et al., Nucl. Inst. Meth. A Vol. 979, Nov. 2020

Present status of ATLAS-CMS timing layer

UFSD are available from many vendors: HPK, FBK, CNM, BNL

and several more are coming on line: Micron, NDL (China), IHEP (China)

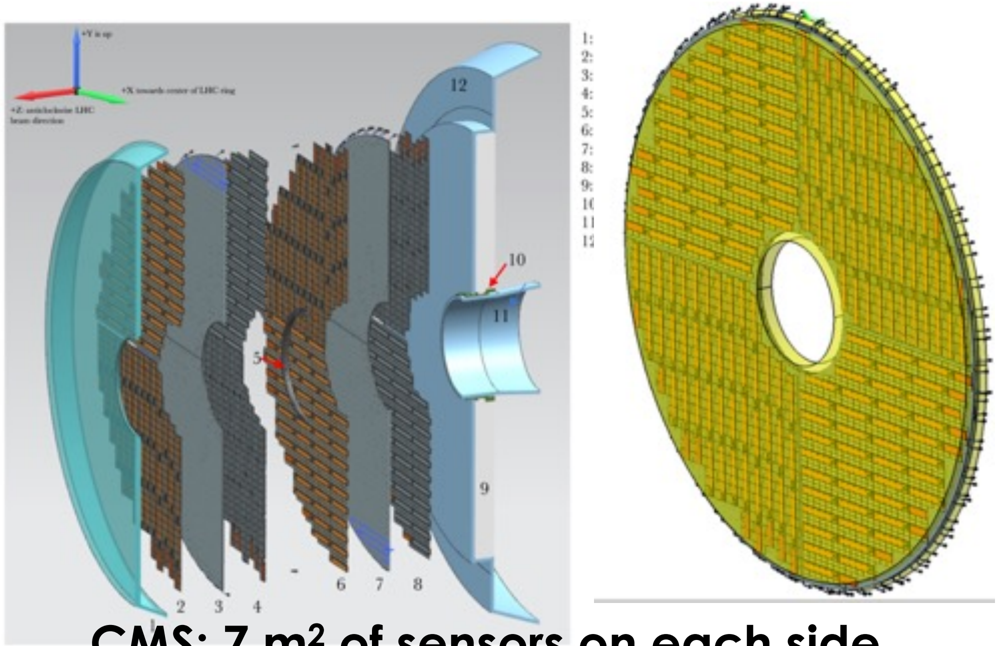
ATLAS and CMS are planning to use ~ 20-30 m^2

➔ Mature technology

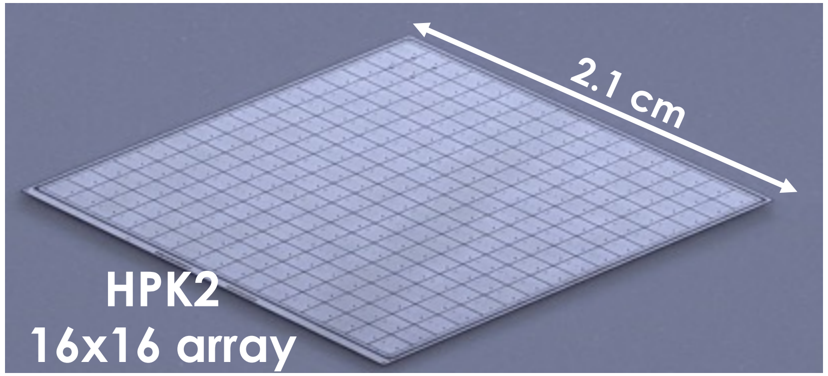
Installation: 2023-2025

CMS: 2 layers, covering the full endcap 1.6 < eta < 3

ATLAS: 2 ½ - 3 layers, covering high rapidity 2.5 < eta < 4



CMS: 7 m^2 of sensors on each side



Read-out chips for UFSDs

In the past 3-4 years, the ATLAS and CMS collaborations poured a considerable amount of resources into designing the read-out chips for their respective timing layers.

ATLAS: ALTIROC, TSMC 130 nm, 15x15 pads,
CMS: ETROC, CMOS 65 nm, 16x16 pads

For both: input load about 4 pF, jitter ~ 20ps at 10fC of input charge
Power:

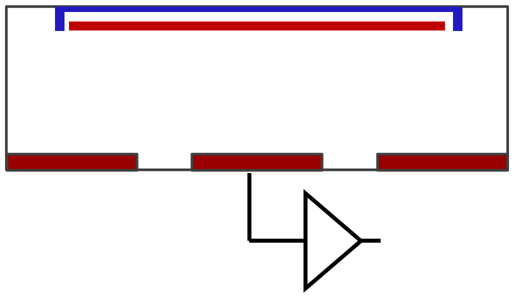
ALTIROC ~ 3.5 mW/ch,
ETROC~ 3 mW/ch

} **2-300 mW/cm^2**

As a comparison, the **RD53 readout chip for pixel detectors** for tracking (i.e. no timing) at the HL-LHC with 50 x 50 um2 and 25 x 100 um^2 feature sizes is estimated to have a power density of **about 1 W / cm^2**

A timing layer with large pixels needs less power than a layer of small traditional pixels

I-LGAD: a new desgin for 100% fill factor



i-LGAD

- **p-side segmentation**
- **Signal in a single pixel**
- **100% fill factor**
- **Thin i-LGAD with single side processing under development (using trenches)**

=> done with TCAD simulation, run starting in spring 2021 @ CNM

- **High Occupancy OK**
- **Rate ~ 50-100 MHz**
- **Rad hardness ~ 2-3E15 n/cm2**

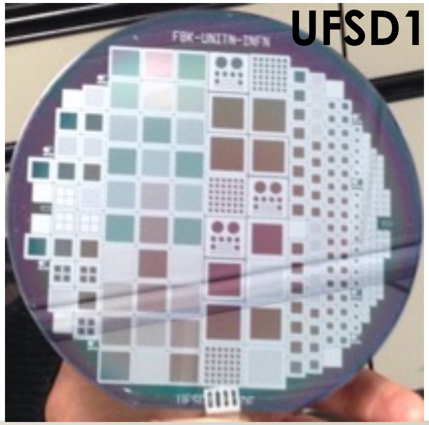
The UFSD project: brief history

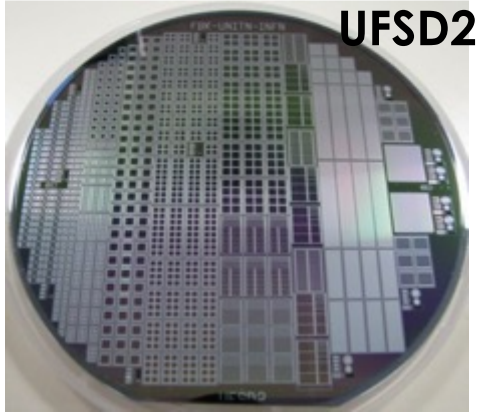
Aim: develop sensors with excellent temporal and spatial resolutions via a series of productions and design refinements

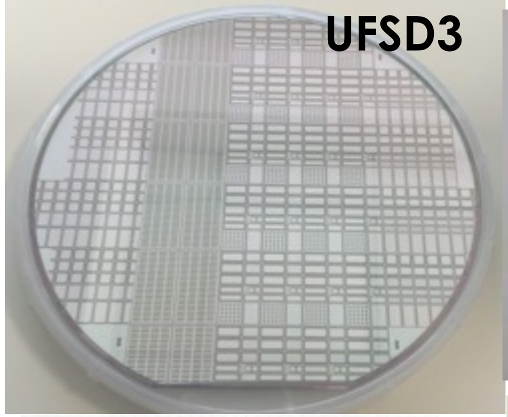
Long term R&D, Not for a specific experiments

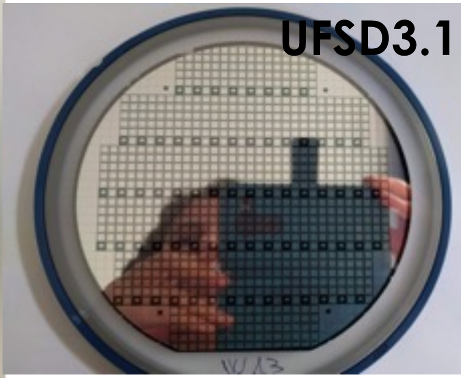
1. **2016**: UFSD1 First 300 µm thick LGAD (FBK 6" wafer)
2. **2017**: UFSD2 First 50 µm thick LGAD (FBK 6" wafer)
Gain layer doping: Boron, Gallium, Boron + Carbon,
3. **Fall 2018:** UFSD3 50 µm LGAD (FBK 6" wafer), produced with the stepper (many Carbon levels, studies of interpad design)
4. **June 2019:** UFSD3.1 50 µm LGAD (internal FBK) interpad design.
5. **June 2019** RSD1 Resistive AC-LGAD (FBK 6" wafer
6. **June 2020:** UFSD3.2 25, 35, 45, and 55 µm LGAD, carbon studies, deep, shallow gain implant (FBK 6" wafer
7. **Q1/2021: UFSD3.3** (FBK 6" wafer)
8. **Q1/2021: Trench-Isolated** (FBK 6" wafer)
9. **Q2/2021: RSD2** (FBK 6" wafer)
10. **Q2/2021: ExFlux** -> optimized for extreme fluence

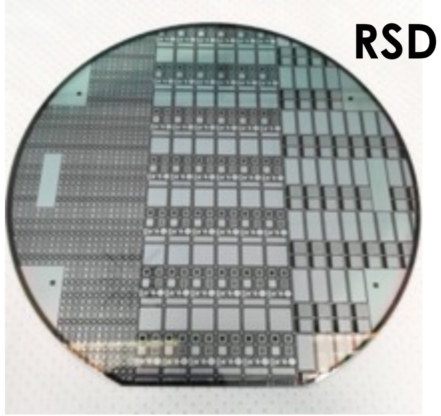
Project fully funded for 3 more years

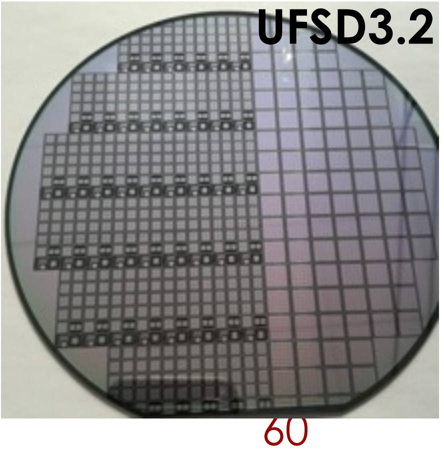






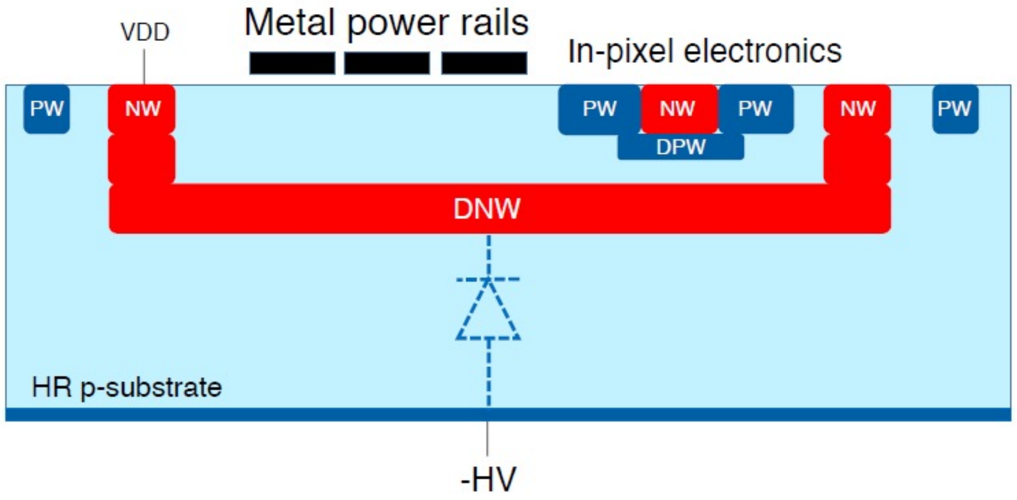






HV-CMOS approach: CACTUS

- CMOS LFoundry 150 nm
- Deep nwell collection diode, fully depleted
- FE electronics inside the pixel
- Fast and uniform charge collection
- Substrate thickness: 200um
- Pixel size: 0.5 – 1 mm^2
- Pixel capacitance: 1 – 1.5 pF
- Res: 278 ps at 1.7 MIPS, 303 ps at 1 MIP
- Noise can be reduced by moving the readout electronics outside the pixels: capacitance reduction



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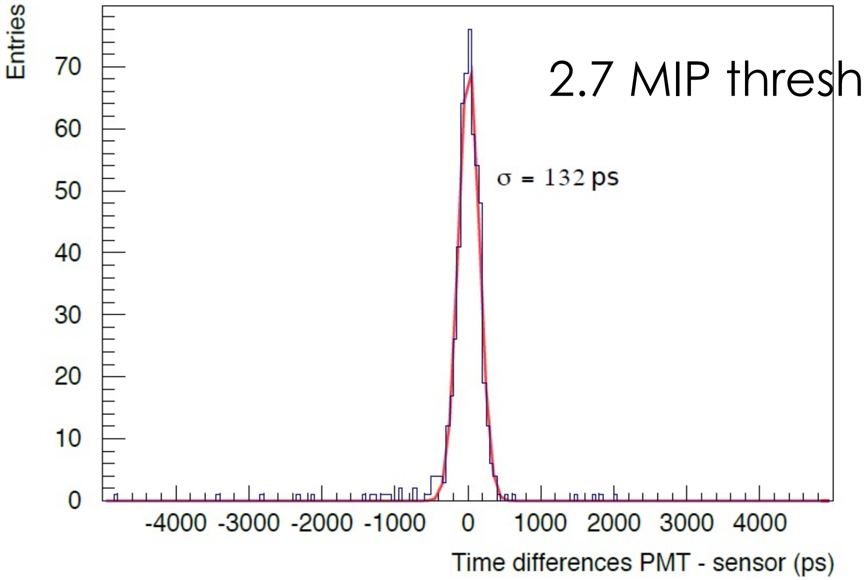


2.7 MIP threshold

Y. Degerli et al., 2020 JINST 15 P06011

Setting the stage: the ECFA report - II

ECFA has also identified key developments in the electronics to achieve 4D tracking

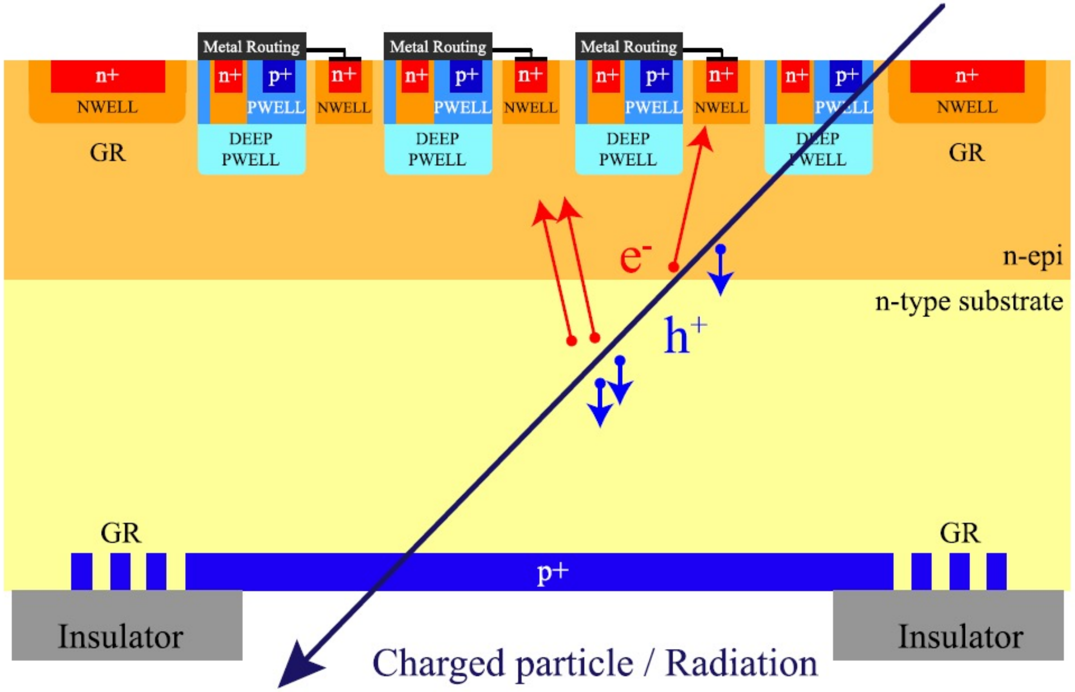
Electronics for 4D-tracking:

- **High-performance sampling (TDC, ADC):**
  High-4D resolution requires a solution to the difficult noise-speed-resolution trade-offs in advanced technologies with low supply voltage and high transistor density;

- **High-precision timing distribution:**
  Distribution of precise frequency and time references remains vital for all readout-systems. The performance of these systems will be pushed to unprecedented levels by 4D sensors, for which they are a limiting factor. There are no ready-made solutions at hand, and the challenge is even bigger in radiation environments;

ARCADIA

- MAPS 110-nm CMOS
- Fully depleted substrate: charge collection by drift
- Process validated on 100 – 300μm thick substrates, 25 and 50μm pitch
- New test structures with 10μm pitch on 50μm substrate being designed: ~ 1ns charge collection time



L. Pancheri et al., IEEE Tran. Electron Dev., Vol. 67, No. 6, June 2020