FAST3: Front-End Electronics to Read Out Thin Ultra-Fast Silicon Detectors for ps Resolution

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2022 IEEE Latin American Electron Devices Conference (LAEDC) | 978-1-6654-9767-1/22/$31.00 ©2022 IEEE | DOI: 10.1109/LAEDC54796.2022.9908192

Abstract— **This paper presents a new version of the FAST family of ASICs and its comparison with the previous version. The new design, FAST3, aims at a timing jitter below 15 picoseconds when coupled to Ultra-Fast Silicon detectors (UFSD). The FAST3 integrated circuit is designed in standard 110 nm CMOS technology; it comes in two different versions: the amplifier-comparator version comprises 20 readout channels, while the amplifier-only version 16 channels. The ASIC power rail is at +1.2 V, and the power consumption for the front-end stage is 2.4 mW/ch and about 5 mW/ch for the output driver. In our tests, the FAST2 ASIC, coupled to a UFDS with a capacitance of 3.4 pF, achieves timing jitters of about 25 ps at an input charge of about 15 fC, while the simulation indicates that the FAST3 jitter will be about 15 ps at the same charge. Furthermore, FAST3 enhances its dynamic range up to 55 fC compared to the 15 fC of FAST2.**

Keywords— Silicon radiation detectors, Timing Jitter, UFDS, Ultra-Fast electronics, CMOS.

I. INTRODUCTION

The FAST3 family of ASICs is an optimized version of the FAST2 family to be used in silicon trackers with excellent temporal resolution (< 40 ps). Such silicon trackers are foreseen in future experiments to mitigate the pile-up effects [1] due to increased luminosity [2]. For this reason, ultra-fast electronics with a timing jitter lower than 30 ps is necessary. This study shows how the FAST3 ASICs cover the main requirements of the high luminosity experiments, such as jitter and dynamic range. FAST3 is the fourth generation of our R&D program in front-end electronics, following the TOFFEE, FAST1, and FAST2 ASICs [3][4][5].

The FAST3 tape-out includes two different ASICs:

- FAST3D_EVO1, with 20 readout channels, implements an amplifier-comparator architecture based on the FAST2D_EVO1 ASIC. However, the amplification stage presents modifications to reduce the jitter and enhance the dynamic range.
- FAST3A, with 16 channels, is an amplification-only design with a buffer stage. The amplification stage is identical to that of FAST3D_EVO1.

The new amplification stage of FAST3, present in both versions, provides improved features, such as the increment of output range from 300-350 mV to 700-750 mV and the reduction of the minimum jitter down to 10 ps for input charges larger than 20 fC.
This study presents the transistor-level design of the new amplification stage and its key features. It also contains the comparison between the experimental result of FAST2A ASICs coupled to a 3.4 pF UFSD (Ultra-Fast Silicon Detector) [6], and the post-layout simulation of FAST3 Analog. This comparison is a good indicator of the improvements in FAST3 since the experimental and post-layout results of FAST2 are in excellent agreement, with differences in the 5-7 % range.

The FAST family of ASIC is designed to work with thin Ultra-Fast Silicon Detectors (50 microns thick) with relatively large capacitance (3-4 pF) and a signal charge range of 5 – 30 fC. The sensor bias determines the gain, i.e., the amount of signal charge. The bias range is about 120-240 V. The FAST2 family has been tested using minimum ionizing particles (beta telescope) and a 110 nm focused laser beam (TCT system) that emulates the energy deposition of a charged particle. The study with the TCT system allows measuring the jitter term, the critical figure-of-merit in ASIC designed for high precision timing [10][11].

II. ASIC ARCHITECTURE

The FAST3 family is designed in UMC 110 nm CMOS technology and uses a power rail of 1.2 V. Both FAST3D and FAST3A implement a simple control logic to modify the readout chain's internal parameters shown in Fig. 1. This control logic consists of two registers:

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The first register has 12 bits per channel (2 bits empty):

- Three bits program the DC gain with 8 selectable gains. This option appears in the analog and digital versions.
- Six bits are used to program the local threshold (V_{th}) of the discriminator. The local V_{th} compensates for the output baseline divergences among channels. It covers a range of 32 mV (only in the digital version).
- The last bit of the local register enables the internal charge injection system.

The second register is common to the whole ASIC, and it comprises 6 bits to control the internal charge injection levels. FAST2D and FAST3D use a trans-impedance amplifier (TIA) connected to a fast discriminator, as shown the Fig. 1. The ASICs output uses low voltage differential signaling (LVDS driver).

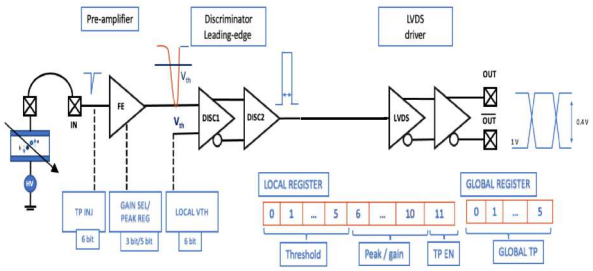

Fig 1. Full readout chain schematic of the FAST3_EVO1 ASIC.

This paper focuses on the comparison of FAST2 and FAST3 Analog. Both ASICs use an identical pre-amplifier stage (1st stage), as shown in Fig. 2. However, FAST3 includes a second stage to amplify the signal, increase the dynamic range and drive a 50 Ω load (Fig. 2). The second stage is an operational amplifier in the inverter configuration, which integrates a Class AB driver as the output stage.

The first stage is a broad-band architecture, which presents a common source topology with an RF transistor as an input transistor (M0). RF transistor facilitates the operation at high frequencies. Besides, the input transistor implements an nMOS topology to guarantee a high-speed circuit due to its high G_m compared to a pMOS topology [7]. The DC current (I_{R1b}) is set at 100 uA.

The pre-amplifier stage benefits from an auxiliary branch (M5,6) configuration since it provides an extra DC current through the input transistor. The auxiliary current varies in a range between 1 a 1.5 mA. The extra DC current is needed since the higher the drain current through the input transistor, the higher its transconductance and gain-bandwidth product, and consequently, the smaller the input resistance [8]. The programmable DC gain, set by R_f, presents three different resistances of 5k, 15k, and 30 k. The parallel combination of these resistances generates the eight selectable gains through the 3 programmable bits.
R_1 and R_{1b} set the DC operating point with DC current equal to 77 uA and 100 uA, respectively. In this architecture, the DC currents are generated with resistors (R_0, R_1) instead of using current mirrors connected to the current generator since this choice generates the lowest RMS noise and parasitic capacitance, improving the achievable jitter.

FAST3 Analog couples the first stage to the inverter stage through a radio frequency capacitor to isolate the respective DC operating points. The inverter stage (Fig. 3) implements a low gain differential amplifier architecture with a class AB amplifier integrated into the output node. The amplifier presents an nMOS topology with the minimum channel length input transistors. In the first stage, the nMOS topology generates a large transconductance to work at high frequencies [9]. The operational amplifier provides a gain bandwidth of around 1 GHz necessary to obtain a rising time below 1.5 ns. The DC gain is equal to 6, which provides a high amplitude at low charges, and it avoids staying close to the unity-gain effects in terms of stability [7].

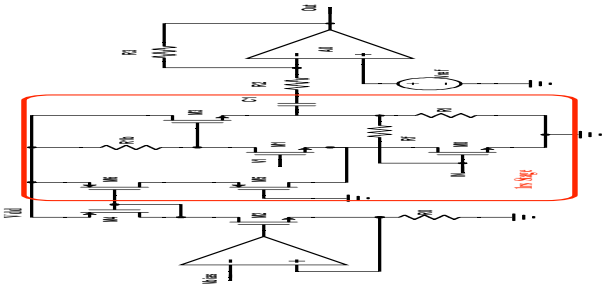

Fig 2. Pre-amplifier stage and inverter stage schematic used by FAST3D and FAST3A.

FAST3 Analog couples the first stage to the inverter stage through a radio frequency capacitor to isolate the respective DC operating points. The inverter stage (Fig. 3) implements a low gain differential amplifier architecture with a class AB amplifier integrated into the output node. The amplifier presents an nMOS topology with the minimum channel length input transistors. In the first stage, the nMOS topology generates a large transconductance to work at high frequencies [9]. The operational amplifier provides a gain bandwidth of around 1 GHz necessary to obtain a rising time below 1.5 ns. The DC gain is equal to 6, which provides a high amplitude at low charges, and it avoids staying close to the unity-gain effects in terms of stability [7].

In addition, the circuit implements a pole splitting compensation technique, which guarantees a safe phase margin since it shifts the second pole to the desired place [8]. The last feature of the circuit is the driver stage. The class AB amplifier can drive any value of load, including 50 Ω, with a symmetrical slew rate.

The transistor sizing is performed considering the following steps:

- The current mirrors M_5:M_6 and M_7:M_8 amplify the DC current (50 µA) of the input transistors by three.
- The DC current through transistors M_{11} and M_{12} is 15 times lower than the current through the class AB transistors. To guarantee a good matching, the aspect ratio of M_{19}:M_{11} and M_{12}:M_{20} is established at 15 as well.
- The size of the miller capacitance and transistors M_{19} and M_{20} were computed using Eq. 1 and 2. The miller capacitance, equal to 100 fF, guarantees a phase margin higher than 50° with K_{pm}=2 (phase margin constant), and β is $\frac{C_{ox}\mu_c}{2}$.

$$C_M = \frac{g_{m20}}{f_p} \qquad Eq.\ 1$$

$$\frac{W}{L}_{19,20} \geq \frac{C_M * GBW * K_{pm}}{4\beta * I_d} \qquad Eq.\ 2$$

The inverter amplifier sets the input common-mode voltage at 900 mV to maximize the dynamic range of a negative output pulse.

The layout structure of the FAST3 Analog is described in Fig. 4: in the figure, the output signal pads are on the top side of the chip, while the bottom side contains the input signal pads. The lateral pads provide the connection for the bias and power inputs. The layout structure occupies an area of 1x5 mm^2.

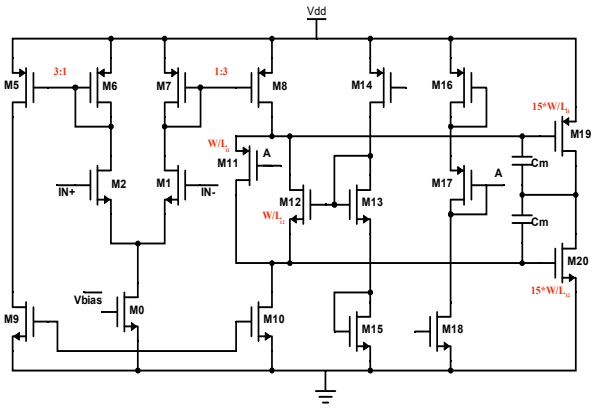

Fig. 3. Transistor-level design schematic of the inverter operational amplifier.

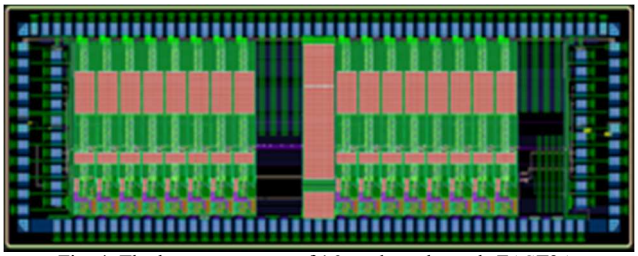

Fig. 4. The layout structure of 16-readout channels FAST3A.

III. Experimental Results Fast 2

The characterization of FAST2 connected to a UFSD sensor was performed using the scanning TCT system and a specially designed board hosting FAST2+UFSD, shown in Fig. 5.

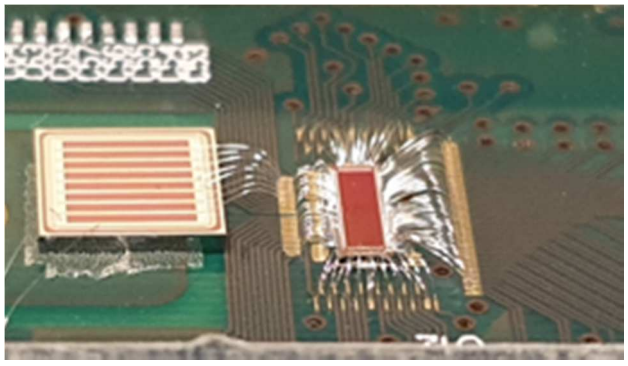

Fig. 5. FAST2_EVO1 ASIC and UFSD bonding to the PCB.

Fig. 6. Shows a few examples of the FAST2A_EVO1 output signal. In this figure, FAST2A has a rising time of about 1.5 ns and an RMS noise equal to 1.5 mV. The study of the jitter is performed acquiring thousands of waveforms for each bias value.

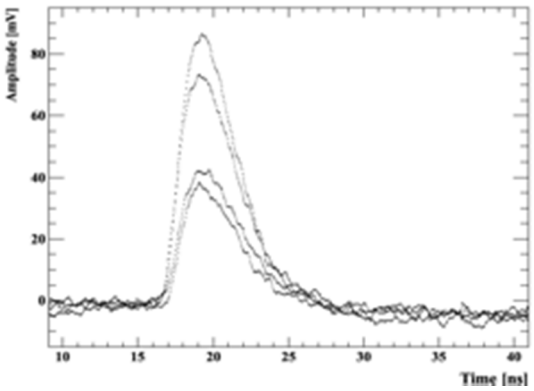

Fig. 6. Output waveforms of a single channel using different input charges.

IV. Post Layout Simulation Fast 3 and Time Resolution

The post-layout (PL) simulation of the jitter and dynamic range of FAST2 agrees very well (within less than 10%) with the experimental results obtained during the FAST2 TCT studies. Therefore, comparing the PL simulation of FAST3 with the FAST2 experimental results provides a good indication of the performance differences between FAST2 and FAST3.

The frequency spectrum of FAST3 is shown in Fig 7. FAST3 has a gain bandwidth of 920 MHz and a bandwidth of 250 MHz, which allows the circuit to develop a rising time of around 1.5 ns.

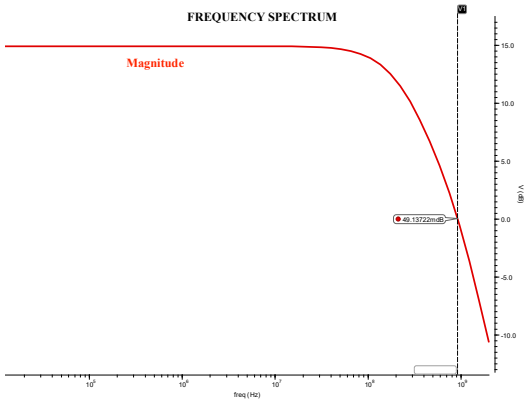

Fig. 7. Frequency response at the close loop of FAST3 second stage. It shows a DC voltage gain of 14.8 dB (5.6).

The jitter, computed in PL simulation such as Fig. 8, has been estimated to simulate 1000 output waveforms.

For an input charge of 8 fC, FAST3 owns a jitter, computed at 40% of the signal amplitude, of around 20 ps, including the 7% of divergence.

The FAST2 and FAST3 ASICs timing jitter and dynamic range are used to estimate the differences between the two designs. The jitter performance as a function of the input

charge is reported in Fig. 9. The amplitude of the FAST2 output signal saturates at charges above 25 fC, and the jitter term saturates at about 8 ps (Fig. 9, blue line). FAST3 accomplishes 2 great improvements, one is the small timing jitter at low charges, providing a reduction of 50% up to 8 fC.

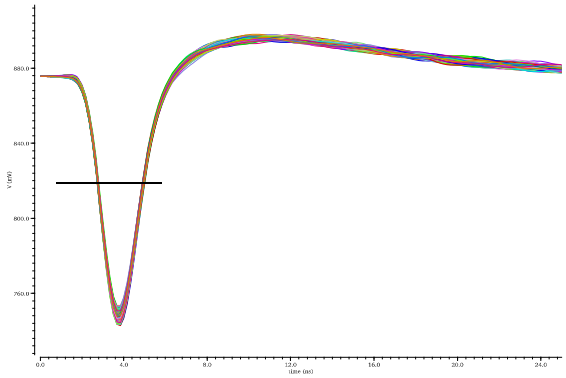

Fig 8. The output waveform of post-layout simulation at 1 MIP (8fC).

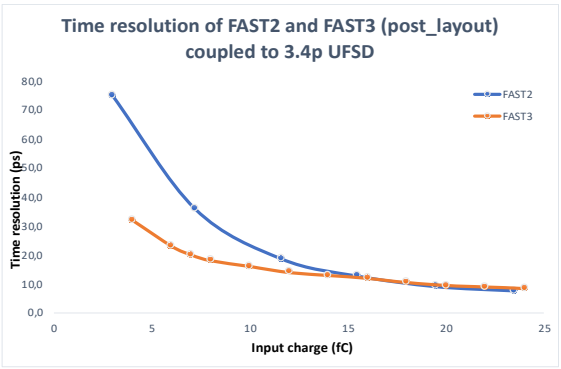

Fig. 9. Comparison of the measured jitter of FAST2 with the FAST3 PL simulation. Both ASICs are coupled to a 3.4 pF, 50-micron thick UFSD sensor.

Overall, according to PL simulation, the FAST3 amplitude does not saturate before 750 mV. FAST2 output swing is about 400 mV, limiting the performance at large input charges. FAST3 more than doubles the dynamic range, thanks to the integration of a class AB driver as the output stage. FAST3 develops an output swing of 800 mV, as shown the Fig.10.

The FAST3 dynamic range is about 50-55 fC without saturating the output signal. The post-layout and experimental test include the detector capacitance effect, using the electrical model of the UFSD detector in the CAD simulation.

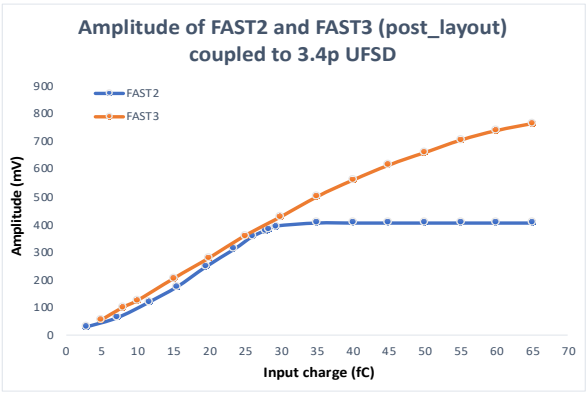

Fig. 10. The amplitude of output signal vs. input charge curve of FAST2A and FAST3A.

V. CONCLUSION

FAST3 substantially enhances the performance of FAST2, increasing the dynamic range from 15 fC to about 55 fC and decreasing the jitter by more than 40%, reaching about 15 ps at 15 fC. The FAST3 power consumption is about 7.5 mW/Ch, mostly due to the output buffer.

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