FAST: a 30 ps time resolution front-end ASIC for a 4D tracking system based on Ultra-Fast Silicon Detectors

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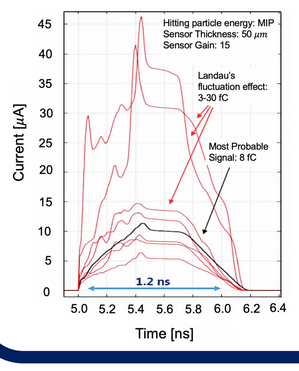
Abstract

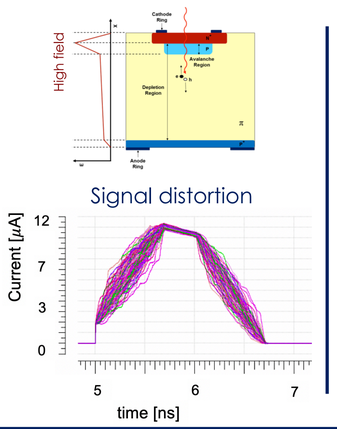
The UFSD group of Turin is working at the development of custom front-end electronics for the read-out of thin silicon sensors with moderate internal gain (Ultra-Fast Silicon Detectors- UFSD), aiming at applications that require very precise time tagging. The possibility of measuring the time of passage of charged particles with a pico-seconds accuracy while maintaining very good spatial resolution (~100 micron) is a very important development in the field of charged particle tracking. In this poster we present **FAST**, a 20 channels novel low power front-end electronics for UFSD, devoted to timing resolution with a **jitter lower than the 30 ps** target. In order to map different solutions, we designed **three flavors** of FAST differing in the amplification stages and component-level technical choices. During the design phase, extensive simulation considered the intrinsic sensor signal shaping, including radiation damage effects. Preliminary characterization results from the first ASIC prototype are shown in this poster.

UFSD sensors (I)

Landau's statistical fluctuations



- The signal amplitude in silicon sensors follows the **Landau distribution**
- Non-uniform ionization along the track generates distortion in the collected charge. This effect is responsible of the sensor contribution in the time resolution
- **These effects can be modelled** with good accuracy and the use of these models allows to simulate every custom readout electronics with much more accuracy

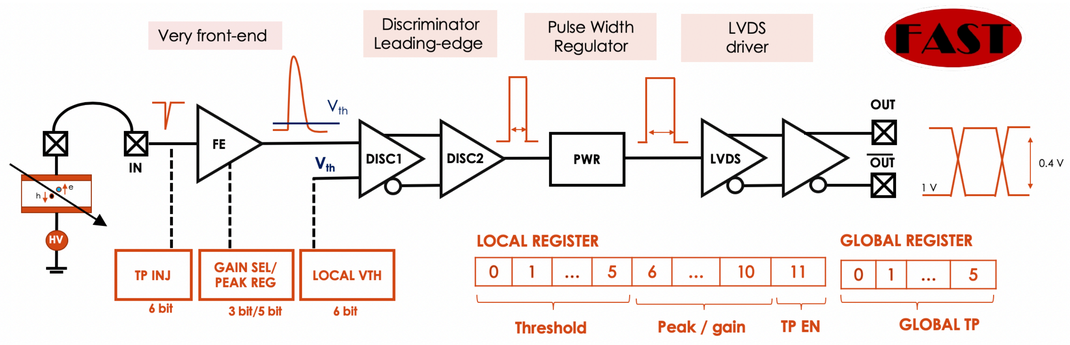


Design approach

$$\sigma_t^2 = \overbrace{\sigma_{LANDAU\ NOISE}^2 + \sigma_{DISTORTION}^2}^{\text{sensor}} + \overbrace{\sigma_{JITTER}^2 + \sigma_{TDC}^2 + \sigma_{TIME\ WALK}^2}^{\text{readout electronics}}$$

- The front-end amplifiers of FAST have been optimized and simulated by using a **system level** approach which aims to take into account each term in the time resolution formula
- **Sensor contribution**: this information is included by means of Weightfield2. It allows to introduce in the simulations effects of Landau distribution, distortion and effects of radiation in silicon.
- **Electronics simulations**: this contribution is evaluated by using transient noise simulations in EDA tools. Parasitics (R-C-CC) in the ASIC are extracted by using two different tools and they are included in the simulations. In these simulations time walk is corrected with the Time over Threshold technique.

The Front-End Electronics



Pulse width regulator

- Pulse duration(MPV): **2-4 ns**
- This block can increase the discriminator output length to make it compatible with **commercial TDCs**

LVDS driver

- It allows compatibility with **commercial TDCs and FPGAs**

The very front end

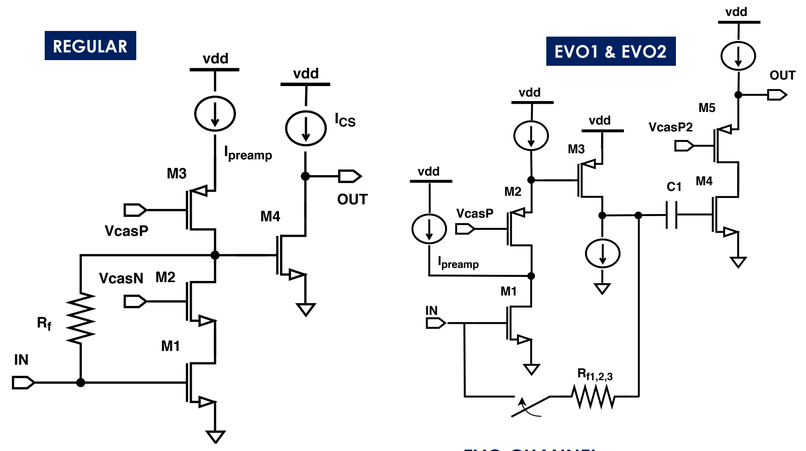
- **Three** architectures: REGULAR, EVO1 and EVO2
- Power limited to **1.5 mW/CH**
- Designed for **1 proton MIP in 50 μm** thick UFSD sensor
- Sensor cap: **1 pF – 6 pF**

Ancillary circuitry

- **Test Pulse injection system:** a global 6 bit register is used to inject charge among 0.3 -18 fC
- **Selectable gain (EVO) or peaking time (REGULAR):** 3 bits/5bits used to select 8 different gains in EVO or for the peaking time tuning in REG. The last regulation is meant to minimize noise
- **Local threshold regulation:** the threshold can be locally regulated up to 30 mV with 6 bits DAC
- **Pulse width regulation:** it allows to add a fixed Δt to the pulse duration.

Discriminator

- Two stage leading-edge differential discriminator
- Power < **0.6 mW/CH**
- **time walk** → offline corrected



REGULAR CHANNEL

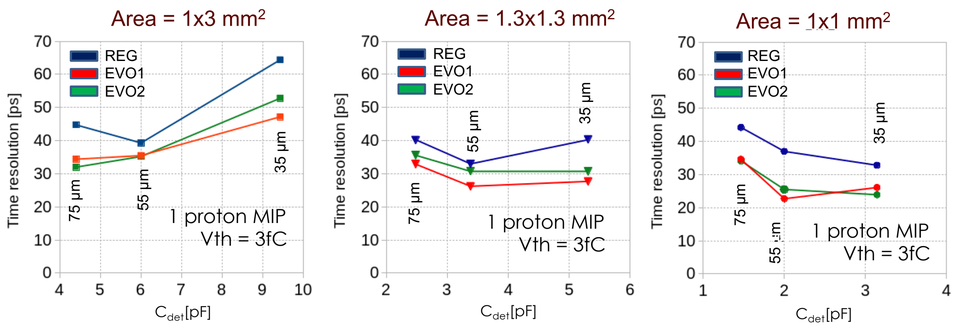
- **Limited bandwidth to 100 MHz**
- Gain: ~ 60 mV/fC
- **Noise: ~310 e-**
- Power consumption: ~1.2mW/CH
- SNR (MIP): ~ 160
- Max hit rate: 50 MHz

EVO CHANNEL

- **Larger bandwidth: ~ 400 MHz**
- Gain: ~ 31 mV/fC (8 regulations)
- **Noise: ~640 e-**
- Power consumption: ~1.2mW/CH
- SNR(MIP): ~75
- Max hit rate: 300 MHz
- AC coupling to reduce mismatch
- 2 topologies: standard CMOS & RF

Simulation results

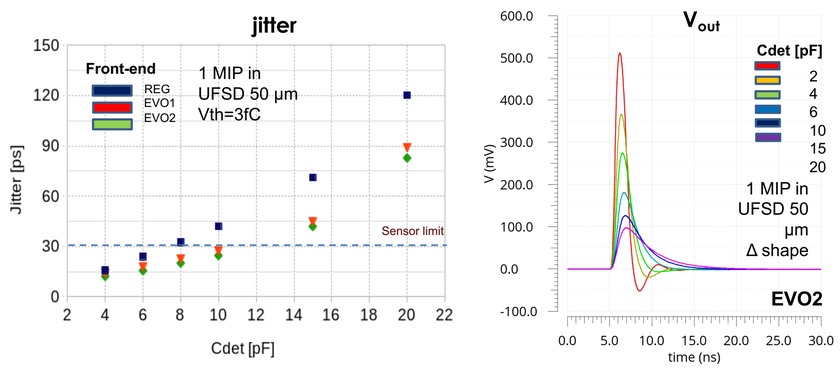
Time resolution vs sensor geometry vs sensor thickness



- 3 geometries
- 3 thicknesses
- 3 front-ends

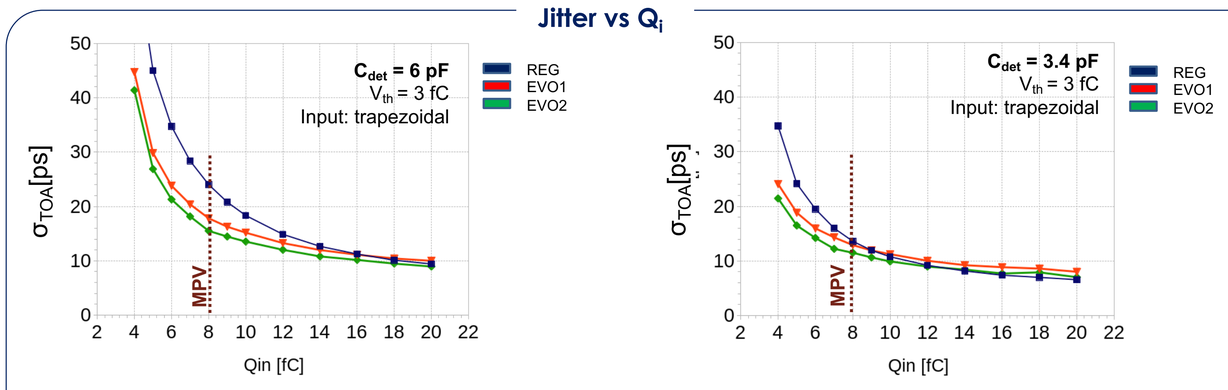
- Area=1x3mm²: time resolution depends on the sensor thickness. **Larger pads require thicker sensors**
- Area=1.3x1.3mm²: good balance between sensor and electronics contribution. In this case time resolution does not depend on the sensor thickness
- Area=1x1mm²: the best time resolution is obtained with thin sensors.

Effects of C_{det}



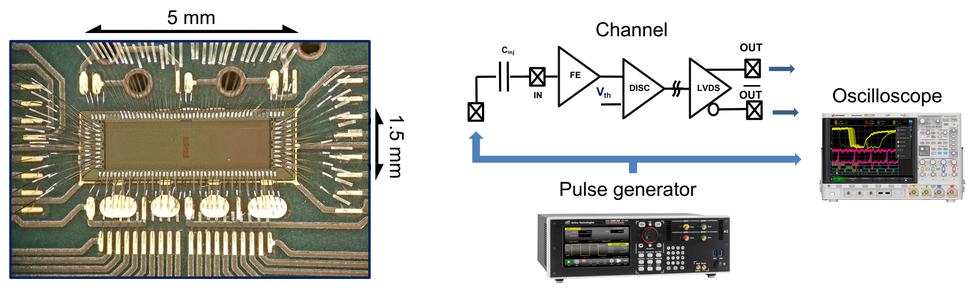
- Jitter is below 30 ps for Cdet < 10 pF
- Analog output (amplitudes and duration) changes with the C_{det}
- Amplifiers are designed to reach 30 ps with 6 pF UFSD sensor
- Generally if the sensor cap decreases, time resolution improves and signals become narrower

Jitter vs Q_i

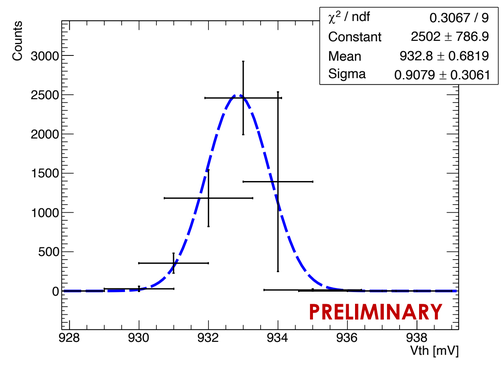


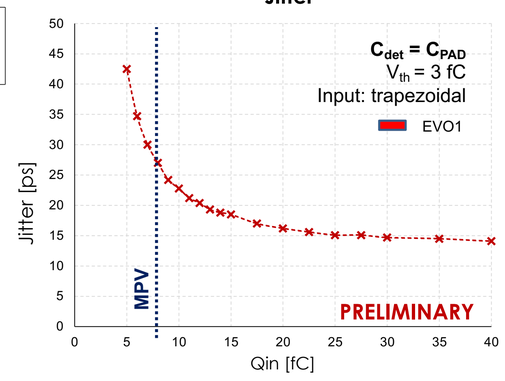
- The MPV in 50 μm A UFSD sensor with a gain of 15 is 8 fC. For this charge, jitter is below 20 ps for EVO channels and around 25 ps for REGULAR
- Jitter for the three flavors is less than the expected sensor contribution which is 30 ps (in 50 μm UFSD)
- Jitter becomes negligible (about 10 ps) for high values of Qin

Setup and first experimental results



- The experimental setup is based on a custom board where the ASIC is wire bonded, an external pulser used to inject charge and an oscilloscope
- The final DAQ system will be based on a FPGA. It will allow to program the chip registers and to readout the information generated by the ASIC. This information will be sent to a software written in LabView.





- Noise is measured with a threshold scan (Vth) counting number of hits at the channel input in a fixed time. Measured noise is 0.9 V.
- Jitter is measured as the standard deviation of the delay between the injected pulse and the channel response. With a threshold voltage fixed to 3 fC, the preliminary jitter for a MPV of 8 fC is 27 ps. The saturation value is 13 ps.
- An automated readout system is under development to characterize the different FAST prototypes and flavors.

Outlooks

- The FAST characterization campaign is ongoing
- Test with different UFSD sensors: laser and active sources
- Test beams with protons is planned in 2020

References: [1] G. Paternoster et al., "Developments and first measurements of Ultra-Fast Silicon Detectors produced at FBK", JINST 12 (2017) C02077 ;

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