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LAUREA MAGISTRALE IN FISICA



MASTER THESIS

Characterization of the Latest Ultra-Fast Silicon Detector Productions for the MIP Timing Detector of the CMS Experiment

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Abstract

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In the next years, the Compact Muon Solenoid (CMS) detector at CERN will undergo a series of upgrades to cope with the much harsher conditions of the High-Luminosity Large Hadron Collider (HL-LHC). One of the main upgrades will be the introduction of the MIP Timing Detector (MTD), able to measure the time of minimum ionizing particles precisely. The Endcap Timing Layer (ETL) of the MTD will be instrumented with Low Gain Avalanche Diodes. This novel sensor technology achieves excellent time resolutions ($\sim 30 \ ps$) thanks to an internal gain mechanism. Torino is leading the sensor R&D, intending to define the sensor design characteristics suitable for the ETL detector. The CMS collaboration is currently concluding the R&D and prototyping phase, so the final sensor design will have to be chosen within a year. This thesis aims to study some key features of the latest sensor productions using ad hoc test methodologies.

This work directly contributes to the technological choices that will define the LGAD sensors of the CMS ETL detector.

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The responsibility for any errors, inaccuracies, and omissions is entirely mine.

Contents

Al	bstrac	ct	iii				
A	cknov	wledgements	v				
Co	onten	its	vii				
In	trodu	action	1				
1	The	CMS MIP Timing Detector Project for the HL-LHC Era	3				
	1.1	Introduction	3				
	1.2	The High-Luminosity Large Hadron Collider	4				
		1.2.1 Present Luminosity at the LHC	4				
		1.2.2 The HL-LHC Project	5				
		1.2.3 Luminosity Impact on CMS Experiment	8				
	1.3	The MIP Timing Detector Project	9				
		1.3.1 Overview of the MTD	9				
		1.3.2 The Endcap Timing Layer	12				
		1.3.3 Impact of the MTD on the CMS Physics Program	14				
	1.4	Conclusions	17				
2	velopment of Ultra-Fast Silicon Detectors for the ETL	19					
	2.1	1 Introduction					
	2.2	Traditional Silicon Sensor Main Features	20				
		2.2.1 The <i>pn</i> Junction Characteristic	20				
	2.3	UFSD Main Features	22				
		2.3.1 Time Resolution	23				
		2.3.2 Radiation Tolerance	24				
		2.3.3 UFSD Design	27				
	2.4	UFSD Productions	28				
		2.4.1 Old Productions	28				
		2.4.2 UFSD3.1 Production	29				
		2.4.3 UFSD3.2 Production	30				
		2.4.4 HPK2 Production	32				
	2.5	UFSD Characterization	33				
		2.5.1 IV Characteristic	33				
		2.5.2 CV Characteristic	34				
		2.5.3 Beta Source Characterization	38				
3	Cha	racterization of the Latest UFSD Productions	39				
	3.1	Introduction	39				
	3.2	Characterization of the UFSD3.2 Production	40				
		3.2.1 The UFSD3.2 Data Sample	40				
		3.2.2 Description of Analysis Framework	41				

3.2.3 Analysis of the IV Characteristics								
3.2.4 Analysis of the CV Characteristics								
3.3 Floating Pads Characterization								
	3.3.1	Measurements	69					
	3.3.2	Experimental Setup	70					
	3.3.3	Results	71					
3.4	Inter-p	bad Resistance Characterization	78					
	3.4.1	Measurements	78					
	3.4.2	Experimental Setup	82					
	3.4.3	Results	83					
Conclu	Conclusions 8							
A List of the Main Contributions 9								
List of l	List of Figures							
List of Tables								
List of A	List of Abbreviations							
Bibliog	Bibliography							

Introduction

In the next years, the Large Hadron Collider (LHC) will increase the peak luminosity and, therefore, the experiments physics discovery potential. For this reason, also the Compact Muon Solenoid (CMS) experiment will undergo several upgrades, among which the introduction of the MIP Timing Detector (MTD).

Ultra-Fast Silicon Detectors (UFSDs) will instrument the Endcap Timing Layer (ETL) of the MTD. UFSDs are silicon sensors based on the novel Low Gain Avalanche Diode (LGAD) technology optimized for high energy physics applications. This work aims at performing a detailed characterization of the latest Ultra-Fast Silicon Detector (UFSD) productions.

A detailed description of the MIP Timing Detector will be given in the first chapter, emphasizing the Endcap Timing Layer description.

In the second chapter, the development of the ETL sensors will be discussed, and the main features of UFSD that distinguish them from traditional silicon sensors will be outlined. This chapter details the latest three productions from Fondazione Bruno Kessler (FBK) and Hamamatsu Photonics K. K. (HPK). The primary characterization methods will also be discussed: current-voltage, capacitance-voltage, and time resolution characterizations.

The third chapter will be dedicated to present the results of this work. The UFSD characterization is based on analysis of the data measured at FBK, together with measurements performed in the *Innovative Silicon Sensor Laboratory* in Torino. The FBK data allows the study of some key aspects of the productions, such as quality, uniformity, and yield. Moreover, the study of device behavior will be discussed in detail, both in new and irradiated sensors.

This work has been presented in dedicated meetings of the CMS collaboration, meetings with vendors, and national conferences (see appendix A). It brought a valuable contribution to the choice of suitable sensors for the ETL.

Chapter 1

The CMS MIP Timing Detector Project for the HL-LHC Era

1.1 Introduction

Today, the CERN Large Hadron Collider (LHC) is the most powerful particle accelerator globally. Since its first onset in 2010, it has been the main center of worldwide High Energy Physics (HEP) researches. The LHC reached its nominal energy for proton-proton collisions in 2018, and it is expected to perform at the same energy in the actual run, from 2021 to 2023. Then, there will be an extended shutdown, in which the LHC will be upgraded to the High-Luminosity Large Hadron Collider (HL-LHC) [1]. During the HL-LHC lifetime, the nominal energy will remain the same, but there will be a significant luminosity upgrade.

The HL-LHC project was already defined in 2010. The main objective is to increase the peak luminosity, which will become fundamental to exploit the full potential of the LHC. Several LHC upgrades will be necessary to reach this goal and, therefore, subsequential experiment upgrades. For a few years, a massive R&D has been carried out to find suitable technologies.

This thesis deals with one of the main upgrades of the CMS experiment: the MIP Timing Detector (MTD). The MTD will be essential to cope with the HL-LHC much harsher conditions, particularly the high number of pileup interactions. This chapter will offer some insight into the MTD project after a brief introduction of the HL-LHC.

1.2 The High-Luminosity Large Hadron Collider

At the moment of the Large Hadron Collider (LHC) construction in the early 21st century, the main physics motivations were [2]:

- to understand the origin of the particle masses, in particular, search for the Standard Model's (SM) Higgs boson;
- to look for physics beyond the Standard Model, such as manifestations of Grand Unified Theories (GUT) or Supersymmetry (SUSY) theory;
- to answer to many others open questions, such as if quarks and leptons are elementary particles, if there are more than three families of leptons, the origin of asymmetry between matter and antimatter;
- to perform precision measurements of the known particles and interactions and improve results related to the W, the bottom quark, and the top quark physics.

Thanks to CMS and ATLAS experiments, the SM Higgs boson was observed in 2012. The Higgs boson discovery is undoubtedly one of the major achievements of the LHC and one of the major milestones in science history.

No evidence for GUT or SUSY was found in the LHC so far, neither information on the origin of asymmetry between matter and antimatter. However, a series of physical limitations have been found for topics such as SUSY [3], GUT [4], Weakly Interactive Massive Particle (WIMP) [5].

Moreover, a series of precision measurements have been performed, especially regarding QCD. Hard-scattering measurements have been carried out from the beginning, leading to impressive precision on Parton Distribution Function (PDF) determinations, enough to make some authors talk about "*the LHC precision era*" [6].

Despite its incredible contributions to HEP, the LHC will need several upgrades to exploit its full physics potential and try to answer still open HEP questions.

A higher luminosity is required to accumulate more statistics. Therefore, the luminosity upgrade is planned for the following years. It will lead to the High-Luminosity LHC (HL-LHC), which is expected to be operational in the next five to ten years.

1.2.1 Present Luminosity at the LHC

The LHC reached the nominal design luminosity of $1 \times 10^{34} cm^{-2} s^{-1}$ on 26 June 2016, during the so-called *Run 2*, which lasted from 2015 to 2018. This excellent performance led to a total integrated luminosity of about 35 fb^{-1} for the year.

In the following years, the peak luminosity has kept increasing until the beginning of 2019, where it reached the value of $2.2 \times 10^{34} \ cm^{-2} \ s^{-1}$, more than twice the nominal design value.

From figure 1.1, by comparing the nominal peak luminosity value (green dotted line) with the measured peak luminosity values (red and blue dots), one may notice that the expected value has been widely reached and exceeded [7].

The total integrated luminosity reached about 30 fb^{-1} at the end of 2012 and about 160 fb^{-1} by the end of Run 2 in 2018. The evolution of the integrated luminosity is shown in figure 1.2.



FIGURE 1.1: Measured peak luminosity during Run 1 (from 2010 to 2012, red dots) and Run 2 (from 2015 to 2018, blue dots). Nominal design luminosity (green dotted line) has been reached on 26 June 2016. Figure from [7].

Remarkably, all the hadron colliders worldwide before the LHC have produced a combined total integrated luminosity of about 10 fb^{-1} , while the LHC has delivered nearly 30 fb^{-1} at the end of 2012.



FIGURE 1.2: Integrated luminosity during Run 1 (from 2010 to 2012, red line) and Run 2 (from 2015 to 2018, blue line). Figure from [7].

1.2.2 The HL-LHC Project

The peak luminosity value of $2.2 \times 10^{34} \ cm^{-2} \ s^{-1}$, reached at the end of Run 2, is a limitation of the LHC interaction quadrupoles. Peak luminosity cannot increase more without a cryogenic cooling improvement. The quadrupoles cooling is the main obstacle for the luminosity increase, but there are other factors to consider as limitations such as inner triple magnets and collimation [1].

In summary, the peak luminosity is limited by several factors. However, after 2023 (at the end of the so-called *Run 3*), the statistical gain in running LHC without a luminosity increase will become marginal. The peak luminosity has to be increased to exploit the full physics potential of the LHC.

CERN council defined the High-Luminosity LHC (HL-LHC) project already at the end of 2010, intending to determine a set of beam parameters and the hardware configuration to reach the following targets:

- a peak luminosity of $5 \times 10^{34} \ cm^{-2} \ s^{-1}$, five times the initial design value;
- an integrated luminosity of 250 fb^{-1} per year with the goal of 3000 fb^{-1} in about a dozen years, which is about ten times the value reached during the first twelve years of the LHC lifetime.

Run periods and shutdown periods always alternate. During shutdown periods, the LHC undergo some maintenance works and, eventually, some upgrades. The installation of the leading hardware for the HL-LHC era will be done during the so-called *Long Shutdown 3* (LS3), from 2024 to 2026. The LHC will re-start in 2026 already in the HL-LHC configuration. A complete forecast for luminosity is shown in figure 1.3, emphasizing the run and shutdown periods.



FIGURE 1.3: Forecast for peak luminosity (red dots) and integrated luminosity (blue line) in the HL-LHC era, according to nominal parameters. Figure from [1].

All equipment is designed with a 50% safe margin for instantaneous heat deposition and the integrated radiation dose. Therefore, the concept of *ultimate performance* has been defined. By pushing the HL-LHC beyond its nominal parameters, the ultimate performance values are reached. Simulations show that it should be possible to reach the ultimate performance values of:

- a peak luminosity of $7 7.5 \times 10^{34} \ cm^{-2} \ s^{-1}$;
- an integrated luminosity of $300 350 \ fb^{-1}$ per year with the value of $4000 4500 \ fb^{-1}$ in about a dozen years.

A complete forecast for luminosity in the case of ultimate parameters is shown in figure 1.4. The main differences respect to figure 1.3 are in the so-called *Run 5* (2030-2033, after *Long Shutdown 4*) and in the so-called *Run 6* (2035-2039, after *Long Shutdown 5*).



FIGURE 1.4: Forecast for peak luminosity (red dots) and integrated luminosity (blue line) in the HL-LHC era, in the case of ultimate parameters. Figure from [1].

In 2013 the European Strategy for Particle Physics Council identified as the highest priority "*the exploitation of the full potential of LHC, including the high-luminosity upgrade of the machine and detectors to collect ten times more data than in the initial design, by around 2030*" [8]. This decision made the HL-LHC project a concrete reality and started an intensive R&D from a large international community.

The nominal design key parameters of LHC and HL-LHC can be summarized in the table 1.1, comparing them with other significant experiments worldwide. A particular emphasis should be placed on the values of the peak luminosity \mathcal{L} .

Experiment	Beam Energy	Ν	R [Hz]	σ_x/σ_y [μm]	$\mathcal{L} \left[cm^{-2}s^{-1} ight]$
$SPS(p\bar{p})$	315 GeV	$1 imes 10^{11}$	$4 imes 10^5$	60/30	$6 imes 10^{30}$
Tevatron($p\bar{p}$)	1 TeV	$30/8 imes 10^{10}$	$4 imes 10^6$	30/30	$5 imes 10^{31}$
$LEP(e^+e^-)$	105 GeV	$5 imes 10^{11}$	≤ 1	200/2	$1 imes 10^{32}$
LHC(pp)	7 TeV	$1.1 imes10^{11}$	$4 imes 10^7$	17/17	$1 imes 10^{34}$
HL-LHC(pp)	7 TeV	$2.2 imes 10^{11}$	$4 imes 10^7$	15/15	$5 imes 10^{34}$

TABLE 1.1: Comparison of luminosity and key parameters comparison between the LHC, the HL-LHC, and other significant experiments worldwide. Values from [1] and [9].

1.2.3 Luminosity Impact on CMS Experiment

The Compact Muon Solenoid (CMS) detector is a multi-purpose apparatus due to operating at the LHC. It has taken data since the beginning of LHC runs in 2010, and it will also continue in the HL-LHC era with some upgrades [10].

In the LHC nominal scenario, with a peak luminosity of $1 \times 10^{34} \ cm^{-2} \ s^{-1}$, the CMS average number of *pileup* interactions, i.e., the average number of collisions per bunch crossing, is about 40. During Run 2, the peak luminosity reached $2.2 \times 10^{34} \ cm^{-2} \ s^{-1}$ and the CMS average number of pileup interactions has grown at about 50-60 per bunch crossing. This number of pileup is still acceptable, but it approaches the values at which the reconstruction algorithm begins to fail at a substantial rate.

During the HL-LHC era, the number of pileup interactions will grow even faster: a CMS average pileup of 140 will be obtained in the nominal design with peak luminosity of $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. In comparison, a CMS average pileup of 200 will be obtained in the ultimate performance scenario with a peak luminosity of $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. In figure 1.5 a simulation of the reconstruction of 140 pileup p-p collisions in the CMS tracker is shown.



FIGURE 1.5: Simulation of the reconstruction of 140 pileup p-p collisions in the CMS tracker. Figure from [11].

The luminosity upgrade will produce a much higher collision rate that will far exceed the existing CMS detector capabilities due to a much higher number of pileup interactions.

During the HL-LHC era, hard interactions, which are the most interesting interactions for the CMS experiment, will occur in far fewer than 1% of the total beam crossing but will always be accompanied by an average of 140-200 additional interactions. The identification and the reconstruction of the hard interactions will be inevitably degraded.

Furthermore, the higher collision rate results in more radiation damage in the overall detectors.

In summary, to maintain the current excellent performance in efficiency, resolution, and background rejection, the CMS will be upgraded in parallel with the LHC. The upgraded detector must survive and function efficiently in this much harsher pileup and high radiation level environment [12].

1.3 The MIP Timing Detector Project

The Compact Muon Solenoid (CMS) detector at the LHC will undergo several upgrades to tackle the HL-LHC challenging conditions. A particular challenge of such a high luminosity phase will be a large number of pileup interactions during collisions being a factor up to five times higher than current pileup conditions [13].

A higher pileup affects the CMS tracking reconstruction performance and efficiency because a higher number of interactions will spatially overlap. However, the introduction of time measurements can resolve these interaction ambiguities by assigning spatially overlapped tracks to different vertices according to temporal criterion.

Typically, bunch crossings last $180 - 200 \ ps$ and occur every 25 *ns*. If one imagines slicing the beam spot into consecutive time exposure of $30 - 40 \ ps$, the number of vertices per exposure drops down to the current LHC pileup levels.

To address this and cope with the HL-LHC much harsher condition, the CMS collaboration is planning to add a dedicated timing layer, called the MIP Timing Detector (MTD). The MTD will have the ability to precisely measure Minimum Ionizing Particles (MIPs) with a time resolution of $30 - 40 \ ps$. The MTD introduction will improve the CMS tracking reconstruction performance during the HL-LHC high pileup environment [12].

1.3.1 Overview of the MTD

The design of the MTD is driven by physics and engineering requirements and constraints. Above all, the MTD must mechanically fit in the compact structure of the CMS detectors (a simplified view is presented in figure 1.6) and must not affect the other detectors efficiencies [12].



FIGURE 1.6: Simplified view of the CMS detector. Figure from [14].

The MTD will be divided into geometrical sections: a barrel and two endcaps. In particular:

- The Barrel Timing Layer (BTL) will be integrated into the support tube for the outer silicon tracker (between the Outer Tracker and the Crystal Electromagnetic Calorimeter ECAL).
- The Endcap Timing Layer (ETL) will be integrated in front of the High Granularity Endcap Calorimeter (CE).

Figure 1.7 shows a simplified view of the MTD.



FIGURE 1.7: Simplified view of the MIP Timing Detector, emphasizing with different colors the BTL and the ETL. Figure from [12].

Impact on the Performance of Other Detectors

Electron and photon energy resolution of the calorimeters is degraded by the amount of material in front of them. Therefore, the MTD must have a low material budget not to degrade the other detector resolutions. In summary, both the barrel and the endcap must be very thin.

Segmentation and Occupancy

Both the BTL and the ETL will be made of a certain number of individual active elements called *cells* or *pads*. The pad size is a compromise between the occupancy (must be less than a few percent), the sensor characteristics, and a reasonable data volume. For the BTL, a maximum per-channel area of $\sim 1 - 2 cm^2$ is suitable, while for the ETL, a single sensor size of $\sim 2 mm^2$ is suitable.

Radiation Tolerance

The higher collision rate during the HL-LHC era results in more radiation damage. A prediction of the absorbed dose of the CMS after about a dozen years of the HL-LHC era is shown in figure 1.8.

According to simulation, which produces figure 1.8, it is possible to find the expected absorbed dose for the MTD in different regions. These values are listed in the table 1.2 together with fluences normalized to 1 MeV neutron equivalent in silicon. The table considers the HL-LHC nominal design scenario, i.e., integrated luminosity of 3000 fb^{-1} after a dozen years.



FIGURE 1.8: Absorbed dose of a CMS section after an integrated luminosity of 3000 fb^{-1} . R is the transverse distance from the beamline and Z is the distance along the beamline from the interaction point. Figure from [15].

TABLE 1.2: Nominal radiation dose and fluence at various locations of the MTD after 3000 fb^{-1} . Table from [12].

Region	$ \eta $	r [cm]	z [cm]	Fluence [<i>n_{eq}/cm</i> ²]	Dose [kGy]
Barrel	0.0	116	0	$1.65 imes10^{14}$	18
Barrel	1.15	116	170	$1.80 imes10^{14}$	25
Barrel	1.45	116	240	$1.90 imes 10^{14}$	32
Endcap	1.6	127	303	$1.5 imes 10^{14}$	19
Endcap	2.0	84	303	$3.0 imes10^{14}$	50
Endcap	2.5	50	303	$7.5 imes10^{14}$	170
Endcap	3.0	31.5	303	$1.6 imes 10^{15}$	450

Radiation tolerance is a crucial parameter in the technological choice of the sensor. The validation of the sensor technology shall be conducted up to $3 \times 10^{14} n_{eq}/cm^2$ in the barrel and up to $2.5 \times 10^{15} n_{eq}/cm^2$ in the endcap to ensure a safety margin even in the ultimate HL-LHC performance scenario, i.e., integrated luminosity of $4000 \ fb^{-1}$ after a dozen years.

Sensor Technologies

The huge differences between the BTL and the ETL, especially in radiation environments and surface areas, led to different sensor technologies. The best suitable technologies are:

- for the BTL, crystal scintillators (LYSO) that are read out with Silicon Photomultipliers (SiPMs), which are pixelated avalanche photodiodes operating in Geiger breakdown mode;
- for the ETL, Low Gain Avalanche Diodes (LGAD), which are silicon sensors with an additional internal gain layer that provides a low gain.

A summary of the main characteristics of the BTL and the ETL is given in the table 1.3. This thesis work is dedicated to characterizing the silicon sensor technology suitable for the Endcap Timing Layer.

TABLE 1.3: Summary of the main features of the BTL and the ETL sections of the MTD. Table from [12].

BTL section	ETL section
Tracker/ECAL interface: $ \eta < 1.45$	In front of the CE: $1.6 < \eta < 3.0$
Inner Radius: 1148 mm (40 mm thick)	315 < Radius < 1200 <i>mm</i>
Length: $\pm 2.6 m$ along z	Position in z: $\pm 3.0 m$ (45 mm thick)
Surface $\sim 38 m^2$; $\sim 332k$ channels	Surface $\sim 14 \ m^2$; ~ 8.5 M channels
Max fluence: $1.9 \times 10^{14} n_{eq}/cm^2$	Max fluence: $1.6 \times 10^{15} n_{eq}/cm^2$

1.3.2 The Endcap Timing Layer

The ETL will be integrated in front of the future High Granularity Endcap Calorimeter (CE) and out of the Outer Tracker endcap. It will be divided into two separated assemblies, one for each side of the interaction region, at a distance of about 2.98 *m* from the interaction point. Each assembly consists of a two-disk system of MIPsensitive silicon sensors for a total active sensor area of ~ 14 m^2 [12].

A schematic view of a single assembly of the ETL is presented in figure 1.9.



FIGURE 1.9: Cross-sectional view of the ETL along beam axis. The interaction point is to the left of the image. Figure from [12].

The fill factor is the ratio between the active area covered by sensors and the total area. The sensors arrangement on opposite faces of the same disk will be made to ensure a fill factor > 85% and maximize the probability of having at least two hits for every particle trace.

The ETL will be installed in front of the CE. However, it will occupy its own independent and thermally isolated volume to guarantee the ETL to be accessible for repairs and replacements when the CMS detector is open during the shutdown.

The total amount of space required along the beam axis is 65 *mm* for each assembly: 45 *mm* of the detector and 20 *mm* of the thermal screen. Between the ETL and the CE, a neutron moderator will protect the tracker from the flux of neutrons originating from hadron interactions in the CE.

The basic unit for the ETL is the so-called *ETL module*. Each module consists of two silicon sensors bump bonded to their dedicated read-out chips, together with all the mechanical components and cooling ancillary components. A view of a two-sensor module is presented in figure 1.10.



FIGURE 1.10: A two-sensors module for the ETL. Figure from [12].

Every single pad of a sensor will be bump bonded to a single channel of a readout chip. The chip is an Application-Specific Integrated Circuit (ASIC), called Endcap Timing Read-Out Chip (ETROC), and it is being developed inside the CMS MTD project. The bump bonding yield is high but not perfect; therefore, some missing bump bonds will be present in the final modules. A pad that is not correctly bonded with the ETROC is called a *floating pad*. The final sensors have to be resilient to floating pads, i.e., their electrical characteristics should not vary to ensure correct functioning even if some pads are floating.

The assembly of the sensor and the ETROC will be protected by two Aluminum Nitride (AlN) layers. This material behaves like an electric insulator and thermal conductor: it will provide the module cooling path.

Each sensor contains a 16×32 array of $1.3 \times 1.3 \text{ }mm^2$ independent pads, where each pad is a single read-out channel. The total dimension of a sensor is $21.2 \times 42.0 \text{ }mm^2$. A schematic view of a single sensor is presented in figure 1.11.



FIGURE 1.11: Basic sensor unit for the ETL. Each sensor is made of an array of 16×32 pads. Figure from [16].

The main characteristics of the ETL can be summarized as follows:

- ETL is a new sub-detector for the CMS during the High-Luminosity Large Hadron Collider lifetime;
- ETL covers the region of pseudorapidity $1.6 < |\eta| < 3.0$;
- ETL is supposed to have a fill factor greater than 85%;
- ETL can provide temporal measurements of MIPs with a time resolution of $\sim 30 40 \ ps$;
- the sensor technology is based on Low Gain Avalanche Diodes optimized for timing and radiation hardness. Both sensors and electronics can survive at least ten years of HL-LHC.

1.3.3 Impact of the MTD on the CMS Physics Program

The CMS experimental program at the HL-LHC will benefit greatly from the increased luminosity provided by the upgrade of the LHC accelerator complex. The MTD impact on the CMS physics program at the HL-LHC has been studied in detail. The temporal information that the MTD can provide is a fundamental quantity that will lead to a precise space and time reconstruction of tracks and vertices [12].

The fundamental impacts can be divided into two categories. First of all, reducing the number of pileup interactions is beneficial for every physics channel. The final state particles and observables will be more efficiently defined from tracks and vertices collections cleaned from spurious tracks using space-time compatibility requirements. Secondly, the particle identification from MTD time-of-flight measurements provides unique opportunities in particular physics channels, such as Long-Lived Particles detection [17], Heavy Ion physics [18] and so on.

In order to better understand the improving performances of the CMS detector thanks to the MTD, it is helpful to define a new quantity called the *Line density*, defined as the number of collision vertices N_V per unit length along the beam axis z. In the actual LHC scenario, the peak density line is $\simeq 0.3 \ mm^{-1}$ with a number of pileup vertices of $\simeq 40$. In the HL-LHC scenario the peak line density will be $1.2 \ mm^{-1}$ with a pileup of 140 and $1.9 \ mm^{-1}$ with a pileup of 200 [19]. An example of vertices distribution is given in figure 1.12, together with the probability density function of the line density, from three simulations with a different number of pileup interactions.



FIGURE 1.12: On the left, distributions of the vertices along the beam direction. On the right, the probability density function of the line density: here the modes of the three distributions are respectively 0.3, 1.2 and $1.9 \ mm^{-1}$. Results are obtained with three simulations with different pileup. Figures from [19].

The current reconstruction algorithms for the hard interactions of the CMS experiment are based on a tracks and vertices compatibility cut of 1 mm. A line density greater than $1 mm^{-1}$ leads to a significant efficiency loss. The exploitation of the timing information for tracks association with hard interaction vertices is crucial to cope with this problem. In summary, thanks to the MTD time measurements, the CMS experiment can increase the luminosity but deals with line densities comparable with the actual ones.

The beneficial effects of the MTD are visible in figure 1.13. Results of simulations with different time resolutions and a different number of pileup interactions are shown from a hard primary vertex in $t\bar{t}$ events. For the MTD with 35 *ps* time resolution, the incorrectly associated tracks are reduced by about 50 %.



FIGURE 1.13: On the left number of pileup tracks incorrectly associated with hard primary vertex as a function of line density with different timing resolution. On the right the distributions of the number of incorrectly associated tracks with and without timing information. Figures from [12].

The rejection of tracks from pileup interactions will greatly impact pileup jet suppression, heavy-flavor tagging, and lepton isolation from charged tracks. Probably, this represents one of the most important MTD benefits. However, others have to be cited. The introduction of the MTD will also provide:

- Electron and photon identification from energy deposits in the MTD, because, for example, pions behave mostly as MIPs while electrons and photons are more likely to deposit large amounts of energy;
- Time-of-flight particle identification, as a direct consequence of space and timing measurement.

All the contributions of the MTD will have a strong impact of the CMS physics program. The improvement of statistical precision and background reduction will enable better physics measurements. A summary of some expected scientific impacts of the MTD is presented in table 1.4.

Signal	MTD Impact	Physics Measurements
$H \rightarrow \gamma \gamma$ and $H \rightarrow 4$ leptons	Isolation and Vertex identification	+20% precision on cross section Improve coupling measurements
HH	Isolation b-tagging	+20% gain in signal yield Consolidates searches
Electroweak SUSY	b-tagging	+40% background reduction 150 GeV increase in mass search
Long-Lived Particles (LLP)	β from timing of displaced vertices	Peaking mass reconstruction Unique discovery potential

TABLE 1.4: Summary of some expected impacts of the MTD on the CMS physics program. Table from [19].

1.4 Conclusions

The exploitation of the timing information has become a crucial topic for future HEP experiments. The MIP Timing Detector (MTD) introduction in the CMS experiment will provide this timing information. This chapter deals with the Endcap Timing Layer (ETL) of the MTD, whose active sensors are Ultra-Fast Silicon Detectors (UFSDs). This thesis work dedicates to the latest UFSD productions characterization in the following chapters.

An extensive R&D activity has been going on since the final HL-LHC decision in 2010. We are now in a crucial phase for the ETL development, particularly relative to the sensor technology finalization. In the following years, beginning from the second half of 2021, the sensor market survey will occur. Then, there will be the sensor vendor qualification and the final geometry selection. In 2022, the sensor vendor selection will occur, bringing the final choices relative to the technology. The studies conducted in this thesis contribute directly to the technological choices that define the LGAD sensors suitable for the ETL.

Finally, starting from the beginning of the year 2024, the module assembly will occur until the ETL installation in front of the CE. The BTL project will proceed on a parallel path in the same period, and the complete MTD will be ready for the HL-LHC in 2026 [12].

Chapter 2

Development of Ultra-Fast Silicon Detectors for the ETL

2.1 Introduction

The CMS collaboration chose to use Ultra-Fast Silicon Detector (UFSD) technology for the ETL [12]. UFSDs are silicon sensors based on Low Gain Avalanche Diode (LGAD) technology optimized for time resolution and radiation hardness. A timing resolution of ~ 30 *ps* is reached thanks to a combination of a low gain mechanism together with a thin thickness [20]. Another crucial aspect of UFSD is radiation tolerance because the UFSD application in the ETL will be conducted in an environment characterized by high radiation levels. As explained in chapter 1.3, the silicon sensors for the ETL should be able to work up to fluences of $2.5 \times 10^{15} n_{eq}/cm^2$.

Many groups work together worldwide to develop the UFSD technology suitable for Timing Layer applications. Torino is leading the sensor effort, with activities in sensor design, testing, and simulation of UFSD sensors.

In this chapter, the main features of the UFSD sensors are described, emphasizing the time resolution and radiation hardness. The most relevant UFSD productions are then listed, together with a detailed explanation of the latest three UFSD productions, which will be studied in the following chapter, where results will be presented. Finally, some useful tools for the sensor characterization are presented. They will be used extensively in the next chapter.

2.2 Traditional Silicon Sensor Main Features

Traditional silicon sensors are based on the *pn* junction obtained by combining a *n*-type and a *p*-type doped silicon. The region near the physical junction is depleted from free charges, and it is sensible to charged particles passage. Therefore, the *pn* junction can be used as a charged particles detector under the correct polarization, i.e., inverse polarization.

The basic operational principle of an *n*-in-*p* silicon detector is the following: an external bias voltage polarizes the *pn* junction inversely; the large depletion volume (absence of free charge) created by inverse polarization is susceptible to passage of charged particles, which creates electron-hole pairs along their paths; finally, under the influence of the electric field, the electrons drift towards the *n* contact, while the holes drift towards the *p* contact [20].

The electrons-holes drift induces a instantaneous current proportional to the electric charge q of the charge in motion, the drift velocity v and the weighting field E_w , according to Shockley-Ramo's theorem [21]:

$$i = -q\vec{v} \cdot \vec{E}_w. \tag{2.1}$$

2.2.1 The *pn* Junction Characteristic

Shockley's equation describes the ideal current-voltage characteristic of a *pn* junction. The derivation of the Shockley's equation is based on a few working assumptions such as abrupt *pn* junction, i.e., abrupt *p*-type and *n*-type silicon boundaries, and low injection assumption, i.e., injected minority carrier density is much smaller compared with majority carrier density. In this case, one can work out the total current-voltage expression [22]:

$$I(V) = I_S(e^{qV/kT} - 1), (2.2)$$

where:

- *I_S* is the saturation current in case of reverse bias: it depends upon the fundamental electric charge, acceptor-donor concentrations, acceptor-donor diffusion coefficients and junction dimensions;
- *q* is the fundamental electric charge;
- *V* is the bias voltage;
- *k* is the Boltzmann coefficient;
- *T* is the junction temperature.

The complete IV characteristic, according to equation 2.2, is shown in figure 2.1.

When the *pn* junction is used as a charged particle detector, the region of interest is the reverse polarization region: in figure 2.1 it corresponds to the region where V < 0 V.

The junction *breakdown* is a fundamental effect that must be considered in reverse bias, which is not present in equation 2.2. If the reverse voltage is too high, the internal electric field could start charging multiplication, leading to an uncontrolled avalanche. The current will blow up at a very high level, and the sensor will not work correctly. This phenomenon is known as junction breakdown and will start at a precise voltage called *breakdown voltage*.



FIGURE 2.1: Complete IV characteristic of a *pn* junction. Figure from [23].

The breakdown could be reversible but also disruptive in extreme cases. In the following sections, an example of the effect of a disruptive breakdown on a UFSD sensor is shown. Some burn marks are visible; hence, probably, a channel of free charge carrier has been created into the junction. In these cases, the sensors did not work anymore.

2.3 UFSD Main Features

Ultra-Fast Silicon Detectors (UFSDs) are silicon sensors based on Low Gain Avalanche Diode (LGAD) technology improved for timing detection and radiation hardness. LGAD design relies on a modification of the doping profile of traditional silicon sensors with an additional doping layer that creates the low gain avalanche mechanism. In the case of a *n*-in-*p* silicon sensor, the additional doping layer is obtained with a p^+ material like silicon doped with boron or gallium [20]. A traditional *n*-in-*p* silicon sensor are shown in the figure 2.2.



FIGURE 2.2: On the left, a traditional *n*-in-*p* silicon sensor. On the right, LGAD design, with an additional p^+ -layer right below the n^{++} -type silicon. Figure from [24].

The figure on the right shows the gain layer: a p^+ -layer right below the n^{++} -type silicon. The resulting doping profile with a significant increase in doping concentration near the junction creates a large electric field. In *n*-in-*p* LGAD, electrons drifting towards the n^{++} electrode initiate the charge multiplications, leading to impact ionization and consequent avalanche multiplication.

Figure 2.3 compares the electric field in a *n*-in-*p* traditional silicon sensor and a LGAD. The figure on the right shows that the gain layer is located in the first few microns: the gain enhances the electric field at values $\sim 300 \ kV/cm$, which is the lower limit to produce charge multiplication.



FIGURE 2.3: Comparison of a simulation of the electric field between a 300 μ m thick traditional silicon sensors and a 300 μ m thick LGAD sensor. Electric fields for the LGAD sensor are obtained with different bias voltages. The right figure is the same as the left figure, but the x-axis scale is logarithmic to clarify the differences between sensors. Figure from [20].

Two main aspects have to be maintained under control to ensure high timing capabilities for UFSD: gain and thickness.

The underlying idea of the UFSD development is to manufacture thin silicon sensors based on the LGAD design with the lowest gain that is sufficient to perform accurate single-particle time measurements [20].

The current signal generated by a MIP in LGAD has a rise time as long as the drift time of an electron traversing the entire sensor thickness. Its maximum current depends uniquely on the value of the gain. At fixed gain values, the signal steepness depends solely on the sensor thickness: thinner sensors have a much faster rising edge time, providing time resolution improvements. Current signals from sensors with equal gain but different thicknesses are shown in figure 2.4.



FIGURE 2.4: Current signals of three sensors with same gain but different thicknesses: thinner sensors provide littler slew rate. Figure from [24].

As visible in the figure, thin sensors achieve better time resolutions, but too thin sensors have large capacitance values that could challenge the read-out electronics. In summary, experimental results and simulations indicate as optimum performance parameters a thickness of $\sim 50 \ \mu m$ and a gain of ~ 20 [20].

2.3.1 Time Resolution

Time resolution is a crucial aspect of UFSD. A time tagging detector model should be provided to define a time resolution parametrization.

The usually considered model is shown in figure 2.5. Here, the UFSD sensor is seen as a parallel between a capacitor and a current source. The sensor signal induced by a charged particle is read-out by an electronic circuit. The first step is a preamplifier that enhances and shapes the signal. Then, the preamplifier output is compared to a threshold voltage V_{th} to determine the time of arrival t_0 , i.e., when the signal exceeds the threshold. Finally, the comparator output is digitized in a Time to Digital Converter (TDC) [20].

The particle arrival time is defined as the time t_0 when the signal exceeds the threshold. Every effect that changes the shape of the signal near the value V_{th} causes t_0 to change and, therefore, affects the total time resolution. The total time resolution σ_t of an UFSD sensor bonded to its electronics is:

$$\sigma_t^2 = \sigma_{TimeWalk}^2 + \sigma_{LandauNoise}^2 + \sigma_{Distortion}^2 + \sigma_{Jitter}^2 + \sigma_{TDC}^2.$$
(2.3)



FIGURE 2.5: Model of a time tagging detector. Particle arrival time is defined as the time t_0 at which the signal exceeds the threshold voltage V_{th} . Figure from [20].

It is possible to group the causes which influence the time resolution into four categories, according to the model in figure 2.5:

- particle energy deposition determines amplitude variations and irregularities of the signal. These are the ultimate limits to signal uniformity. Amplitude variations of the signal affect the time walk σ_{TimeWalk}, while irregularities affect the Landau noise σ_{LandauNoise};
- non-uniform weighting field and carrier drift velocity affects the signal distortion *σ*_{Distortion};
- electronic noise affects the amplifier slew rate σ_{litter};
- digitization provides the TDC resolution σ_{TDC} .

2.3.2 Radiation Tolerance

Radiation tolerance is another crucial aspect of UFSD, together with time resolution; therefore, it is still studied in detail. The main conclusion is that radiation damage causes three main effects [20]:

- decrease of charge collection efficiency;
- changes in doping concentration;
- increase of leakage current.

Decrease of Charge Collection Efficiency

The charge collection efficiency decreases because the probability of trapping during the drift of the charge carriers in the silicon bulk increases with fluence. This wellestablished effect in traditional silicon detectors does not depend on the gain layer.

Once defined the average trapping time, thinner sensors will collect most of the charges created because the average drift time will be shorter. For example, the trapping time corresponds to a distance of $\sim 50 \ \mu m$, assuming a fluence of $1 \times 10^{15} \ n_{eq}/cm^2$ and the maximum drift velocity. Therefore, only sensors up to that thickness will collect most of the charges created [20].

Changes in Doping Concentration

Changes in doping concentration are also a well-established effect in traditional silicon sensors. The radiation creates two main effects: acceptor creation by deep traps and initial acceptor (usually boron) removal. The total effect on acceptor doping N_A as a function of the normalized fluence Φ_{eq} , could be parametrized according to [20]:

$$N_A(\Phi_{eq}) = g_{eff} \Phi_{eq} + N_A(0) e^{-c(N_A(0))\Phi_{eq}},$$
(2.4)

where:

- *g*_{eff} is the coefficient that accounts for acceptor creations by deep traps;
- *c*(*N*_{*A*}(0)) is the acceptor removal coefficient which depends upon the initial acceptor doping *N*_{*A*}(0).

Before irradiation, the gain layer provides the electric field necessary to charge multiplication almost exclusively. After the irradiation, the gain layer multiplying capability starts to decrease. Measurement of gain layer disappearance effect is shown in figure 2.6, together with the collected charge in figure 2.7, which is directly correlated to the gain. The considered fluences of $1 \times 10^{14} - 3 \times 10^{15} n_{eq}/cm^2$ are around the ETL interesting ones, according to table 1.2. The red lines correspond to the optimum performance parameters of gain ~ 20 and collected charge ~ 10 *fC*.



FIGURE 2.6: Gain in a 45 μm thick UFSD as a function of the bias voltage for difference fluences. The red line corresponds to the optimum performance parameters of gain \sim 20.

At a production level, the gain reduction after irradiation could be mitigated in two ways: by using carbon enriched wafers, where the interstitials get filled with carbon instead of with boron, or by replacing Boron with Gallium. Both ways have already been explored, but it seems that carbon-enriched wafers could provide the best results.

The charge multiplication depends upon the gain layer electric field: the field is supplied both by the gain layer doping concentration and the field in bulk. Increasing the bias voltage will increase the bulk electric field and gain. Therefore a direct approach to mitigate the gain lowering is to drive the sensors at higher bias when subjected to higher radiation fluence to achieve the optimum performance gain of ~ 20 . In figure 2.6, it is visible that higher bias voltages lead to higher gain values.



FIGURE 2.7: Collected charge in a 45 μm thick UFSD as a function of the bias voltage for difference fluences. The red line corresponds to the optimum performance parameters of collected charge $\sim 10 \ fC$.

Increase of Leakage Current

The increase of the leakage current is another well-established effect in traditional silicon sensors. The observed increase in leakage current in LGADs is proportional to the increase of leakage current in traditional silicon sensors by the gain factor, which multiplies the charges generated in bulk before being collected at the electrodes. In summary, the leakage current in LGADs after irradiation follows the relation give in [25]:

$$I_{leak}(\Phi_{eq}) = G(\Phi_{eq})I_{leak,nogain}(\Phi_{eq}) = G(\Phi_{eq})\alpha\Phi_{eq}V,$$
(2.5)

where:

- *G*(Φ_{eq}) is the LGAD gain, which has a dependency upon the normalized fluence;
- *α* is a coefficient which depends upon the type of radiation particles;
- Φ_{eq} is the fluence normalized to 1 MeV neutron equivalent;
- *V* is the detector volume.

The detector should be operated at low temperatures to mitigate leakage current. The leakage current has a strong dependence upon the temperature: it is possible to find that lowering the temperature by $\sim 7^{\circ}C$ reduces the leakage current approximated by a factor of two.

2.3.3 UFSD Design

The peripheral region design is one of the main UFSD production topics. The gain layer is made of a p^+ region right under the n^{++} contact (see figure 2.2). The first is the most critical for its impact on the device gain and breakdown voltage. Proper termination of the p^+ region that can prevent premature edge breakdown is necessary [26].

A proper solution is to design a termination structure made of a deep n^+ region equipped with a metal field plate, the so-called *Junction Termination Extension* (JTE). This termination is implanted in multi-pad devices in the inter-pad area around each pad, even those not at the sensor physical edge. The reason for implementing such a protection ring around each pad is to ensure that the electron-hole pairs generated by particles hitting in between pads are not reaching the multiplication layer because it will generate a large, out-of-time signal [27].

Another patterned p^+ region called *p*-stop is used to isolate the n^+ regions.

Different designs have been studied in different productions. A section of the edge of a UFSD is shown in figure 2.8, where pixel border region design could be aggressive, intermediate, or safe according to the total width of the inactive area between the gain layers. Short width, or aggressive design, provides a high fill factor but also premature breakdown.



FIGURE 2.8: Three examples of JTE design. From top to bottom: aggressive, intermediate and safe design, with increasing gain/p-stop width. Figure from [28].

Not shown in figure 2.8, but essential for the device operation, is a set of n^+ rings, called *guard rings*, preventing early breakdown at the periphery. The n^+ rings are isolated by patterned p-stop. The first guard ring, closer to the detector core region, is biased to collect the charge carriers generated outside the detector separately, thus decreasing the leakage current [27].

2.4 UFSD Productions

The LGAD technology was first proposed and developed by *Centro Nacional de Microelectrónica* (CNM in Spain, Barcelona) in the framework of RD50 Collaboration [29]. The first LGAD measurements have been made public in a 2014 publication [30]. In 2016, CNM produced for the first time thin UFSDs and performed the first beam test on them.

Since these first results, many other research centers have developed UFSD technology. Apart from the cited CNM, nowadays, the vendors competing for the CMS ETL sensors production are two: Fondazione Bruno Kessler (FBK) in Italy and Hamamatsu Photonics K. K. (HPK) in Japan [31]. Every vendor has manufactured a certain number of R&D productions in order to explore different parameters and find the optimal ones that accommodate the CMS requests.

Every production consists of a certain number of silicon wafers. Each wafer can be different from the others according to its parameters, such as gain layer strategy or thickness. On the contrary, every wafer has the same layout. Usually, the wafer layout explores different sensor layouts, for example, single pad sensors, 2×2 array sensors, or 5×5 matrix sensors.

This work focuses on the latest productions: UFSD3.1, UFSD3.2 from FBK, and HPK2 from HPK. The following chapter deals with a detailed characterization of these productions key features.

2.4.1 Old Productions

Before the latest productions, many others have been manufactured. Every production can focus on several topics to carry on an intensively R&D on some key features of the UFSD. The main productions before the latest ones are listed below in chronological order.

- UFSD1 Production: in 2016, the first production of UFSD at *Fondazione Bruno Kessler* FBK (Italy, Trento) was completed, referred to as FBK UFSD1. The production goals were the good control of the low gain mechanism and the good correspondence between measurements and data. Since the agreements were strong, FBK moved into the next production [32].
- UFSD2 Production: in 2017 FBK completed the production referred as FBK UFSD2. For the first time, carbon was implanted together with the gain layer to study if carbon could slow down the acceptor removal mechanism by protecting the boron dopant. In this production, five of the total fifteen wafers were implanted with gallium dopant instead of boron to study if gallium could have a low probability of becoming interstitial. Both carbon addition and gallium dopant were potential solutions to enhance the radiation tolerance of UFSD devices [32], but in the following productions, gallium dopant was abandoned.
- UFSD3 Production: in 2018 FBK completed the production referred as FBK UFSD3. The main features of this production were low and high gain layer diffusion profiles, four different carbon doses, and five different gain layer doses. The aim was to explore a wide range of boron dopants and find the optimal carbon doping parameter that maximizes radiation hardness [33]. Moreover, different inter-pad designs were adopted, ranging from aggressive to safe design.
2.4.2 UFSD3.1 Production

The UFSD3 production manifested a noise very similar to the so-called *popcorn noise*, which is a noise that exhibits itself by a random step-type voltage fluctuation [34]. High voltage measurements were very noisy; hence the sensors could not be operated at the appropriate voltage [35]. A dedicated production was needed; therefore, the UFSD3.1 production was born in 2019. The principal aim was to explore a wide range of p-stop doping, which was considered the cause of popcorn noise.

UFSD3.1 production consists of 7 wafers. Each wafer has different p-stop doping. Each wafer has the same design: the reproduction of a basic reticle throughout the wafers. The basic reticle and wafer layout are shown in figure 2.9. The basic reticle is made of twelve subdivisions. There are eleven different 2×2 pads array called *types*, i.e., devices with 2×2 pads that explore different inter-pad design. The last subdivision is called *Process Control Monitor* (PCM), and it is made of simple devices such as resistance and capacitance to monitor the manufacture. The PCM is in the lower-left corner of the reticle, as visible in figure 2.9.



FIGURE 2.9: On the left, the UFSD3.1 reticle layout, made of 11×2 array types. On the right, the UFSD3.1 wafer layout: the reticle is reproduced throughout the wafer. Figures from [36].

Each type has its design that differs from the other according to inter-pad design, i.e., width between the gain layer and p-stop design. Moreover, designs can also differ in the region where the four pad corners meet, i.e., the array center. For example, some types have the four pads intersection filled with a p-stop roundabout, while others have it free.

Guard rings surround each device. The guard rings design of the UFSD3.1 production comprises four concentric guard rings: the inner one is the bias ring. The same design also holds for the UFSD3.2 production.

2.4.3 UFSD3.2 Production

The next FBK production was UFSD3.2, out in the first half of 2020. This production was born after the optimal p-stop doping from UFSD3.1 was found. The optimal value is the one that reduces the most popcorn noise. UFSD3.2 production has the same p-stop dose for every wafer and does not suffer from popcorn noise as in UFSD3 production.

UFSD3.2 production consists of 19 different wafers. The focus is to continue the carbon doping exploration to enhance radiation tolerance. Therefore every wafer could be different from the others by the carbon doping. Moreover, gain implant doping, Boron and Carbon activation, gain implant depth could also be different. Finally, this is the first production with extremely thin thickness exploration, with some wafers thick 25, 35, 45, and 55 μm .

The basic reticle layout and wafer layout are shown in figure 2.10. The basic reticle is quite similar to UFSD3.1 basic reticle, shown in figure 2.9. The main differences are that:

- of the eleven types of 2×2 pads array of UFSD3.1, only nine types of 2×2 array survived in UFSD3.2 production;
- new devices have been introduced instead of the two deleted types: an LGAD-PiN pair and a single LGAD pad with dimensions 1.3 × 1.3 mm;
- a new and larger design have been introduced: the 5×5 matrix. There are three different versions, i.e., devices with 5×5 pads that explore different inter-pad designs.



FIGURE 2.10: On the left, the UFSD3.2 reticle: the left part is quite similar to the UFSD3.1 reticle (see figure 2.9), while the right part is made of three versions of 5×5 matrix. On the right, the UFSD3.2 wafer: left side is made of 2×2 arrays, LGAD-PiN pairs and single pads, while right side is made of 5×5 matrices. Row 4, the one underlined in red, does not have gain layer.

According to Cartesian coordinates, the overall wafer could be subdivided into six rows and 18 columns. Rows and columns define a network, where every intersection defines a so-called *shot*. Every shot consists of a single half of the basic reticle, which could be the half with 2×2 arrays, LGAD-PiN pairs, and single pads or the half with 5×5 matrices. The shot number, i.e., the cartesian coordinates, is used to recognize different sensors from the same wafer during measurements. A detailed description of the wafer subdivision is presented in the following chapter.

Such as the UFSD3.1 production, the nine different types have a different design of the inter-pad region, i.e., the gain layer-gain layer distance and the p-stop design. The most interesting designs found from the UFSD3.1 production have been used for the three versions of the 5×5 matrices. The three versions are called *version* 8, *version* 9 and *version* 10. They have an increasing inter-pad width from version 8 to version 10; therefore, version 10 has the safest design. Moreover, they have a different inter-pad p-stop design, in particular:

- version 8 has a grid of p-stop;
- version 9 has independent p-stops that surround each pad;
- version 10 has the same p-stop strategy as version 9 but has an additional guard ring grid.

In figure 2.11, the p-stop strategy for the three different versions is shown. The p-stop is colored in blue, while the guard ring is colored in purple.



FIGURE 2.11: The three different p-stop strategy of the 5×5 pads devices of the UFSD3.2 production. The p-stop is blue, the guard ring is purple. From left to right: version 8 has a grid of p-stop, version 9 has independent p-stops surrounding each pad, version 10 has an additional guard ring grid respect to version 9.

All the devices of the UFSD3.2 production have the same guard rings design of the UFSD3.1 production: four concentric guard rings, where the inner one is the bias ring.

The UFSD3.2 production represents the state of art of FBK productions. Another R&D production should be defined in the second half of 2021, the UFSD4 production. UFSD4 will be the last R&D production before the CMS production; therefore, wafer parameters and sensor design will have to be finalized.

2.4.4 HPK2 Production

HPK production 2 (HPK2) is the newest production from Hamamatsu Photonics K. K. (HPK). It follows a first production called HPK1 in 2018. HPK2 sensors came in early July 2020, and the production is shared between ATLAS and CMS. HPK2 production consists in:

- 8 wafers with small devices: LGAD-PiN pairs, 2×2, 3×3 arrays and 5×5 matrices layouts;
- 8 wafers with large devices: 5×5, 8×8, 15×15 and 16×16 matrices layouts.

The small devices wafer layout is shown in figure 2.12.



FIGURE 2.12: HPK2 wafer layout. Both ATLAS and CMS prototypes are present, with 5×5 , 3×3 , 2×2 arrays or single pad.

2.5 UFSD Characterization

A UFSD sensor, as an electric device, can be fully static characterized by performing current and capacitance measures at different bias voltages. Usually, the measurements are done using device analyzers which performed the characteristics automatically. The main electrical characteristics are:

- current-voltage characteristic, or IV characteristic;
- capacitance-voltage characteristic, or CV characteristic.

It is possible to carry on a radiation damage characterization from the CV curves. The main effects of radiation damage are visible on the gain layer. The CV curves are the measurements that give direct information on the gain layer doping. Therefore, they are the best tool to evaluate radiation tolerance.

Moreover, it is possible to perform a timing resolution characterization using a radioactive font. In Torino's laboratory, a β -ray font is used to measure the time resolution. The measurements can be performed both with new and irradiated sensors. Therefore it is possible to evaluate the effect of radiation damage on the time resolution.

2.5.1 IV Characteristic

The IV characteristics performed on silicon sensor explore the reverse polarization region, like the negative bias voltage in figure 2.1. They are used basically to evaluate the breakdown voltage V_{BD} of a particular sensor, which gives information on the voltage range at which the sensor could be piloted. Knowing the V_{BD} is crucial because, when biasing the UFSD sensor, the voltage must be tuned to provide the optimum parameter of gain of ~ 20. Therefore, the sensor must reach this bias voltage avoiding the breakdown.

Moreover, the breakdown voltage is helpful to evaluate the sensor design. As mentioned before, aggressive designs lead to premature breakdown. If it happens at too low voltage, the UFSD sensor will be unusable because the gain will be too low. In summary, IV characteristics help find the optimum design, which maximizes the fill factor but provides solid sensors.

The IV characteristics for LGAD sensors and traditional silicon sensors are quite different. A *n*-in-*p* traditional silicon sensor is called *PiN*. Its behavior is exactly the one seen in figure 2.1: the leakage current fluctuates around the saturation current I_S (see equation 2.2) due to noise until the junction breakdown. In figure 2.13 two IV curves are presented: on the left, for a PiN sensor and on the right, for an LGAD sensor. Both sensors are 45 μm thick.

The gain layer presence shapes the IV characteristic of LGAD sensors: the leakage current increases exponentially. Therefore, the behavior of LGAD and PiN is different. The gain also has exponential growth as a function of the bias voltage (see figure 2.6), and it is responsible for the leakage current exponential growth in LGAD sensors.

The current compliance of the measurement blocks the exponential growth of the leakage current to avoid damaging the sensor. Usually, the apparatus compliance is $\sim 1 - 10 \ \mu A$ for new sensors and $\sim 100 \ \mu A$ for irradiated sensors.



FIGURE 2.13: Comparison between IV characteristics of a 45 μ m PiN sensor (on the left) and a 45 μ m LGAD (on the right).

In the Torino's laboratory *Innovative Silicon Sensor Laboratory*, usually the IV characteristics are measured with a semiautomatic probe station and a *Device Analyzer Keysight B1500A*, using the setup in the figure 2.14. The Source Module Units (SMUs) could give voltage to the sensor and measure the corresponding current.



FIGURE 2.14: IV characterization setup. Figure from [37].

2.5.2 CV Characteristic

The CV characteristics are the other fundamental tool for sensor characterization. A measure of the capacitance at different bias voltage is used to evaluate the gain layer depletion voltage V_{GL} and the full depletion voltage V_{FD} . These values provide helpful information about the gain layer doping, gain layer depth, and sensor depletion.

The doping concentration of the gain layer is proportional to the V_{GL} : $V_{GL} \alpha N_{A,GL}$. Moreover, the initial capacitance at low voltage (for example, the capacitance around 10 V) is an indication of the depth of the gain layer. For example, assuming the same area and same doping for two sensors, a lower capacitance indicates a deeper gain layer [38]. Both gain layer and full depletion voltage can be visualized and extracted using a CV curve. In figure 2.15 two CV are presented, both for a PiN and for an LGAD 45 μm thick sensor.



FIGURE 2.15: Comparison between CV characteristics of a 45 μ m PiN sensor (on the left) and a 45 μ m LGAD (on the right).

The CV curve for a PiN sensor immediately exhibits a strong fall-off until an asymptotic value. The full depletion voltage for a PiN sensor is proportional to bulk doping $N_{A,bulk}$: $V_{FD} \alpha N_{A,bulk}$). Bulk doping is widely lower than gain layer doping, namely $N_{A,bulk} \simeq 10^{12} a toms/cm^2$ against $N_{A,gainlayer} \simeq 10^{16} a toms/cm^2$. Therefore, full depletion in PiN sensors will come earlier.

As opposed to PiN sensors, the CV curve for LGAD sensors decreases slowly, then exhibits a substantial fall-off. The voltage at which the knee appears is where the gain depletes, namely V_{GL} . After this value, the CV curve quickly reaches an asymptotic value revealing a lightly doped bulk [38].

It is interesting to find in the figure 2.15 that the final capacitance after the full depletion is equal for both PiN and LGAD sensors. This happens because the sensor could be approximated with a parallel plate capacitor, hence the capacitance depends only upon the dimensions according to:

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d},\tag{2.6}$$

where:

- $\varepsilon_0 = 8.85 \times 10^{-12} F/m$ is the vacuum dielectric constant;
- $\varepsilon_{Si} = 11.7$ is the silicon relative dielectric constant;
- *A* is the sensor area;
- *d* is the depletion layer thickness.

Once the sensor is completely depleted, the depletion layer thickness is the total sensor thickness. The capacitance reaches the asymptotic value C_{FD} , which is the full depletion capacitance. The measured sensors, from whom figure 2.15 is taken, have both $A = 1.3 \times 1.3 \text{ mm}^2$ and $d = 45 \mu m$, hence $C_{FD} \simeq 4 pF$.

It must be added that depletion voltages could be easily visualized using $C^{-2}V$ curves. It descends from the equation 2.6. In fact, the depletion layer thickness is obtained from:

$$d = \sqrt{2\epsilon\mu_e\rho V},\tag{2.7}$$

where:

- $\varepsilon = \varepsilon_0 \varepsilon_{Si}$ is the total dielectric constant;
- μ_e is the electron mobility;
- $\rho = \frac{1}{e n_i(\mu_e + \mu_h)}$ is the resistivity, where *e* is the electron charge, n_i is the intrinsic carrier density and μ_h is the holes mobility.

Putting together equation 2.6 and equation 2.7, one obtains:

$$C^{-2} = \frac{\rho \mu_e}{\varepsilon A} V. \tag{2.8}$$

In summary, $C^{-2} \alpha V$, where the angular coefficient is related to resistivity. In the gain layer, the intrinsic carrier density is higher than the bulk; hence, resistivity is lower. It means that $C^{-2}V$ curve will be made of two straight lines, one corresponding to gain layer depletion with a very low angular coefficient, the other corresponding to bulk depletion, with a very high angular coefficient. Finally, after the complete sensor depletion, the capacitance is constant; therefore, a final horizontal straight line will be present. An example of $C^{-2}V$ curve is shown in the following chapter.

In Torino's laboratory *Innovative Silicon Sensor Laboratory*, usually, the CV characteristics are measured with a manual probe station and a *Device Analyzer Keysight B1500A*, using the setup in the figure 2.16. The Capacitance Module Unit (CMU) produces a sinusoidal wave propagating in the sensor. Knowing the wave frequency and measuring the amplitude and the phase shift of the incoming wave, the device analyzer can calculate the total sensor impedance, hence the sensor capacitance.



FIGURE 2.16: CV characterization setup. Figure from [37].

CV characteristics could also be measured with the quasi-static capacitancevoltage (QSCV) method. As its name suggests, the capacitance characterization uses a quasi-static method based upon the charge-capacitance-voltage relation Q = CV. The total amount of charge Q can be expressed by the current I integrated for a time interval Δt as $Q = I\Delta t$. It follows that:

$$C = \frac{Q}{V} = \frac{I\Delta t}{V} = \frac{I}{\Delta V / \Delta t}.$$
(2.9)

Therefore, capacitance *C* could be obtained from a *I* measurement, for example, using a linear voltage ramp. This method is a traditional QSCV method: it simply applies the voltage at a fixed ramp rate $(\Delta V / \Delta t)$ and measures the current *I* [39].

For some UFSD sensors, especially those with very high radiation fluence, a simple CV cannot be performed to extract the capacitance-voltage characteristic. CV measure has a dependency on the sinusoidal signal frequency used to calculate the capacitance. In such cases, the frequency must be shallow, and the measure will not be precise; therefore, a QSCV method should be preferred.

QSCV is very sensitive to leakage current and current noise. A large leakage current requires a considerable time of integration and could lead the measure to fail, while current noise spikes could produce capacitance overflow and lead the measure to fail. High-irradiated sensors have high leakage current ($\sim 100 \ \mu A$); therefore, this method seems inappropriate. In reality, the device analyzer provides some tools to compensate leakage current, for example, by placing another SMU on the sensor, which is only dedicated to compensating the leakage current by measuring it before and after the time integration and subtracted from the current measurement. In summary, a QSCV is often feasible also on high irradiated sensors.

The QSCV setup is the same as figure 2.14: two SMUs provide the bias voltage linear ramp $\Delta V/\Delta t$ and measure the current *I*. With this setup, some QSCVs were performed. An overlap between data obtained from High-Frequency CV (the standard CV) and quasi-static CV is shown in figure 2.17. One may notice that data from different methods lead to consistent measurements.



FIGURE 2.17: Overlap of data obtained from High Frequency CV and Quasi-Static CV.

2.5.3 Beta Source Characterization

The time resolution is a key feature of the UFSD technology; therefore, its measurements occupy a central role in the characterization. In Torino's laboratory *Innovative Silicon Sensor Laboratory*, a beta source is used for the time resolution σ_t measurements. Moreover, the characterization with a beta source could provide a series of detailed measurements on other UFSD key features, such as:

- gain versus bias voltage curves, such as the ones shown in figure 2.6;
- charge versus bias voltage curves, such as the ones shown in figure 2.7.

The beta source characterization is carried on with a ${}^{90}Sr$ source. The experimental setup is made of a silicon sensors telescope, with a reference and well-known UFSD aligned with the Device Under Test (DUT), i.e., the UFSD sensor that needs to be measured. Both sensors are bounded with read-out boards, which provide the bias voltage and allow the signal to be read. An oscilloscope reads out the boards with a high sampling rate; hence the σ_{TDC} in the equation 2.3 is minimized. The beta source particle signals that cross the UFSD sensors are stored as digital file events on the oscilloscope.

The data analysis is based on an algorithm called Constant Fraction Discriminator (CFD), which defines the event time as when the signal crosses a constant fraction on the maximum amplitude. The choice of this algorithm limits the time walk, which is the $\sigma_{TimeWalk}$ in the equation 2.3.

Chapter 3

Characterization of the Latest UFSD Productions

3.1 Introduction

During my thesis, I worked on characterizing the latest Ultra-Fast Silicon Detector productions from FBK and HPK. These productions explore different inter-pad designs to find the best pad isolation strategy. A relevant part of the work focused on comparing the different inter-pad designs under aspects such as the robustness to high voltage, the resilience to floating pads presence, and the inter-pad resistance.

The first section reports the characterization of the FBK UFSD3.2 production based on the IV and CV measurements on all the wafers. The focus is on the wafer uniformity of the breakdown voltage, the leakage current, and the full depletion voltage. Other interesting parameters are extracted, such as the type inversion of the wafer substrate and the breakdown voltage as a function of the wafer thickness. Finally, a bad pads count method is introduced, and the yield is measured.

The second section reports the device behavior study with one or more floating pads. As mentioned in section 1.3.2, the presence of floating pads in the final ETL modules is inevitable because the bump bonding yield is not 100%. The sensor resilience to floating pads is a crucial topic for the ETL application. The study is carried out with 2×2 arrays of the UFSD3.2 and HPK2 productions.

The third section reports the study of the isolation of the pads. This characterization is performed by measuring the inter-pad resistance, which should be high to avoid charge dispersion. The method followed for such measurements is explained, together with a study of the dependency upon the operating conditions of the device. The study is carried out with 2×2 arrays of the UFSD3.1 and HPK2 productions.

3.2 Characterization of the UFSD3.2 Production

Fondazione Bruno Kessler (FBK) provides IV and CV measurements on a large fraction of devices for all the wafers of its productions. This large amount of data can be analyzed to extract useful information, such as:

- breakdown uniformity;
- leakage current uniformity;
- gain layer uniformity;
- the fraction of pads that do not hold the operating voltage;
- the fraction of noisy pads;
- superficial density of catastrophic defects;
- uniformity of carbon implant.

Some of these performance parameters are extracted on the UFSD3.2 production, the latest FBK production, in the following sections.

The UFSD3.2 production consists of small devices compared to the final ETL sensor, which will be a matrix of 16×32 pads, as mentioned in section 1.3.2. The different devices are very useful in evaluating aspects of the production relevant for the final matrix. Devices such as single pads, 2×2 array, and 5×5 matrices have been using to evaluate several aspects. For example, the different approaches to pad isolation have been evaluated with 2×2 arrays, which have been produced with different inter-pad designs. On the other hand, pads and sensors yield has been evaluated with 5×5 matrices.

3.2.1 The UFSD3.2 Data Sample

FBK performed measurements of IV and CV characteristics at wafer level on most of the UFSD3.2 production. The measurements have been performed right after the production and before the sensors were diced. The measurements were carried out using a probe card with automatic movements.

As mentioned in section 2.4, the UFSD3.2 production consists of 19 wafers. Each wafer is subdivided into a certain number of units called *shots*, labeled following the Cartesian coordinates. The wafer layout results from the composition of devices derived from two reticle shots hosting different sensor types. The reticle shots are:

- shot A with nine different types of 2×2 array sensors, LGAD-PiN pair sensors, and single pad LGAD sensors;
- shot B with three different versions of 5×5 matrix sensors. The term *version*, instead of *type*, is here used to distinguish 5 × 5 from 2 × 2 devices.

It is useful to separate the shot A devices into two categories when performing the characterization: shot A.1 and shot A.2. The three shots are shown in figure 3.1, together with the type or version number. Sensors from shot A.2 are called *P_PAD*, *P_PiN* or *A_PAD*, respectively for LGAD sensor from LGAD-PiN pair, PiN sensor from LGAD-PiN pair, LGAD sensor in single layout $(1.3 \times 1.3 mm^2)$.

One may notice a square in the left-down part of shot A that takes no place in the device definitions. As explained in section 2.4, it is called Process Control Monitor (PCM), and it is used to monitor the manufacture.



FIGURE 3.1: Three UFSD3.2 shots are shown: on the left shot A.1 made of nine types of 2×2 array; in the middle shot A.2, made of LGAD-PiN pair and PAD 1.3 *mm*; on the right shot B, made of three versions of 5×5 matrix.

The set of the device name, wafer number, shot coordinates, and type (or version) number is unique for every sensor of the UFSD3.2 production. Figure 3.2 shows an example of sensor identification. The chosen sensor is:

- shot B, on the right half of the wafer with 5×5 matrix sensors;
- shot coordinates (2,4), i.e., column 2 (yellow in figure) and row 4 (red in figure);
- version V10, i.e., the upper version of the 5×5 basic reticle (see figure 3.1).



FIGURE 3.2: Example of identification of a UFSD3.2 sensor. The sensor (orange) is from: shot B, the right half of the wafer; column 2 (yellow) and row 4 (red); version V10, i.e. the upper version.

3.2.2 Description of Analysis Framework

A large amount of data from FBK have been manipulated with software. During my thesis, I wrote an analysis software using *C*++ code with *ROOT CERN* framework classes, which can perform some valuable analyses.

The software could be divided into three main steps, starting from the measurements performed by FBK. First of all, the text files (i.e. *.txt* files) have been converted in so-called *root tree* files (i.e. *.root* files), which are easier to manipulate. A root tree is a *ROOT CERN* class that allows the storage of a large quantity of same-class objects in a way such as to optimize disk space use and access speed [40].

Five conversion macros have been written to produce five root tree files. Given different structures of IV and CV text files and shots A.1, A.2, and B, the measurements have been organized as listed below:

- the tree containing IV data of shot A.2;
- the tree containing IV data of shot A.1;
- the tree containing IV data of shot B;
- the tree containing CV data of shot A.2;
- the tree containing CV data of shot A.1.

The five root trees are examined in the following sections in the same order as they appear in the list. The analyses on the root tree files have been developed to address the uniformity studies and the inter-pad comparison. FBK did not measure the CV characteristics on shot B.

The UFSD productions for the ETL must satisfy high yield and uniformity requirements. The dimension of the final sensors for the ETL will be larger than all the devices characterized in this chapter: CMS will have sensors of 16×32 pads of active area $1.3 \times 1.3 \text{ mm}^2$. Therefore, it is fundamental that the yield and uniformity of production are as high as possible, i.e., the working properties of each sensor and each pad must be as similar as possible. The uniformity studies are fundamental because they allow quantifying the capability of FBK to produce large sensors with the same characteristics. A qualitative way to visualize the uniformity results is through two-dimensional histograms, in which a particular quantity is plotted on the wafer. Instead, a quantitative analysis relies on the extraction of mean and standard deviation from the Gaussian distributions of a certain quantity. The quantities under investigation are breakdown voltage, leakage current, and full depletion voltage.

The inter-pad studies have been performed to evaluate the best inter-pad strategy, i.e., which type (or version) is the best. The optimum design is the reasonable compromise between fill factor and robustness to high voltage; therefore, breakdown voltage provides very useful information.

3.2.3 Analysis of the IV Characteristics

The IV characteristics from FBK provide useful information about the sensor breakdown and the sensor leakage current. Both of them can be used to evaluate wafer uniformity and inter-pad design.

The first step is to convert IV text files into root tree files. Then, using the macros of the software plot section, each IV curve for a specific device is plotted, obtaining a plot similar to figure 2.13. Finally, the analysis is performed.

The analysis is based on the breakdown voltage extraction from each IV curve. Breakdown leads to an uncontrolled current flow, which is stopped only by the apparatus compliance, i.e., the maximum current that the measurement apparatus can provide. There is a simple way to define the breakdown voltage: the voltage at which the compliance is reached. A series of interesting plots are shown and explained in the following sections, based on the breakdown voltage extraction.

The breakdown uniformity on a wafer is presented as a two-dimensional histogram wafer map, where the breakdown voltage value is encoded using color. Instead, a box plot has been used to compare the inter-pad design behaviors. A box plot is a method for graphically depicting numerical data groups through their quartiles. In this case, the breakdown voltage distribution is shown as a function of the sensor type.

Another interesting way to evaluate the wafer uniformity is to study the current distributions: a wafer map is produced displaying the current at a fixed voltage, again encoded using color.

IV Curves of 2×2 Arrays

The shot A.1 includes nine 2×2 arrays called *types*, as already mentioned in the previous sections. Different inter-pad designs characterize each type.

Devices of shot A.1 have been measured using a setup with five SMUs and an HV module in a way similar to figure 2.14. HV module is connected to the sensor backplane, and the SMUs are connected to each of the four pads and the guard ring. The HV module polarizes the sensor inversely and measures the total backplane current flowing into it. The four pads and the guard ring currents are measured concurrently by the SMUs.

All IV curves are traced, obtaining a large number of plots. One of these plots is shown in figure 3.3 as an example. Guard ring current, called *IGR*, and total current (backplane current), called *IBACK*, are also plotted, each curves with a different color.

The breakdown voltage value V_{BD} is extracted from each plot as the voltage at which the total backplane current reaches the compliance $I_{cmpl} = 10 \ \mu A$. In figure 3.3, one may notice that pad 1, IP1 in orange, causes the breakdown of the device. A pad that leads the total current to compliance before the others should not necessarily be identified as a bad pad. A tiny spread of breakdown voltages among the four pads must be considered, as the production uncertainties bring to slight differences between pads. It is visible from figure 3.3 that the other pad currents, IP2, IP3, and IP4, are, in any case, close to breakdown: one can imagine that the breakdown would have occurred in a few voltages due to another pad. A criterion to evaluate if a pad is bad is given in the following sections.



FIGURE 3.3: Example of a IV curve of a UFSD3.2 shot A.1. The selected sensor is: wafer 12, shot (8,8), type 10; with $V_{BD} = 425 V$.

Evaluation of the Breakdown Voltage Uniformity on 2×2 Arrays

From figure 3.3, one can extract the breakdown voltage value of the device. As explained above, compliance is always set on the HV module. The breakdown voltage V_{BD} is extracted from the total backplane current, and, therefore, it is unique for every sensor.

Figure 3.4 shows an example of a wafer map. The breakdown voltages of all the 2×2 devices are visualized according to the shot (x,y) coordinates.



FIGURE 3.4: Breakdown voltage map of wafer 12, shot A.1. The voltage scale is shown on the right.

The breakdown voltage value is encoded using color: higher breakdown voltage corresponds to a brighter color, while lower breakdown voltage corresponds to a darker color. The voltage scale is shown on the right side of the plot. The maximum value is 500 V, as this is the upper limit set during the measurements at FBK. Some helpful information can be obtained by looking at the map of figure 3.4. In row 1, some sensors are broken, as they show a very premature breakdown voltage, the ones in deep blue color. This effect is reproduced on every wafer. All the devices near the wafer border have a high probability of being broken, showing a very premature breakdown. This fact is related to the manufacturing of the sensors. During the production, wafers typically undergo many lithography steps, etching processes, i.e., processes that use strong acid to remove some parts of metal, and heating processes. Every step has its precision and could lead to uncertainties in the production. These uncertainties are broader near the wafer periphery. For this reason, every vendor defines a *safe zone*, which is the region delimited by the green circle shown in figure 3.2, which should be considered as the effective area of the wafer. The green circle area and the region close to it do not guarantee proper functioning sensors.

Another interesting feature of this map is that quite different breakdown voltages characterize the sensor types. For example, type 10 has a higher breakdown voltage than the others on average: this type is colored more often in a brighter color. Type 10 has a very safe design and has a guard ring grid added between pads (see section 2.4), making this design very robust. The topic of the inter-pad design is further detailed in the following sections.

Finally, one may notice that in row 4, the breakdown voltage values tend to be slightly higher: all sensors in this row are PiN sensors, with no gain layer, as in all the other wafers of the production, see figure 2.10. This fact is visible by looking again at type 10, which is always bright yellow in row 4. Other types are less robust to high voltage and show premature breakdown, which happens at a voltage where the gain layer contribution to the current is not yet significant: this explains why the color of other types is quite the same both for PiN and for LGAD sensors.

The distributions of breakdown voltages are presented using box plots. These plots show the mean of the distribution as a circle, the median as a straight horizontal line, the upper and lower quartile (respectively values that delimits 75% and 25% of data points) as top and bottom of a box, the highest and lowest value as top and bottom whiskers [40]. Figure 3.5 shows the breakdown voltage distributions as a function of the type for LGAD sensors of wafer 12. The sensors which breakdown is $V_{BD} < 50 V$ are considered *broken* and are discarded from the plot.



FIGURE 3.5: Box plot of breakdown voltage as a function of the type for LGAD sensors (all the rows except row 4) of wafer 12.

This figure shows wide distributions, even if sensors with $V_{BD} < 50$ V are discarded. Moreover, each type, except type 2, 9, and 11, shows asymmetrical distributions, with bottom whiskers at very low voltage. The explanation is visible from figure 3.4. Some sensors from rows 1 and 6 (also row 5 for other wafers) have not been considered broken because they have $V_{BD} > 50$ V. However, they are surely damaged because they show a breakdown voltage lower than the same types in rows 2 and 3. A refined analysis must also discard these sensors because they are related to production issues. Damaged sensors, if present, will be discarded in the final matrix production and, therefore, do not contribute to the definition of uniformity.

The uniformity of the breakdown voltage V_{BD} has been studied by evaluating the mean $\langle V_{BD} \rangle$ and Root Mean Square RMS_{BD} of the collected breakdown voltages. The ratio $R_{BD} = RMS_{BD} / \langle V_{BD} \rangle$ is taken as an indication of the uniformity of the breakdown voltage. Both broken and damaged sensors must be discarded. Therefore, sensors with $V_{BD} \langle 50 \rangle$ and rows 1, 5, and 6, are excluded from the analysis. Only six wafers are considered because they have a large number of measurements, a few dozens for each type. Among them, only type 10 is considered because it always has the highest breakdown. Table 3.1 shows the founded values.

TABLE 3.1: Ratio $R_{BD} = RMS_{BD} / \langle V_{BD} \rangle$ for six wafers and for type 10 of LGAD sensors of UFSD3.2 shot A.1.

Wafer	$< V_{BD} > [V]$	$RMS_{BD}\left[V\right]$	R _{BD}
Wafer 4	252	17	$(6.7 \pm 0.9)\%$
Wafer 7	292	22	$(7.7 \pm 0.9)\%$
Wafer 8	431	29	$(6.7 \pm 0.9)\%$
Wafer 10	367	5	$(1.3 \pm 0.4)\%$
Wafer 12	396	42	$(10.6 \pm 1.1)\%$
Wafer 14	294	12	$(4.1\pm0.7)\%$

The mean of the ratios gives a final uniformity parameter for the breakdown voltage of $\simeq 6\%$. This value indicates a high uniformity, and it is satisfactory in the current point of research and development. In the final production of the ETL sensors, the vendor will increase the uniformity. These values are also consistent with those found in the next sections regarding leakage current uniformity and full depletion uniformity.

Comparison of Inter-pad Designs with 2×2 Arrays

As already mentioned in section 2.4, shot A contains nine different types of 2×2 array, which differ for the pad isolation structures design. The best way to perform a comparative study of the design behavior and robustness is using PiN sensors, i.e., sensors without gain layer.

Figure 3.6 shows a box plot with the breakdown voltage distributions as a function of the sensor type. Only PiN sensors from wafer 12 are considered, discarding the ones with $V_{BD} < 50 V$.



FIGURE 3.6: Type comparison using box plots of UFSD3.2 sensors from wafer 12 only PiN sensors (from row 4).

Again, the plot shows that type 10 has the highest breakdown, thanks to its robust design. Other types with higher V_{BD} are type 4 and type 8, while types with lower V_{BD} are type 2, 1, and 11. In general, there is a close relationship between inter-pad width and breakdown voltage. Types 1 and 2 have the smallest gain-gain width, and they have the lowest breakdown voltages. However, the inter-pad width is not the only parameter that determines the robustness of a certain type, but also the design strategy implemented by FBK has to be considered. These studies are very valuable feedback to the design engineer.

Evaluation of the Leakage Current Uniformity on 2×2 Arrays

Another way to analyze the production uniformity is to study the leakage current uniformity. The basic idea is to extract each pad current at a fixed voltage and create a two-dimensional map to display all the values on the wafer. Figure 3.7 shows a current map of the wafer 4, together with its breakdown voltage map. The current values are taken at 50 *V*.



FIGURE 3.7: Comparison between UFSD3.2 wafer 4 current map at 50 *V* on the left and breakdown voltage map on the right. A correspondence between sensors with premature breakdown and sensors with high current could be found.

A current map can also help to identify the presence of bad pads. A *bad pad* may be defined using both sensor breakdown and pad current. A bad pad leads to a premature breakdown and has a current higher than device other pads. For example, one can define a *bad pad* as having $V_{BD} < 50$ V and $I_{pad} > 10 * I_{neighbors}$. Should we use this definition, the counting of bad pads would be inaccurate. After the sensor reaches the current compliance, no more data are registered. If the voltage at which the current map is plotted (here 50 V) is higher than the sensor breakdown voltage, the entire device will have no data at such a voltage. The map will enable identifying the bad pads which induce a breakdown at a voltage higher than 50 V.

The probability of having a bad pad is better investigated using 5×5 matrices in the following sections because a larger layout and different way to measure IV lead to more significant results.

The direct comparison between the current map and breakdown voltage map, like in figure 3.7, allows noting a certain correspondence between pads with high current and devices with premature breakdown. Pads with higher current are colored in brighter yellow in current maps, while sensors with premature breakdown are colored in darker blue in breakdown voltage maps (see, for example, shot (10,6)).

The current values at a certain voltage have been collected in one-dimensional histograms. The current distribution of each wafer follows a Gaussian distribution when the broken and damaged sensors are discarded. As already did for the break-down voltage uniformity, the sensors with $V_{BD} < 50 V$ and the rows 1, 5, and 6 are not considered in the following analysis.

Figure 3.8 shows an example of currents distributions at 100 *V* for wafer 12. On the left, LGAD sensors, and, on the right, PiN sensors. There is no reason why the leakage current should vary with the type designs, in contrast to breakdown voltage (confirmed in figure 3.7); therefore, all types are placed together. The distributions are fitted with a gaussian function, shown in red.



FIGURE 3.8: UFSD3.2 shot A.1 wafer 12 current distributions at 100 *V*. On the left, the LGAD currents; on the right, the PiN currents.

The Gaussian fit gives the mean μ_I and the standard deviation σ_I of the current distributions. The current uniformity can be quantified by calculating the ratio $R = \sigma_I / \mu_I$. As already did for the breakdown voltage uniformity, only six wafers are considered here. The table 3.2 shows the resulting ratios at 100 *V*.

	UFSD3.2 shot A.1.		
Wafer	R _{LGAD}	R _{PiN}	

TABLE 3.2: Ratio σ_I/μ_I for each wafer of LGAD and PiN sensors of

Wafer	R _{LGAD}	R _{PiN}
W4	$(14.4 \pm 2.1)\%$	$(30 \pm 9)\%$
W7	$(11.9\pm1.4)\%$	$(24\pm6)\%$
W8	$(5.5 \pm 0.3)\%$	$(30\pm9)\%$
W10	$(5.9\pm0.3)\%$	$(26\pm7)\%$
W12	$(5.5 \pm 0.3)\%$	$(33 \pm 11)\%$
W14	$(12.7 \pm 1.6)\%$	$(32\pm10)\%$

The LGAD values are of the same order of magnitude ($\sim 5 - 15\%$) of the ratios found for the breakdown voltage uniformity studies and confirm that the UFSD3.2 have high uniformity, both for breakdown voltage and leakage current. Analogous results were obtained on the UFSD3 production (see [41] and [42]).

The ratios for PiN sensors are about double the ratios for LGADs. This can be related to the lower currents of the PiN sensors. For example, by looking at figure 3.7, the mean of leakage current for PiNs (row 4) is about two order of magnitude lower than LGADs: $\sim 10^{-12} A$ against $\sim 10^{-10} A$.

Type Inverted Wafers on 2×2 Arrays

Type inversion of the silicon bulk of a wafer is a phenomenon that can happen during sensor production processes. The bulk of a *n*-in-*p* UFSD is made of silicon poorly *p*-doped with acceptor atoms, see figure 2.2. When type inversion occurs, the bulk becomes poorly *n*-doped.

UFSD3.2 sensors were produced using epitaxial growth, where a very pure silicon deposition grows on a bearing layer of a handle wafer of not very pure silicon. Type inversion in UFSD3.2 sensors probably happened because of oxygen diffusion from the handle wafer to the sensor bulk. Since oxygen defects in silicon behave like n defects, a too poorly p-doped bulk can lead to a type inversion.

The type inversion is not a problem in itself because sensors work correctly. Moreover, when irradiated, type inversion happens again, bringing back the bulk to *p*-doping [43]. However, it is essential to know which wafer is type inverted to consider the side effects. One of these is the increase of the guard ring leakage current up to $\sim \mu A$ against $\sim nA$ of non-type inverted sensors. The guard rings are *n*-type implants inside *p*-doped silicon, and they act as a local *pn* junction, collecting the local depletion voltage charges. When type inversion occurs, the guard rings act like *n*-implants inside *n*-doped silicon; therefore, they collect charge generated from all bulk, increasing their currents.

A study was carried out to find which wafers are type inverted and find whether type inversion was occurring everywhere. Figure 3.9 shows the comparison of the guard ring leakage current for wafer 7 and wafer 4, plotted as a function of the shot number at 30 *V*.



FIGURE 3.9: Guard ring leakage current at 30 V against wafer shot number: comparison between wafer 4 and wafer 7.

One may notice that guard ring currents of wafer 4 are higher than the same currents from wafer 7: wafer 4 is type inverted, while wafer 7 no. It was possible to find that every wafer of the UFSD3.2 production is type inverted except wafer 5, 7, 9, and 15. Moreover, it is confirmed that a type inverted wafer is type inverted everywhere. CV curves on type inverted sensors are complicated to interpret because an *n* bulk leads to several *pn* junctions through the sensor height. Therefore, FBK decided to measure CV curves only on non-type inverted wafers using the information obtained with this study.

Thickness Studies on 2×2 Arrays

The behavior of sensor types at different thicknesses is another interesting topic studied. As mentioned in 2.3, the thickness is crucial in UFSD production. Thickness shapes the signal (see figure 2.4), and, in general, thinner silicon sensors have better time resolution. Very thin sensors look promising, especially to cope with high irradiation fluence, up to $10^{16} - 10^{17} n_{eq}/cm^2$ [44].

UFSD3.2 production is the first production that explored very thin thickness, up to 25 μm . Wafers 1, 5, 6, and 7 have the same parameters of gain doping concentration and carbon dose, but they have increasing thickness: wafer 1 is 25 μm thick, wafer 5 is 35 μm , wafer 6 is 45 μm and wafer 7 is 55 μm .

Figure 3.10 shows the average breakdown voltages of the various types as a function of the wafer active thickness for wafers 1, 5, 6, and 7.



FIGURE 3.10: Breakdown voltage of different sensor types against wafer thickness: wafer 1 is 25 μm , wafer 5 is 35 μm , wafer 6 is 45 μm and wafer 7 is 55 μm .

Some interesting conclusions arise from this plot. First of all, it is confirmed that type 10 always has the highest breakdown. Secondly, the breakdown has a strong dependence on sensor thickness. At a first approximation, a silicon sensor could be seen as a parallel plate capacitor. The average electric field *E* inside a parallel plate capacitor is:

$$E = \frac{V}{d},\tag{3.1}$$

where V is the potential between the two plates and d is their distance. The same electric field is reached at lower voltages for smaller distances.

The value of the electric field is responsible for junction breakdown; therefore, a smaller thickness corresponds to a smaller voltage applied to reach the junction breakdown. One should expect a linear dependence between breakdown voltage and sensor thickness: this seems well reproduced by data. There is a bias in the measurements done at FBK, as the maximum voltage allow was 500 *V*. For this reason type 10 seems to depart from the linear behavior at higher sensor thicknesses.

Evaluation of the Breakdown Voltage Uniformity of Single Pads

Some of the analyses made for 2×2 arrays have been repeated on shot A.2, which comprises three sensors: an LGAD-PiN pair and a single LGAD pad. Both breakdown voltage maps and box plots have been used to study the breakdown voltage uniformity.

IV characteristics of each sensor were measured independently by connecting with two SMUs and one HV module similar to figure 2.14. The HV module measured the total backplane current flowing into the sensor, which is the sum of the pad current, measured by one SMU, and the guard ring current, measured with the other SMU. As an example, figure 3.11 shows two IV characteristics of the LGAD sensor (from the LGAD-PiN pair) of shots (8,2) and (8,1) of the wafer 4. The sensor on the right side of the plot is not working correctly, as it shows a premature breakdown of $V_{BD} = 35 V$.



FIGURE 3.11: Two IV curve plots of shot A.2. On the left, of a correctly working sensor: LGAD from LGAD-PiN pair, wafer 4, shot (8,2) ($V_{BD} = 265 V$). On the right, a badly working sensor: LGAD from LGAD-PiN pair, wafer 4, shot (8,1) ($V_{BD} = 35 V$).

All the breakdown voltages of the shot A.2 devices have been extracted and displayed on a two dimensional map. Figure 3.12 shows the map of the wafer 4.



FIGURE 3.12: UFSD3.2 shot A.2 wafer 4 breakdown voltage map.

The breakdown voltage map done for shot A.2 devices complements the information given by the map of the 2×2 devices. As expected, all the PiN sensors have higher breakdown voltage than LGAD sensors. This can be seen on the map in every shot (PiN sensor of the LGAD-PiN pair) or in row 4, which does not have the gain layer.

As for 2×2 devices, row 1 shows a premature breakdown, which is visible from every wafer.

The direct breakdown voltage comparison is shown in figure 3.13 for wafer 4, both for sensor from row 4 (on the right) and for sensor from every row except row 4 (on the left). All the sensors with $V_{BD} < 50$ V have been neglected.



FIGURE 3.13: Breakdown voltage comparison using box plots of UFSD3.2 sensors from wafer 4. On the right, only sensors from row 4, on the left, only sensors from all rows except row 4.

PiN sensors from LGAD-PiN pairs have a wider spread breakdown voltage according to their position. In other words, breakdown voltage distribution of PiNs from row 4 is wider than distribution of PiNs from the rest of the wafer. This effect is unexpected because PiN sensors should be equal. An explanation could come from broken sensors in rows 1 and 6. Eliminating row 1 and row 6 from the box plots and confronting again, the breakdown voltage of the two sets of PiNs are now consistent.

The breakdown voltage values for single LGAD pads and LGADs from the LGAD-PiN pair are consistent. These values are greater than the mean of the breakdown voltage of the most robust type of 2×2 array, which is the type 10, of \sim 50 – 100 *V*. The guard ring structures are the same for each device, but 2×2 arrays also have inter-pad structures, which weaken the sensor robustness; therefore, one expects a lower breakdown voltage. This is confirmed by comparing the breakdown voltage distributions of shot A.1 and shot A.2, for example figure 3.5 with figure 3.13.

IV Curves of 5×5 Matrices

The conversion software produces a tree containing all IV curves of shot B from all the wafers. Shot B contains three 5×5 matrices with different inter-pad designs, as explained before.

FBK performed IV measurements on the 25 pads of these devices in several configurations. The first interesting configuration is the one with all 25 pads connected to SMU1 and guard ring connected to SMU2, which measures the total matrix and guard ring currents.

The second interesting configuration is the one where individual IV characteristics from the 25 pads are measured using six total SMUs. A single column is connected to five SMUs, from SMU1 to SMU5, one for each pad. The other 20 pads of the matrix are connected to SMU6, while the guard ring is connected to ground unit GNDUnit that fixes the bias to 0 *V* but does not measure the current. The entire process is repeated five times, moving to the next column to get 25 IV curves from single pads.

Figure 3.14 shows a schematic view of a 5×5 matrix, illustrating the connections for the single IV curve measurement of the first column. The enumeration of the pads follows Cartesian coordinates, as each pad of a specific matrix could be identified using a column and a row number. For example, referring to figure 3.14, pad 33 is the central pad, i.e., column 3 and row 3.





For each 5×5 matrix, a plot is produced, putting together all IV curves of the single pads and the IV curve of the total matrix current. For example, the plot for wafer 7, shot (1,3), version 10 is shown in figure 3.15.

The total current is equal to the sum of the 25 pad currents because the equation $ITPA \simeq 25 * IPnm$ holds. The guard ring current contributions are often negligible, like in this case. For example, taking the current points at 100 V one finds that:

- total current is $ITPA = 2.7 \times 10^{-7} A$ (*ITPA* means *I Total Pads Array*, the total matrix current);
- each pad current is $IPnm \simeq 1 \times 10^{-8} A$ (*IPnm* means *I Pad n m*, the current of the pad from n column and m row).



FIGURE 3.15: Plot of IV curves from wafer 7, shot (1,3), version 10 sensor. Each pad IV is plotted, together with total matrix current and guard ring total current. The sensor breakdown is $V_{BD} = 225 V$.

Figure 3.15 shows that one pad with premature breakdown, *IP*13, causes the total sensor breakdown. The sensor breakdown is defined from the total current measurement: when it reaches the current compliance, the measure stops. The voltage at which the measure stops is defined as the sensor breakdown voltage. The pad *IP*13 has a breakdown voltage of 225 *V* and leads the total current to reach the compliance at that value. Although pad *IP*13 leads the total current to reach the compliance, the other pads characteristics continue until higher voltage. This effect depends on how the currents were measured. As explained, the same column pads are connected to five different SMUs, while the other 20 pads are connected to SMU6. SMUs from 1 to 5 have lower compliance than SMU6. Therefore, if a pad from the column reaches compliance, the measure stops for all columns, while if it belongs to one of the 20 pads connected to SMU6, it can draw a higher current before reaching compliance. In summary, all pads from the same column have the same breakdown voltage.

A few pads per wafer (1 or 2) with premature breakdown from the single IV characteristics do not lead the total current to breakdown. This effect is still unexplained; it seems that pads behave differently depending on whether they are measured alone or with other pads. The bad pads count will be done in the following sections and these pads should not be counted as bad pads because they do not cause matrix breakdown.

Evaluation of the Breakdown Voltage Uniformity on 5×5 Matrices

The breakdown voltage values are displayed in a two-dimensional histogram, like the one in figure 3.16. In general, similar observations to the previous sections can be made on breakdown voltage distribution.



FIGURE 3.16: UFSD3.2 shot B wafer 7 breakdown voltage map. Breakdown voltage is encoded using color.

From figure 3.2, it is possible to see that row 1 of the shot B is on the green circle that delimits the safe zone; therefore, one expects these sensors being usually broken. For this reason, devices in row 1 from shot B have not been measured.

The map shows that many sensors on this wafer are broken, in particular sensors from rows 5 and 6, on the periphery of the wafer. Further analysis finds that the 5×5 yield is lower than in previous productions, such as UFSD3 (will be discussed in the following sections), and it is lower than the yield of smaller devices. One should expect that larger devices yield is worse than smaller devices: if a single broken pad leads to a broken sensor, then a larger device will have a worse yield.

The total number of devices and pads measured are counted to quantify yield and bad pad probability. FBK measured 25 shots in wafer 7 and 8 and only 20 shots in all the others. Every shot is made of three versions, and there are 19 total wafers; hence, there are 390 measured shots (17 wafers with 20 shots plus two wafers with 25 shots) corresponding to 1170 sensors. By considering a sensor broken when the breakdown voltage is $V_{BD} < 50 V$, one may find that 461 out of 1170 are broken. Hence, the yield of 5x5 matrices is $\simeq 60.6\%$. The quantification of the breakdown voltage uniformity has not been performed on 5×5 matrices because of the low yield, leading to a too low number of properly working devices for wafer and version to give significant results.

Figure 3.17 shows the breakdown voltage distributions for 5×5 LGAD sensors of wafer 12. On the left, the broken sensors ($V_{BD} < 50$ V) have not been considered. The comparison between the two figures shows that version 9 of wafer 12 has no broken sensors because the two distributions are the same. Instead, version 8 and version 10 have a large number of broken sensors. The same holds for every wafer and anticipates the fact found in the following sections that version 8 and 10 have a lower yield than version 9.



FIGURE 3.17: Version comparison using box plots of UFSD3.2 sensors from wafer 12. Only LGAD sensors (all rows except row 4) are shown. On the left, broken sensors ($V_{BD} < 50 V$) are discarted; on the right, all sensors are considered.

Comparison of Inter-pad Designs with 5×5 Matrices

The inter-pad validation has been carried out by comparing the breakdown voltages of PiN sensors, i.e., devices of row 4, like for shot A.1. The box plots of figure 3.18 show an example of breakdown voltage distribution for the devices of wafer 12.



FIGURE 3.18: Version comparison using box plots of UFSD3.2 sensors from wafer 12. Only PiN sensors (from row 4) are shown.

In this plot, all the bad matrices ($V_{BD} < 50 V$) have not been considered. The number of remaining devices is very low: two sensors for version 8, two for version 9, and one for version 10; therefore, the box plots are very narrow. In general, the number of measured PIN devices per wafer and per version is low (\leq 7).

The plot shows that version 10 has the highest V_{BD} , followed by version 8 and version 9. The same trend can also be observed in the other wafers. As explained in section 2.4, version 10 has a inter-pad design very similar to type 10 of 2 × 2 array. For this reason, they both show the highest breakdown voltage.

Evaluation of the Leakage Current Uniformity on 5×5 Matrices

As already done for shot A.1, every pad current value at a fixed voltage is displayed in two dimensional histograms representing the wafers map. Figure 3.19 shows a comparison between shot A.1 and shot B of the wafer 12, where the same current limits have been used to show the same color legend.



FIGURE 3.19: Comparison between leakage current maps of shot A.1 (on the left) and shot B (on the right) of UFSD3.2 wafer 12

It is interesting to notice a straight dark blue line that cut the shots B from (1,6) to (5,5). Right under the dark line there is a bright yellow, which means that a higher gain doping has been implanted in this wafer region. Rows 5 and 6 must be discarded from the leakage current uniformity analysis on shot B, like it has been done for shot A.1. As for the types of shot A.1, all the versions are considered together. By eliminating rows 5 and 6 and sensors with $V_{BD} < 50 V$, the distributions can be fitted with gaussians profile to extract μ_I and σ_I . Then the ratio $R = \sigma_I / \mu_I$ at 100 V has been evaluated, obtaining the table 3.3 below.

Wafer	R _{LGAD}	R _{PiN}
W4	$(11 \pm 1)\%$	$(29\pm8)\%$
W7	$(15 \pm 2)\%$	$(24\pm 6)\%$
W8	$(10 \pm 1)\%$	$(28\pm8)\%$
W10	$(13\pm2)\%$	$(32\pm10)\%$
W12	$(16\pm2)\%$	$(30\pm9)\%$
W14	$(12\pm1)\%$	$(46\pm21)\%$

TABLE 3.3: Ratio σ_I/μ_I for six wafers of LGAD and PiN sensors of UFSD3.2 shot B.

The ratios obtained are greater than the ones from shot A.1 (see table 3.2), which means that the current uniformity is lower for 5×5 matrices than 2×2 arrays. Even if broken sensors ($V_{BD} < 50 V$) and rows 5 and 6 are neglected, there are some sensors which does not behave correctly but have $V_{BD} > 50 V$. These are damaged sensors spread on rows 2 and 3 and, therefore, difficult to eliminate: they influence the uniformity. The low yield of the 5×5 matrices is responsible for such uniformity ratios, which are, in general, below the expectations.

Evaluation of the Single Pad Yield on 5×5 Matrices

The 5x5 matrices contain a large number of pads and are very useful to evaluate the yield, both of single pads and matrices.

A *bad pad* is a pad with a breakdown earlier than other pads in the same matrix and causes the entire matrix to be broken. Some steps were performed to find the best criterion to classify bad pads, which considers both matrix breakdown voltage and IV curve shape.

For example, in figure 3.15, one may notice a pad that causes the breakdown of the entire matrix; hence this could be counted as a bad pad. However, this breakdown is not very catastrophic. One must consider as bad pads only the ones that make the device unusable, following some given acceptance cuts. The best criterion to identify bad pads was found to be the following:

- consider only broken matrices, i.e., the ones with breakdown $V_{BD} < 50 V$;
- fix a voltage limit, corresponding to 80% of the maximum reached voltage;
- fix a current limit, corresponding to 1µA.
- count the IV characteristics which have value inside this region.

A visualization of the criterion is given in figure 3.20.





This procedure can be followed to obtain the number of bad pads present in figure 3.20, for example. First of all, the total matrix breakdown voltage is V_{BD} = 40 V; therefore, it is considered broken. Secondly, the maximum reached voltage is MRV = 175 V, in black in figure 3.20. Then, the voltage and current limits are defined: voltage limit corresponds to 80% of maximum reached voltage, hence $V_{limit} = 140 V$, while current limit corresponds to $I_{limit} = 1 \mu A$. At this point, the pads which fall inside the fiducial area delimited by the voltage and current limits (the one colored in red in figure 3.20) are counted. In this case, one bad pad is counted, the one with current coordinates IP12.

Once the bad pads are identified, it is possible to put them into a two-dimensional histogram, the so-called *bad pads* map, like the one shown in figure 3.21 for wafer 7, together with the breakdown voltage map of the same wafer. The correlation between bad pads and sensor premature breakdown is well visible.



FIGURE 3.21: UFSD3.2 shot B wafer 7: on the left, bad pads map; on the right, breakdown voltage map.

The bad pads of all UFSD3.2 production have been identified using this method. FBK measured in total 1170 sensors (see previous sections), representing 29250 total pads (1170 total sensors per 25 pads for each sensor). The bad pads are 716 out of 29250. This means that the overall single pad yield is \simeq 97.6%, while the probability of having a bad pad is \simeq 2.4%.

If confronted with previous productions, like, for example, the one of UFSD3 \simeq 99.8% [33], the single pad yield obtained for this production is quite low and not in line with the expectations.

The consequences of such value and some considerations are outlined in the following.

One could consider the simple approximation that the probability of finding a bad pad is constant in a wafer and that at least one bad pad lead to a broken sensor. The probability of having a bad sensor in a matrix with *N* pads is:

$$p(bad sensor) = p(at least 1 bad pad) =$$

= $p(1 bad pad, N - 1 good pads) + p(2 bad pads, N - 2 good pads) + ... = (3.2)$
= $1 - p(0 bad pads, N good pads),$

hence:

$$p(bad sensor) = 1 - p(good pad)^{N}.$$
(3.3)

The final ETL matrix will be a 16 × 32 matrix, hence a matrix with N = 512 total pads. A pad yield of $p(good pad) \simeq 97.6\%$, like the yield found for the UFSD3.2 production, gives the certainty of having only bad structures $p(bad sensor) \simeq 99.9996\%$.

Using equation 3.3, one can find that a hypothetical pad yield of $p(good pad) \simeq$ 99.98% gives the probability of having a broken structure of ~ 10%. Such value for the single pad yield is extremely difficult to reach. The yield measured in UFSD3, $p(good pad) \simeq$ 99.8%, would give a low but still acceptable probability of ~ 60% of having a good half-size 16 × 16 matrix.

Detailed Analysis of the Bad Pads Features

This section reports the characterization of the bad pads found with the criterion described above. Some questions regarding the features of the bad pads arise from the analysis of the single pad yield:

- Are bad pads coming in clusters?
- Are bad pads more concentrated in a certain area of the wafers?
- Are bad pads more concentrated in a certain area of the matrices?

It is necessary to find the number of bad pads per device to answer the first question. The count is simple: find how many bad pads there are in a matrix, then proceed with another matrix and collect all the data in a one-dimensional histogram, representing the distribution of bad pads.

The figure 3.22 was obtained by collecting data from all the shots and all the wafers. The three versions are divided to identify if clustering effects are different according to versions. There are 390 total shots for each version, leading to 1170 shots measured from all wafers.



FIGURE 3.22: UFSD3.2 shot B all wafer distributions. The three versions are divided.

Suppose the probability of finding a bad pad, called here p, is the same on all wafers, and there is no clustering effect. In that case, the probability of finding k bad pads inside a matrix of n pads should follow the binomial distribution:

$$P(k) = \frac{n!}{k!(n-k)!} p^k (1-p)^{n-k}.$$
(3.4)

Using the distributions of figure 3.22, the binomial fit fails. It seems that there are clustering effects, but the data are not enough to make significant affirmations. Further study reveals that it is not true that the probability of finding a bad pad is the same on all wafers. The shots near the wafer edges have a higher probability of bad pads; therefore, they modify the binomial distribution to increase the distributions right tail.

Figure 3.22 also allows finding the yield of good sensors. Recalling that a *bad sensor* is defined as a sensor with at least one bad pad, then the ratio between the first bin and total shots gives the yield of good sensors. From this, one may find table 3.4.

Version	Sensors with 0 Bad Pads	Total Sensors	Yield of Good Sensors
Version 8	212	390	54.4%
Version 9	337	390	86.4%
Version 10	277	390	71.0%
Total	826	1170	70.6%

TABLE 3.4: Yield of good sensors, i.e., sensors with 0 bad pads, of shot B sensors of the UFSD3.2 production.

The overall yield of good sensors is 70.6%. In the previous sections, it was found that the yield of good sensors, defined as sensors with breakdown voltage $V_{BD} > 50 V$, is $\simeq 60.6\%$. The number of matrices with 0 bad pads is higher than the number of matrices with $V_{BD} > 50 V$. Some of the broken sensors do not have identified bad pads, as most of the pads may have a premature breakdown, failing to pass the criterion used.

It is necessary to find if a certain area of the wafers has more bad pads to answer the second question. By summing the bad pads maps, like the one shown on the left side of figure 3.21, one obtains the map of figure 3.23, where the normalized projections according to rows and columns are also shown. Since not all rows and columns have the same number of pads, the projections have to be normalized by the considered row or column pad number.



FIGURE 3.23: UFSD3.2 shot B all wafer summed together bad pads map. Row and column normalized projections are also shown.

The analysis of the normalized projections shows that: row 6 has a higher percentage of bad pads than other rows; column 1 has a higher percentage of bad pads than other columns. The first conclusion for row 6 confirms the general trend from shot A.1 and shot A.2. The only shot present in row 6 is close to the wafer border. The second conclusion that column 1 has a higher number of bad pads could induce to think that something went wrong during the dicing line of the half wafer. However, measurements from FBK were taken before the wafer dicing; therefore, this can not be the reason for this trend. The origin of this localized worse yield is under scrutiny in FBK.

To answer the third question, it is necessary to determine whether a certain area of the matrix has more bad pads than the rest. One has to consider the different designs independently, summing all the wafers to increase the statistics. If a certain sensor has a bad pad corresponding to position IPnm, this will increase the map by an entry in position column n and row m.



Figure 3.24 shows the four different maps: the three versions of LGAD sensors are separated from all versions of PiN sensors. All wafers are summed together.

FIGURE 3.24: UFSD3.2 shot B all wafer summed together bad pads position maps. The four maps correspond respectively to LGAD sensors from version 8, LGAD sensors from version 9, LGAD sensors from version 10, PiN sensors from all the versions.

The entries of each plot represent the number of total bad pads for each version of LGAD sensors or for PiN sensors (all versions summed). The table 3.5 summarizes the results. LGAD sensors have a higher probability of having bad pads than PiN sensors. This suggests that the presence of the gain layer can be responsible for the lower yield.

Version 9 has the lowest bad pads probability. Sensors with the same inter-pad design as version 9 have been produced since UFSD2 by FBK, representing a well-tested design. On the opposite side, version 10 has a more complex inter-pad design due to the additional grid of guard ring between pads, which can lower the yield.

Version	Sensor	Bad Pads	Total Pads	Probability of Bad Pads
Version 8	LGAD	394	8550	4.6%
Version 9	LGAD	104	8550	1.2%
Version 10	LGAD	204	8550	2.4%
All Versions	PiN	14	3600	0.4%

TABLE 3.5: Bad pad probabilities for shot B sensors of the UFSD3.2production.

The origin of the yield of version 8 is under scrutiny in FBK.

Another interesting conclusion is that bad pads seem more concentrated in certain areas of the matrices. In particular, for version 8, the central pad is the most problematic, and the eight neighboring pads are more problematic than the outer pads. A similar trend also appears for version 10, even with a less precise pattern. Instead, the low statistic does not allow clear conclusions about version 9 and PiN sensors. In particular, version 9 has a random distribution of bad pads.
3.2.4 Analysis of the CV Characteristics

The CV characteristics measured by FBK can be used to extract important parameters, as the gain layer and full depletion voltage (V_{FD}) of the device. This information can be used to evaluate gain layer uniformity on the wafer.

The analysis performed is, in particular, based on the full depletion voltage distribution. The extraction is performed using the numerical derivative of C^{-2} (see next sections for details), which is a commonly used method and seems very appropriate in this case.

A two-dimensional map can be used to display the gain layer uniformity on a single wafer: here, the full depletion voltage value is encoded using color.

As already explained in the type inversion studies section, only wafer 5, 7, 9, and 15 have meaningful CV curves because they have no substrate-type inversion. So CV analysis is performed only on these wafers.

Full Depletion Uniformity

The software conversion section produces a tree containing all CV curves of both shot A.1 and A.2 of the wafers 5, 7, 9, and 15. The CV curves have been used exclusively to study the gain layer uniformity through the full depletion voltage V_{FD} .

An example of plot for a 2×2 array is shown in figure 3.25, where the CV curves of the four pads are presented together with their C⁻²V curves. Each pad has a different color.



FIGURE 3.25: UFSD3.2 shot A.1 Wafer 7, shot (3,3), version 10 CV curves. Every pad is shown, together with the $C^{-2}V$ curves.

As explained in section 2.5, $C^{-2} \alpha \rho V$, where ρ is the resistivity of the doped silicon $\rho \alpha N_A^{-1}$, and N_A is the density of doping atoms (see equation 2.8). The resulting $C^{-2}V$ curve is composed of two straight lines with different angular coefficients, followed by a horizontal line. The two slope changes occur at the gain layer depletion voltage and full depletion voltage, respectively. It is easier to evaluate the full depletion voltage V_{FD} from $C^{-2}V$ curves.

The method followed for the extraction of V_{FD} is here summarized:

- starting from C values from the CV curves measured by FBK, C⁻² was calculated for each voltage;
- the numerical derivative curve was found by replacing $C^{-2}[i]$ with $\frac{C^{-2}[i]-C^{-2}[i-1]}{V[i]-V[i-1]}$. The symbol V[i] means the voltage with index *i*, same holds for $C^{-2}[i]$;
- the maximum of the numerical derivative was found.

The CV curve has been measured with voltage steps of 200 mV. The index *i* is the index corresponding to the *i*-th measurements of capacitance or, equivalently, to the *i*-th voltage step.

The three steps of the process are shown in figure 3.26, taking pad 1 (P1) from wafer 7, shot (3,3), type 10, the same sensor as figure 3.25.



FIGURE 3.26: Simple view of the method used to extract the full depletion voltage from a pad CV curve. On pad 1 from wafer 7, shot (3,3), type 10 was found $V_{FD} = 24 V$.

One may notice that the numerical derivative in figure 3.26 presents several spikes at higher voltages. The sensor is fully depleted at such voltages, and the capacitance is very low. There are little spikes in the capacitance value induced by noise fluctuations, which propagate to the C^{-2} and significantly affect numerical derivatives. Occasionally, tiny noise spikes can lead to huge spikes in numerical derivatives, even higher than the maximum depletion voltage. In this case, the maximum research fails. For such reason, the interval in which the maximum is searched is restricted. Moreover, the numerical derivative curve could be smoothed, for example by replacing x[i] with (x[i] + x[i+1])/2, where x[i] is the numerical derivative value: this limits the fluctuation effects.

The method has a systematic bias due to how numerical derivative is evaluated. In fact $C^{-2}[i]$ is replaced with $\Delta C_{i,i-1}^{-2} / \Delta V_{i,i-1}$ and this is connected to the value V[i]. In order to get a correct result, one should place $\Delta C_{i,i-1}^{-2} / \Delta V_{i,i-1}$ in the center of the interval V[i] - V[i-1]. In summary, as the voltage steps are of 200 *mV*, one should consider a systematic error on V_{FD} of 100 *mV*. The full depletion voltage of every pad of every measured sensor has been placed in two-dimensional maps, one per wafer. An example of a map is shown in figure 3.27 for wafer 7. Row 4 was not considered in the analysis.



FIGURE 3.27: UFSD3.2 shot A.1 full depletion voltage map for wafer 7. V_{BD} is encoded with colors.

The same analysis has been repeated also on CV curves from shot A.2. According to the method explained before, one can find the depletion voltage value for every LGAD pad and put the values on a two-dimensional map. The map for wafer 7 is shown in figure 3.28.



FIGURE 3.28: UFSD3.2 shot A.2 full depletion voltage map for wafer 7. V_{BD} is encoded with colors.

Both figures show that some pads have no corresponding value in the map and are colored in white. This means that the software fails in the full depletion voltage evaluation because, for example, it finds a maximum that does not correspond to full depletion but is related to noise spikes. Pads with no V_{BD} values are more concentrated in rows 1, 5, and 6: the rows near the border.

It is important to note that the average full depletion voltage from wafer 7, shot A.1 devices, is consistent with the average full depletion voltage measured on shot A.2 devices: respectively $V_{FD,A1} = (23.7 \pm 0.4) V$ and $V_{FD,A2} = (24.2 \pm 0.6) V$. The errors were evaluated as the standard deviation of full depletion voltage distributions. Following the method used in the previous sections, the full depletion uniformity can be quantified by the ratio σ_{FD}/μ_{FD} , obtaining the table 3.6. Only rows 2, 3, and 5 have been considered because they are not affected by software issues; moreover, only wafer 7 has CV data for shot A.2.

Wafer	R _{A1}	R _{A2}
W5	$(0.94 \pm 0.01)\%$	/
W7	$(1.68 \pm 0.03)\%$	$(2.48 \pm 0.06)\%$
W9	$(0.579 \pm 0.003)\%$	/
W15	$(0.188 \pm 0.004)\%$	/

TABLE 3.6: Ratio σ_{FD}/μ_{FD} for non-type inverted wafers of UFSD3.2 shot A.1 and shot A.2. Shot A.2 has CV data only for wafer 7.

In summary, the non-type inverted wafers have a very good full depletion uniformity and, therefore, a good gain layer doping uniformity.

3.3 Floating Pads Characterization

The final sensor for the ETL will be a 16×32 pads matrix (see figure 1.11). Each pad is a single read-out channel; therefore, it must be connected with a single channel of the read-out chip, called ETROC. The connection will be made with bump bonding between single channels of the sensors and the ETROCs (see figure 1.10) [12]. The bump bonding process has a high technology yield, but not 100% [45]. One may expect that a few pads (1-2) of the total 512 pads are not correctly bonded with the ETROC.

A pad of the sensor which is not correctly bonded with the ETROC is called a *floating pad*. The entire matrix should be resilient to floating pads presence, i.e., its electric characteristics should not vary to ensure correct functioning even if some pads are floating.

The resilience to floating pads presence depends upon the inter-pad design. With the inter-pad resistance characterization (see next sections), the floating pads characterization could provide a useful tool for evaluating the most robust inter-pad design.

This chapter shows how a floating pads characterization could be done, together with the results on UFSD3.2 and HPK2 sensors.

3.3.1 Measurements

Evaluating the resilience to floating pads presence means evaluating the standard electric characteristics with one or more pads floating. CV curves are useful for evaluating the depletion voltage and obtaining useful information on the gain layer doping and shape. Both of these characteristics are unaffected by floating pads presence; therefore, one should focus on IV curves.

Pads correctly bonded to the ETROC have a voltage of 0 *V*, while the backplane has a voltage of *Vbias*, which inversely polarizes the sensor. A floating pad would position at a voltage between 0 *V* and *Vbias*: the voltage difference between two neighboring pads can lead to a premature breakdown or noisy IV characteristics. In summary, in order to study resilience to floating pads presence, one should focus on breakdown voltage and curve shape of IV curves.

The method used to perform this study consists of recreating a floating pads configuration. The standard IV characteristic (figure 2.14) is measured, but with one or more pads floating. The pads connected to the SMUs are forced to ground because each SMU provides a voltage $V_{GND} = 0$ V and measures the current, while the pads that are not connected to SMU are floating. The main focus is on breakdown voltage and the shape of IV curves. One should compare these characteristics with and without floating pads presence.

The measurements on 2×2 pads sensors have been performed with one, two, or three floating pads. The configuration with two and three floating pads means that, respectively, 50% and 75% of the total pads are floating. These configurations will not correspond to any real application condition. However, a floating pads study pushed over the limits could also be performed for academic interest.

The four pads of a 2×2 array were numerated according to figure 3.29, where the left-down pad is pad P1. The sensor shown has the typical UFSD3.2 layout, but the same concept has been applied to HPK2 sensors.



FIGURE 3.29: Layout of a 2×2 pads sensor, where pad number is specified.

In the following, the legend used to indicate which pad is floating is:

- 0 pads floating means all connected to SMU;
- 1 pad floating means pad P2 floating;
- 2 pad floating means pads P2 and P3 floating;
- 3 pad floating (when necessary) means pads P2, P3, and P4 floating.

During measurements of HPK2 irradiated sensors, two sensors went to irreversible breakdown using the configuration with 3 pads floating. Therefore, the configuration with 3 pads floating has not been used anymore for HPK2 sensors.

3.3.2 Experimental Setup

The experimental setup used for floating pads measurements consists in:

- a probe station with five probes, one for the guard ring and the others four for the 2×2 pads;
- a device analyzer with three independent SMUs and an HV unit.

The guard ring is connected through a probe to the low voltage of the HV unit, which provides a voltage of 0 *V*; the high voltage of the HV unit is connected directly to the backplane, which provides a voltage *Vbias*. The number of independent SMUs is sufficient since pads P3 and P4 are short connected. This SMU measures together with the IV characteristics of pads P3 and P4, but this does not affect the results.

In standard IV, all the probes are connected to the sensors, one to the guard ring and the other four to the 2×2 pads. The floating pad configuration means that a certain number of probes are not connected to the respective pad. When the probe is lifted, the pad will be floating.

Figure 3.30 shows the experimental setup, where both the probe station with the five probes (on the left) and the device analyzer *Keysight B1500A* (on the right) are visible.



(a) Probe station

(b) Device Analyser

FIGURE 3.30: Experimental setup used for the floating pads studies. On the left the probe station; on the right the device analyzer.

3.3.3 Results

Floating pad studies were performed on 2×2 array devices with different features. Both PiN and LGAD sensors, both new and irradiated sensors, both production UFSD3.2 from FBK and production HPK2 from HPK were considered to explore the complete set of parameters that could influence the resilience to floating pads.

The inter-pad design has been studied both for UFSD3.2 sensors and HPK2 sensors by comparing the different types. Like UFSD3.2 production, HPK2 2×2 pads sensors have different inter-pad designs. The types are four according to gain layer-gain layer distance. The names of these four types follow the abbreviation *SEn IPm*, where the *IPm* stands for *inter-pad*. The number *m* could be 3, 4, 5, or 7 and represents different inter-pad distances in ascending order.

The table 3.7 below shows the sensors that were measured.

PiN sensors of UFSD3.2 production have been measured before irradiation. The type comparison is the main purpose of this study for UFSD3.2 sensors; therefore, unirradiated PiNs are the most suitable sensors. PiN sensors were chosen to exclude the gain layer effects on premature breakdown or noisy characteristics. All PiN sensors are from the same wafer to reduce other uncertainties causes.

There are two HPK2 sensors from wafer 28 and 43 irradiated at $1.5 \times 10^{15} n_{eq}/cm^2$. These two sensors were the first tested, and both broke in a configuration with 3 floating pads. The rest of HPK2 sensors have been measured at most with two floating pads to avoid further irreversible breakdowns. The rest of the HPK2 sensors have been taken from the same wafer (wafer 37) to reduce other uncertainties causes. There is one sensor of each type (four in total) at each fluence (three in total), hence twelve total HPK2 sensors from wafer 37.

Production	Sensor	Wafer	Туре	Fluence $[n_{eq}/cm^2]$	Tested Sensors
UFSD3.2	PiN	Wafer 7	Type 4	0	3
UFSD3.2	PiN	Wafer 7	Type 8	0	3
UFSD3.2	PiN	Wafer 7	Type 9	0	3
UFSD3.2	PiN	Wafer 7	Type 10	0	3
HPK2	LGAD	Wafer 28	SE3IP5	$1.5 imes10^{15}$	1
HPK2	LGAD	Wafer 43	SE3IP5	$1.5 imes10^{15}$	1
HPK2	LGAD	Wafer 37	SE3IP3	$8 imes 10^{14}$	1
HPK2	LGAD	Wafer 37	SE3IP4	$8 imes 10^{14}$	1
HPK2	LGAD	Wafer 37	SE5IP5	$8 imes 10^{14}$	1
HPK2	LGAD	Wafer 37	SE3IP7	$8 imes 10^{14}$	1
HPK2	LGAD	Wafer 37	SE3IP3	$1.5 imes10^{15}$	1
HPK2	LGAD	Wafer 37	SE3IP4	$1.5 imes10^{15}$	1
HPK2	LGAD	Wafer 37	SE5IP5	$1.5 imes10^{15}$	1
HPK2	LGAD	Wafer 37	SE3IP7	$1.5 imes10^{15}$	1
HPK2	LGAD	Wafer 37	SE3IP3	$2.5 imes10^{15}$	1
HPK2	LGAD	Wafer 37	SE3IP4	$2.5 imes10^{15}$	1
HPK2	LGAD	Wafer 37	SE5IP5	$2.5 imes10^{15}$	1
HPK2	LGAD	Wafer 37	SE3IP7	$2.5 imes10^{15}$	1

TABLE 3.7: Sensors under investigation within floating pads characterization.

UFSD3.2

The floating pads studies were carried out on UFSD3.2 production to evaluate the differences in resilience to floating pads presence between types. The main types under investigation are the four types with the highest breakdown voltage, as evaluated from the software analysis (see, for example, figure 3.10). Type 4, 8, 9, and 10 were selected. A total of twelve 2×2 sensors were measured to accumulate statistics: three different shots for each type.

Every shot has been measured with 0, 1, 2, and 3 floating pads. The comparison between the four IV curves on the same plot gives figures very similar to figure 3.31 for each sensor. Figure 3.31 shows the sensor from wafer 7, type 8, and shot (8,4) as an example.

The four characteristics are shown in different colors, where each color represents an IV curve measured with different floating pads number. The characteristics were measured using the bias voltage step of 5 *V*. The breakdown voltage is visible and defined as the voltage where the current increases. For example, the blue curve has a breakdown voltage of $\simeq 530$ *V*.

First of all, it is interesting to notice that the four characteristics are very similar except for the breakdown voltage. One may notice that the breakdown voltage decreases with the number of floating pads for every measured sensor. Instead, the entity of the current spikes, i.e., the noise of the IV curve, is of the same magnitude as the apparatus noise, which is $\sim 10 nA$, and does not increase above the experimental resolution. Therefore, only variations of the breakdown voltage have been studied.



FIGURE 3.31: UFSD3.2 wafer 7 typical example of PiN sensor IV curve with floating pads. Different color belongs to different floating pads number.

By calculating the means and the standard deviations of the breakdown voltage for all the sensors of the same types, one obtains the plot in figure 3.32. The figure 3.32 is useful to evaluate which type is the most resilient to floating pads.



FIGURE 3.32: UFSD3.2 wafer 7 breakdown voltage against floating pads number. Different color belongs to different types.

Another type of plot is produced, showing the difference of breakdown voltages with different floating pads configuration divided by the breakdown voltage with 0 floating pads $\Delta V_{BD}/V_{BD,0FP}$ as a series of columns. Every column of this plot represents a difference between the breakdown voltage with 0 floating pads and the breakdown voltage with 1, 2, or 3 floating pads, respectively. The lower the column and the more the resilience to floating pads. Figure 3.33 shows this plot.



FIGURE 3.33: UFSD3.2 wafer 7 breakdown voltage difference between configuration with 0 floating pads and the others divided by breakdown voltage of configuration with 0 floating pads. Different color belongs to different type.

The direct comparison between the columns of the plot in figure 3.33 helps to evaluate which type is the most resilient to floating pads quantitatively. One may notice that types 4 and 10 seem more resilient to the configuration with 1 floating pad than types 8 and 9. Type 10 is the most resilient to configuration with 2 or 3 floating pads, while type 8 is the least resilient in every case.

In summary, these results confirm that type 10 is, in general, the most resilient to floating pads. As already mentioned, type 10 has the safest design (largest inter-pad width with an additional grid of guard ring between pads).

HPK2

The floating pads studies were carried out on HPK2 production to evaluate the resilience to floating pads presence of new and irradiated sensors and, like UFSD3.2 production, to evaluate the resilience to floating pads presence of the different types.

First of all, two sensors from wafer 28 and wafer 43 were taken. Both sensors have been irradiated with neutron at a fluence of $1.5 \times 10^{15} n_{eq}/cm^2$, and have the same inter-pad design, named *SE3 IP5*. A comparison of the IV curves is shown in figure 3.34. As explained before, HPK2 sensors are identified by the name *IPn*, where *n* stands for the wafer position.

It is interesting to compare these characteristics and the ones shown in figure 3.31. The current is higher: here $\sim 10 \, uA$, while before $\sim 10 \, nA$. The comparison is between UFSD3.2 unirradiated PiNs and HPK2 irradiated LGADs. LGADs have a higher current than PiNs. Moreover, as mentioned in section 2.3, irradiation causes an increase of the leakage current. The breakdown voltage remains quite the same also when increasing the number of floating pads, while in figure 3.31 the breakdown voltage changes a lot. On the other hand, increasing the number of floating pads leads to noisier curves, while before, this effect was not visible.



FIGURE 3.34: HPK2 wafer 28 and wafer 43 IV curves comparison with different floating pads number. Both sensors broke using three floating pads configuration.

Both sensors broke during the three floating pads measurements at the same voltage, $\simeq 650 V$, in the same configuration with three floating pads. The meaning of *breaking* is that these sensors underwent an irreversible breakdown. After the sensors reached the breakdown, some burn marks appeared on the corner. Performing an IV curve on the sensors again, one obtains that a very high current is flowing even at very low voltage. Probably, the sum of damage from irradiation, three floating pads, and high voltage led to an irreversible junction breakdown.

At a visible level, a broken sensor has some burn marks on the contact of the guard ring. Typically, these marks correspond to the probe contact points, probably because there is a higher current density. The marks are recognizable because of the color contours tending to green. In figure 3.35 a broken HPK2 sensor is shown, together with the zoom in on the burn mark.



(a) Broken Sensor

(b) Zoom of the Burn Mark

FIGURE 3.35: On the left an HPK2 broken sensor, on the right the same sensor but zoom in on the burn mark.

The configuration with three floating pads on HPK2 irradiated sensors was abandoned to avoid further breakings during the following measurements.

A set of 12 total sensors were chosen from HPK2 wafer 37, like is shown in

table 3.7. All four types have been measured: SE3IP3, SE3IP4, SE5IP5, and SE3IP7. Similarly, all three fluences have been measured: $8 \times 10^{14} n_{eq}/cm^2$, $1.5 \times 10^{15} n_{eq}/cm^2$ and $2.5 \times 10^{15} n_{eq}/cm^2$.

Plotting the three IV curves on the same graph (with 0, 1, and 2 floating pads), one may notice a situation very similar to the one in figure 3.34. The presence of floating pads does not influence the breakdown voltage. The HPK2 irradiated sensors are very resilient to floating pads presence.

One should remember that with UFSD3.2 unirradiated PiN, the noise was not visible because it had the same magnitude as the apparatus noise. In this case, on the opposite, the noise could lead to spikes of magnitude $\sim 10 \ uA$, which are visible in the final IV curves. Instead, the breakdown voltages do not vary at all. In summary, the only visible effect is the increase in noise. Therefore, the study of floating pads with HPK2 irradiated sensors means studying the noise of the IV curves.



The IV curves with floating pads are shown in a single plot like in figure 3.36.

FIGURE 3.36: HPK2 wafer 37, an example of IV curves with 0, 1, and 2 floating pads from SE3 IP4, P84. The difference between the curve without floating pads and, respectively, with 1 or 2 floating pads is also shown.

The curve obtained by calculating the point-to-point difference between curves with 0 and 1 or 2 floating pads is called *difference curves*, and it is also shown in figure 3.36. If floating pads presence does not influence a sensor, one should expect that its difference curve fluctuates around the zero value, with spikes of the same magnitude of apparatus noise $\sim 10 nA$. Instead, difference curves of HPK2 sensors have fluctuations of $\sim 10 uA$.

The Root-Mean-Square (RMS) evaluation from the difference curves provides a quantitative comparison. From figure 3.36, it is visible that the RMS noise of the difference between 0 and 2 floating pads is higher than the difference between 0 and 1 floating pad, which simply means that the sensor is less resilient with two floating pads than one floating pad. The calculation has been carried out for every sensor, obtaining the plots shown in figure 3.37 and figure 3.38. According to the two difference curves obtained, two figures show the RMS: the difference between 0 and 1 floating pads (top figure) and the difference between 0 and 2 floating pads (bottom figure). All fluences and all types are presented.



FIGURE 3.37: HPK2 wafer 37, RMS of the curves obtained from the difference between 0 floating pads and 1 floating pad. Every fluence and every type is presented.





By comparing columns of the same plot at different fluences, one may notice that the RMS noise is quite the same with different fluences.

By comparing columns of the same plot and the same fluence, one may carry out the type comparison. The RMS noise of the type SE3 IP3 (in red in figure 3.37 and figure 3.38) is always the lowest. SE3 IP3 is the type with the most aggressive design, i.e., the smallest inter-pad distance; therefore, one should expect that it is the least resilient to floating pads presence. Instead, SE3 IP3 is the type with higher resilience to floating pads presence.

A type comparison between the other types is quite difficult. In general, type SE5 IP5 seems the least resilient to floating pads presence because it has the highest RMS noise, but this does not hold for all the comparisons. In fact, by looking at RMS noise with two floating pads (figure 3.38) and with fluence $8 \times 10^{14} n_{eq}/cm^2$, the type SE3 IP4 has the highest RMS noise.

3.4 Inter-pad Resistance Characterization

The inter-pad designs have also been studied with respect to the inter-pad resistance, which is the ohmic resistance between two neighboring pads.

A pixelated sensor, such as the final sensor for ETL (a 16×32 pads matrix, see figure 1.11), needs that each pad is independent from the others. In other words, the charge created from a particle must be collected only by the pad crossed by the particle. In the ideal case, no charge sharing is present.

The UFSD inter-pad region has a JTE implant which ensures the pad isolation (see figure 2.8). Moreover, it ensures that electron-hole pairs generated by particles hitting in between pads are not reaching the multiplication layer. A safe inter-pad width and a good JTE design ensure high pad isolation and, therefore, a high interpad resistance.

This chapter shows the inter-pad resistance characterization performed on the sensors of the UFSD3.1 and HPK2 productions.

3.4.1 Measurements

The inter-pad resistance can be evaluated from a measurement of the inter-pad current on 2×2 pads sensor. The inter-pad current can be present only when there is a voltage difference between pads; therefore, one needs to create a voltage difference between pads.

The standard IV characteristic does not provide a voltage difference between pads. In fact, in the standard IV characteristic (see figure 2.14), each pad is connected to its own SMU and the backplane to a High Voltage unit (HV unit). Each SMU fixes the voltage to 0 V and measures the current, while the HV unit provides a voltage sweep between fixed values V_{start} and V_{stop} . Both $V_{start} < 0 V$ and $V_{stop} < 0 V$ to ensure the inverse polarization of the sensor.

Performing a standard IV characteristic, focusing on pad P1 with voltage $V_1 = 0 V$ and focusing on the extremes of a small voltage region, for example, $\pm \delta V$ around a value *V*bias < 0 *V*, one obtains:

- when $HV = Vbias \delta V$, each pad has a voltage difference respect to the backplane of $\Delta V_1 = V_1 - HV = -Vbias + \delta V$;
- when $HV = Vbias + \delta V$, each pad has a voltage difference respect to the backplane of $\Delta V_1 = V_1 - HV = -Vbias - \delta V$.

All the pads are at the same voltage; therefore, no inter-pad current is expected. Another type of measurement is needed to evaluate the inter-pad current.

The so-called *inter-pad IV characteristic* is introduced. The SMUs are placed in the same way as the standard IV characteristic, but the voltages provided are different. The HV module provides a fixed voltage *Vbias* to the backplane, while the SMU1 provides a small voltage sweep around 0 *V* of $\pm \delta V$. The other three pads are connected to their own SMU, which fixes the voltage to 0 *V*.

As before, if we perform an inter-pad IV characteristic and focus on the pad P1 with voltage V_1 , we obtain:

- when HV = Vbias and $V_1 = \delta V$, pad P1 has a difference respect to the backplane of $\Delta V_1 = V_1 - HV = -Vbias + \delta V$;
- when HV = Vbias and $V_1 = -\delta V$, pad P1 has a difference respect to the backplane of $\Delta V_1 = V_1 HV = -Vbias \delta V$.

The voltage difference between the backplane and the pad P1 is the same as the standard IV characteristic, but the voltage differences between pads are different. This time, since the voltage sweep is performed only on the pad P1, we obtain:

- when HV = V bias and $V_1 = -\delta V$, pad P1 has difference respect to the pad Pn of $\Delta V_{1n} = V_1 V_n = -\delta V$, therefore the inter-pad current flows inside P1;
- when HV = V bias and $V_1 = \delta V$, pad P1 has difference respect to the pad Pn of $\Delta V_{1n} = V_1 V_n = \delta V$, therefore the inter-pad current flows outside P1.

In summary, one expects an inter-pad current because there are voltage differences between pads.

The idea behind the inter-pad IV characteristic is shown in figure 3.39, where some numerical values have been inserted: V bias = -200 V, $\delta V = 10 V$. Both the extremes of the pad P1 voltage sweep are shown, together with the expected inter-pad current according to voltage difference between pads.



FIGURE 3.39: Schematic view of the inter-pad IV characteristic measurement. On the left the lower bound of the P1 voltage sweep, on the right the upper bound. The expected inter-pad current is shown as red arrows going inside (on the left) or outside (on the right) the pad P1. The inter-pad IV characteristic performed on pad P1 measures the total current flowing into the pad P1, which is the sum of the pad-backplane current and the interpad current. The two effects must be disentangled to recognize only the inter-pad contribution. According to figure 3.39, one expects that:

- when $V_1 = -\delta V$ ($\Delta V_1 = -V bias \delta V$ and $\Delta V_{1n} = -\delta V$), the inter-pad current flows inside the pad P1, therefore the total P1 current is lower than the standard P1-backplane current;
- when $V_1 = 0V$ ($\Delta V_1 = -Vbias$ and $\Delta V_{1n} = 0V$), the inter-pad current is zero, therefore the total P1 current is equal the standard P1-backplane current;
- when $V_1 = \delta V$ ($\Delta V_1 = -Vbias + \delta V$ and $\Delta V_{1n} = \delta V$), the inter-pad current flows outside the pad P1, therefore the total P1 current is higher than the standard P1-backplane current.

A comparison between the standard IV characteristic and the inter-pad IV characteristic is shown in figure 3.40. Data are taken with a sensor of the HPK2 production (see next sections).



FIGURE 3.40: Comparison between the standard IV characteristic and the inter-pad IV characteristic. Data are taken from an HPK2 sensor (see next sections).

In the beginning, the total pad P1 current is lower than the standard P1-backplane current, while at the end, the total P1 current is higher than the standard P1-backplane current. Both currents have a linear trend as a function of the voltage: this is since the considered δV is small compared to the total sensor characteristics, from 0 *V* to breakdown voltage; therefore, a linear approximation holds.

A method to evaluate the inter-pad resistance consists of performing the standard IV characteristic and the inter-pad IV characteristic on a sensor in the same ΔV_1 interval like it has been done in figure 3.40. Then compute the difference between the inter-pad and the standard IV characteristics: the resulting IV characteristic is the contribution of the inter-pad current. From this characteristic, it is possible to extract the inter-pad resistance from Ohm's law as the inverse of the angular coefficient:

$$R_{int,1} = \frac{\Delta(\Delta V_1)}{\Delta(I_{int,1} - I_{std,1})}.$$
(3.5)

The inter-pad resistance of the pad P1 is the sum of the inter-pad resistances between pad P1 and the neighbor pads. The guard ring must also be considered because the inter-pad design is the same between guard ring and pad or between pad and pad. In summary, the inter-pad resistance between pad P1 and a given pad Pn can be extracted by considering that the overall inter-pad resistance $R_{int,1}$ is the parallel between the four single inter-pad resistance $R_{int,1,n}$. Here, *n* is anyone of the neighboring pads or the guard ring; hence:

$$\frac{1}{R_{int,1}} = \frac{1}{R_{int,1,2}} + \frac{1}{R_{int,1,3}} + \frac{1}{R_{int,1,4}} + \frac{1}{R_{int,1,guard\ ring}}.$$
(3.6)

If the single inter-pad resistances are quite similar, the relation become:

$$R_{int,1,n} \simeq 4 * R_{int,1}. \tag{3.7}$$

It must be added that, as mentioned in 2.4, type 10 has an inter-pad design where a grid of guard ring is added between each pad. A guard ring covers all four sizes of a single pad, and, therefore, the inter-pad resistance for type 10 should be understood as a pad-guard ring resistance.

The main focus of the study is to evaluate the inter-pad resistance after irradiation. A large number of measurements have been performed on sensor irradiated at different fluences.

It is also interesting to study the dependency of this method upon the different operating conditions of the device. The main operating conditions under investigation are:

- the voltage *V*bias, by evaluating the inter-pad resistance at two different *V*bias: Vbias = -100 V and Vbias = -200 V;
- the temperature *T*, by evaluating the inter-pad resistance at two different *T*: $T = 24 \degree C$ (room temperature) and $T = -20 \degree C$.

A more detailed measurements of the inter-pad resistance as a function of the temperature has been performed.

3.4.2 Experimental Setup

The experimental setup used for inter-pad resistance measurements consisted in:

- a probe station with five probes, one for the guard ring and the other four for the 2×2 pads. This probe station has a temperature controller which allows to control and change the chuck temperature up to $T = -40 \,^{\circ}C$;
- a device analyzer with two independent SMUs and an HV unit.

The number of independent SMUs is sufficient because three pads are always short connected: this does not affect the results because a single pad (generally pad P1) is interesting. The guard ring is connected to the low voltage of the HV unit, which provides 0 *V*, while the backplane is connected to the high voltage of the HV unit, which provides *V bias*.

A view of the experimental setup is shown in figure 3.41, where both the probe station and the device analyzer *Keysight B1500A* are shown.



(a) Probe Station

(b) Device Analyzer

FIGURE 3.41: Experimental setup used for the inter-pad resistance measurements. On the left, the probe station; on the right, the device analyzer.

3.4.3 Results

Inter-pad resistance characterization has been performed on LGAD sensors of 2×2 array devices. The comparison between different types, which correspond to different inter-pad designs, is crucial. Finally, also a comparison between different wafers has been made. Both HPK and FBK productions have been considered, in particular, HPK2 production from HPK and UFSD3.1 production from FBK.

Type comparison in UFSD3.1 has been carried out using three types: type 8, type 9, and type 10. The layout of these types is the same on UFSD3.1 and UFSD3.2; therefore, the results are valid for UFSD3.1 and UFSD3.2 productions. As mentioned in 2.4, wafers of the UFSD3.1 production have different p-stop dopings. The p-stop doping could affect the inter-pad resistance; therefore, three wafers have been measured: wafer 13, wafer 14, and wafer 18. The p-stop dose in wafer 14 of UFSD3.1 is the same as all wafers of UFSD3.2, while wafer 13 has p-stop doping of half of wafer 14 and wafer 18 has ten times higher.

Type comparison in HPK2 has been carried out using all the four different types: SE3 IP3, SE3 IP4, SE5 IP5, and SE3 IP7. Each HPK2 type has a different inter-pad width according to their name *IPn*.

Each type has been measured at different fluences. Each measurement has been performed at different temperatures and different *Vbias*. Everything is summarized in the table 3.8: 43 different sensors have been tested, of which 4 from wafer UFSD3.1 wafer 13, 15 from UFSD3.1 wafer 14, 12 from UFSD3.1 wafer 18, and 16 from HPK2 wafer 37. A series of repeated measurements were performed on the same sensor but using different pads. The tested HPK2 sensors are the same used for the floating pad characterization.

Production	Wafer	Туре	Fluence $[n_{eq}/cm^2]$
UFSD3.1	Wafer 13	Type 9	$4 imes 10^{14}$, $1.5 imes 10^{15}$
UFSD3.1	Wafer 13	Type 10	$4 imes 10^{14}$, $1.5 imes 10^{15}$
UFSD3.1	Wafer 14	Type 8	$0,4 imes 10^{14},8 imes 10^{14},1.5 imes 10^{15},3 imes 10^{15}$
UFSD3.1	Wafer 14	Type 9	$0,4 imes 10^{14},8 imes 10^{14},1.5 imes 10^{15},3 imes 10^{15}$
UFSD3.1	Wafer 14	Type 10	$0, 4 imes 10^{14}, 8 imes 10^{14}, 1.5 imes 10^{15}, 3 imes 10^{15}$
UFSD3.1	Wafer 18	Type 8	$0,4 imes 10^{14},8 imes 10^{14},1.5 imes 10^{15}$
UFSD3.1	Wafer 18	Type 9	$0,4 imes 10^{14},8 imes 10^{14},1.5 imes 10^{15}$
UFSD3.1	Wafer 18	Type 10	$0,4 imes 10^{14},8 imes 10^{14},1.5 imes 10^{15}$
HPK2	Wafer 37	SE3 IP3	$0,8 imes 10^{14}, 1.5 imes 10^{15}, 2.5 imes 10^{15}$
HPK2	Wafer 37	SE3 IP4	$0,8 imes 10^{14}, 1.5 imes 10^{15}, 2.5 imes 10^{15}$
HPK2	Wafer 37	SE5 IP5	$0,8 imes 10^{14}, 1.5 imes 10^{15}, 2.5 imes 10^{15}$
HPK2	Wafer 37	SE3 IP7	$0,8 imes 10^{14}, 1.5 imes 10^{15}, 2.5 imes 10^{15}$

 TABLE 3.8: Sensors under investigation within inter-pad resistance characterization.

UFSD3.1

Wafer 14 has the highest number of measured sensors; therefore, it is particularly indicated for carrying on the studies on the dependencies upon the operating conditions of the device: these sensors have been used to evaluate the effect of the backplane voltage *V bias* and the temperature *T*.

First of all, it is possible to compare the inter-pad resistance measured with different *Vbias*. The results are shown in the figure 3.42, where the temperature is set to T = -20 °C. The y-axis has a logarithmic scale because the inter-pad resistances vary by a few orders of magnitude. The same results could be obtained for a temperature of T = 24 °C.



FIGURE 3.42: Inter-pad resistance from UFSD3.1 wafer 14. Two different *V*bias are shown: on the left *V*bias = -100 V, on the right *V*bias = -200 V.

Inter-pad resistance for unirradiated sensors is very high, of the order of magnitude of $\sim 10^3 - 10^4 G\Omega$. Conversely, inter-pad resistance for irradiated sensors is much less, of the order of magnitude of $\sim 10 - 10^2 G\Omega$.

A clear trend does not appear for irradiated sensors with different fluences, except for the measurement with fluence $30 \times 10^{14} n_{eq}/cm^2$, which seems lower than the other fluences. In summary, the radiation damage affects the inter-pad resistance by lowering it and, therefore, by lowering the pad isolation. However, the inter-pad resistance for irradiated sensors is still very high.

It is interesting to focus on unirradiated sensors. An inter-pad resistance of $R_{int} \sim 10^3 G\Omega$ with a $\Delta(\Delta V) = 20 V$, means that a current of $\Delta(I_{int,1} - I_{std,1}) = \Delta(\Delta V)/R_{int} \sim 20 pA$ has been measured, according to equation 3.5. This current value is of the same order of magnitude as the apparatus noise; hence the R_{int} measured values are not very significant.

A difference in *Vbias* does not affect the measurements. The two trends with Vbias = -100 V and Vbias = -200 V are quite similar, and the same holds for the absolute values. When *Vbias* is not indicated in the following plots, the mean between the two values with different *Vbias* is implicit.

The other operating condition under investigation is the temperature *T*. The results are shown in the figure 3.43. Also here, the y-axis has a logarithmic scale. Here V bias = -200 V for both plots, but the same results could be obtained for the V bias = -100 V.



FIGURE 3.43: Inter-pad resistance from UFSD3.1 wafer 14. Two different *T* are shown: on the left T = 24 °C, on the right T = -20 °C.

The general trend is the same as before both for T = 24 °C and for T = -20 °C. The unirradiated sensors have a very high inter-pad resistance, while the irradiated sensors have a still high inter-pad resistance, but much less than unirradiated ones. The temperature affects the absolute values. In particular:

- unirradiated sensors have $R_{int} \sim 10^3 10^5 G\Omega$ when T = 24 °C and $\sim 10^3 10^4 G\Omega$ when T = -20 °C;
- irradiated sensors have $\sim 10^{-2} 1 \ G\Omega$ when $T = 24 \ ^{\circ}C$ and $\sim 1 10^2 \ G\Omega$ when $T = -20 \ ^{\circ}C$.

The measured inter-pad resistance changes about two orders of magnitude when the temperature lowers from T = 24 °C to T = -20 °C. The inter-pad current measured can be seen as the sum of an ohmic current, purely due to the ohmic resistance, and a thermal current, related to the leakage current:

$$I_{inter-pad} = I_{ohmic} + I_{thermal}.$$
(3.8)

The latter has a strong dependency upon the temperature. As already mentioned in section 2.3, the leakage current reduces by a factor of two when the temperature is lowered by $T_{step} \simeq 7 \,^{\circ}C$. When the temperature drops from $T = 24 \,^{\circ}C$ to $T = -20 \,^{\circ}C$, there is a total difference of $\Delta T = 44 \,^{\circ}C$, hence the leakage current reduces of $2^{\Delta T/T_{step}} \simeq 78$ times. This result is coherent with the observed drop of about two orders of magnitude of the measured inter-pad resistance. The conclusion is that the thermal current is the largest contribution at room temperature.

The termic contribution can be lowered by lowering the temperature, as it is shown in figure 3.44. The plot shows the measured inter-pad resistance as a function of the temperature for a type 10 sensor of the UFSD3.2 production, wafer 14, irradiated with $8 \times 10^{14} n_{eg}/cm^2$.

At low temperature ($T \le -20$ °C), a plateau is visible, and the measured interpad resistance settles around a value of ~ 100 G Ω . The conclusion is that the measured inter-pad resistance is asymptotic to the ohmic inter-pad resistance when the temperature is lowered because the thermal contribution becomes smaller and smaller. In general, the measured value has to be considered a lower limit to the inter-pad resistance.



FIGURE 3.44: Inter-pad resistance as a function of the temperature for a type 10 sensor of the UFSD3.2 production, wafer 14, irradiated with $8 \times 10^{14} n_{eq}/cm^2$.

A low temperature measurement limits the thermal contribution and is the relevant one for the ETL sensors characterization. In the following plots, all the inter-pad resistance shown have been measured with T = -20 °C.

Finally, it is possible to compare different wafers from the same productions: wafer 13, wafer 14, and wafer 18 from UFSD3.1. The results are shown in figure 3.45.



FIGURE 3.45: Comparison of the inter-pad resistances of UFSD3.1 wafer 13, wafer 14 and wafer 18.

The inter-pad resistances from different wafers are compatible. All the three wafers have values of $\sim 10 - 50 \ G\Omega$, which indicates that sensors are well isolated. The conclusion is that a different p-stop dose does not influence the inter-pad resistance value.

HPK2

For the HPK2 production, the same method as before is used. A direct comparison between different *Vbias* and different temperatures has been carried out, and the results are very similar to the one obtained from UFSD3.1. There is no dependence of the inter-pad resistance for the *Vbias*, and dependence for the temperature. These are features of the measurement method and not of the different sensors.

A summary of the results obtained from HPK2 production is shown in figure 3.46.



FIGURE 3.46: Inter-pad resistance from HPK2 wafer 37. Here the measures are the mean between the ones obtained from *Vbias* = -100 V and *Vbias* = -200 V, while T = -20 °C.

The same trend as UFSD3.1 measurements appears. The overall inter-pad resistance values are of the same order of magnitude as the UFSD3.1 sensors. The type SE5 IP5 (the one in green in figure 3.46) has a lower inter-pad resistance than the other types on average. In particular, this is visible with the highest fluence of $2.5 \times 10^{15} n_{eq}/cm^2$, where inter-pad resistance of SE5 IP5 is about two order of magnitude lower. It is interesting to notice that the previous study concludes that SE5 IP5 is the least resilient to floating pads. The two results suggest that SE5 IP5 has a less robust design than the other HPK2 types.

Conclusions

In this work, a detailed characterization of the latest Ultra-Fast Silicon Detector (UFSD) productions has been performed. UFSDs are silicon sensors based on the novel Low Gain Avalanche Diode (LGAD) technology with a thin thickness, which ensures good time resolution ($\sim 30 \ ps$) and high radiation tolerance (up to $2.5 \times 10^{15} \ n_{eq}/cm^2$). UFSDs were chosen to instrument the future Endcap Timing Layer (ETL) of the MIP Timing Detector (MTD). The MTD will be one of the main upgrades of the Compact Muon Solenoid (CMS) during the High-Luminosity Large Hadron Collider (HL-LHC) lifetime.

The latest UFSD productions called *UFSD3.1* and *UFSD3.2* from Fondazione Bruno Kessler (FBK) and *HPK2* from Hamamatsu Photonics K. K. (HPK) have been studied in detail. The characterization is based on measurements performed in Torino's laboratory *Innovative Silicon Sensor Laboratory* and on data provided by FBK.

A direct comparison of the breakdown voltage of different inter-pad designs showed that the guard ring grid between each pad led to the most robust sensors. This design is also the least affected by floating pads. The resilience to floating pads has been evaluated through laboratory measurements. It has been observed that the predominant effect due to floating pads is the degradation of breakdown voltage for FBK sensors and the increase of noise of the IV characteristics for HPK sensors. The effects are minimal with the most robust design when there is only one pad floating.

The inter-pad resistance has been measured in the laboratory at low temperature $T \leq -20^{\circ}C$. All the measured sensors ($\simeq 50$) have a enough high inter-pad resistance when new ($\sim 10^4 - 10^6 G\Omega$) and after irradiation ($\sim 1 - 100 G\Omega$). No differences upon the inter-pad design neither differences upon the p-stop dose have been observed.

The uniformity studies showed a good overall uniformity of the UFSD3.2 production: $\sim 1 - 10\%$ for breakdown voltage, $\sim 5 - 15\%$ for leakage current, and $\sim 1 - 2\%$ for full depletion voltage. These values are aligned with the expected values for an R&D production. The single pad yield of the UFSD3.2 production was found to be 97.6% (too low for the production of large layout sensors).

In the second half of 2021, there will be another production from FBK, called *UFSD4*. This will be the last R&D production before the ETL sensors, and, therefore, some technological choices have to be made. The studies conducted in this thesis directly contributed to the finalization of the UFSD4 production.

Appendix A

List of the Main Contributions

This work has been presented in dedicated meetings of the CMS collaboration, meetings with vendors, and national conferences. Here is a list of the main talks where my work has been shown, either in detail or as part of the material. The presentations are given according to: meeting or conference name, date, speaker, title, and reference.

Dedicated Meetings of the CMS Collaboration

- ETL Meetings on Sensors and Modules, February 22, 2021, Roberta Arcidiacono, UFSD4 Production: Finalization of Requests, private meeting;
- *ETL Meetings on Sensors and Modules,* December 1, 2020, Roberta Arcidiacono, *Yield of UFSD3.2 and HPK2 Productions,* private meeting.

Meeting with Vendors

- *HPK Meetings*, February 25, 2021, Nicolò Cartiglia, *Feedback on HPK2 Performances*, private meeting;
- *TnTo Meetings,* November 23, 2020, Matteo Milanesio, *UFSD3.2 Bad Pads and Bad Structures on* 5 × 5 *Matrices,* private meeting;
- *TnTo Meetings*, September 20, 2020, Matteo Milanesio, *UFSD3.2 Type Inverted Studies*, private meeting;
- TnTo Meetings, September 6, 2020, Matteo Milanesio, UFSD3.2 Uniformity Studies, private meeting.

National Conferences

• 106 Congresso Nazionale Società Italiana di Fisica, September 13, 2020, Matteo Milanesio, Ultimi Sviluppi sui Rivelatori Veloci al Silicio UFSD [46].

List of Figures

1.1	Measured Peak Luminosity of the LHC during Run 1 and Run 2	5
1.2	Measured Integrated Luminosity of the LHC during Run 1 and Run 2	5
1.3	Luminosity Forecast of the HL-LHC	6
1.4	Ultimate Luminosity Forecast of the HL-LHC	7
1.5	Simulation of 140 Pileup Event in the CMS Tracker	8
1.6	Simplified View of the CMS Detector	9
1.7	Simplified View of the MIP Timing Detector	10
1.8	Simulation of the CMS Absorbed Dose	11
1.9	Cross-sectional View of the ETL	12
1.10	Design of a ETL Two-Sensors Module	13
1.11	Simplified Design of a ETL 16×32 Sensor	14
1.12	Simulation of Line Density and Line Density PDF of the LHC and	
	HL-LHC	15
1.13	Simulation of the Number of Tracks Incorrectly Associated with Hard	
	Primary Vertex for Different MTDs	15
		• •
2.1	Complete IV Characteristic of a <i>pn</i> Junction	21
2.2	Schematic View of a Traditional Silicon Sensor and a Low Gain Avalanche	
	Diode	22
2.3	Comparison of the Electric Field in Traditional Silicon Sensors and	
	LGADs	22
2.4	LGAD Current Signals Dependence to Gain and Thickness	23
2.5	Model of a Time-Tagging Detector for a UFSD	24
2.6	Gain vs Reverse Bias in $45 \mu m$ UFSD	25
2.7	Charge vs Reverse Bias in $45 \mu m$ UFSD	26
2.8	Examples of Safe, Intermediate and Aggressive JTE Design	27
2.9	UFSD3.1 Reticle and Water Layouts	29
2.10	UFSD3.2 Reticle and Wafer Layout	30
2.11	UFSD3.2 Version Layouts	31
2.12	HPK2 Water Layout	32
2.13	IV Characteristics of PiN and LGAD sensors	34
2.14	IV Characterization Setup	34
2.15	CV Characteristics of PiN and LGAD sensors	35
2.16	CV Characterization Setup	36
2.17	High Frequency CV and Quasi-Static CV Overlap	37
31	Three Different Shots of the LIFSD3 2 Production	11
3.1	Example of Identification of a LIESD3.2 Sonsor	41 12
33	LIFSD3.2 shot A 1: Example of IV Curves from Wafer 12	τ∠ 44
3.4	UESD3.2, shot A 1: Breakdown Voltage Man for Wafer 12	 11
35	UFSD3.2, shot A 1: Breakdown Voltage as a Function of the Type for	TT
0.0	Wafer 12	45
	THILE 14	TU

3.6	UFSD3.2, shot A.1: Types Comparison for Wafer 12	47
3.7	UFSD3.2, shot A.1: Comparison between Current Map and Break-	
	down Voltage Map for Wafer 4	48
3.8	UFSD3.2, shot A.1: Current Distributions at 100 V for Wafer 12	49
3.9	UFSD3.2, shot A.1: Guard Ring Leakage Current at 30 V for Wafers 4	
	and 7	50
3.10	UESD3.2, shot A.1: Breakdown Voltage of Different Types as a Func-	
	tion of the Thickness	51
3 11	UESD3 2 shot A 2 [·] Example of IV Curves for Wafer 4	52
3.12	UFSD3 2 shot A 2: Breakdown Voltage Map for Wafer 4	52
3.12	UFSD3.2, shot A 2: Comparison of Sensors for Water 4	53
3.14	UESD3.2, shot R: Matrix Simplified Layout and Single IV Curve Mea-	00
5.14	surement Detail	54
2.15	LIESD2.2 shot P. Example of IV Curries for Wafer 7	54
5.15 2.16	UESD2.2, shot D. Example of IV Curves for Water 7	- 33 EC
3.10	UFSD3.2, shot b: breakdown voltage Map for Wafer 7	56
3.17	UFSD3.2, Shot B: Comparison of Versions for Water 12 LGADS	57
3.18	UFSD3.2, shot B: Versions Comparison for Wafer 12 PiNs	57
3.19	UFSD3.2, Shot A.1 and Shot B: Comparison between Current Maps	-
	for Water 12	58
3.20	UFSD3.2, Shot B: Example of Bad Pads Counting	59
3.21	UFSD3.2, Shot B: Bad Pads Map and Breakdown Voltage Map for	
	Wafer 7	60
3.22	UFSD3.2, Shot B: Bad Pads Distributions for All Wafers	61
3.23	UFSD3.2, Shot B: Bad Pads Map for All Wafers	62
3.24	UFSD3.2, Shot B: Bad Pads Position Maps for All Wafers	63
3.25	UFSD3.2, Shot A.1: Example of CV Curves for Wafer 7	65
3.26	UFSD3.2, Shot A.1: Method Used to Extract Full Depletion Voltage	66
3.27	UFSD3.2, Shot A.1: Full Depletion Voltage Map for Wafer 7	67
3.28	UFSD3.2, Shot A.2: Full Depletion Voltage Map for Wafer 7	67
3.29	Layout of a 2×2 Pads Sensor	70
3.30	Floating Pads Studies Experimental Setup	71
3.31	UFSD3.2 Wafer 7 Typical IV with Floating Pads	73
3.32	UFSD3.2 Wafer 7 Breakdown Voltage with Floating Pads	73
3.33	UFSD3.2 Wafer 7 Breakdown Voltage Difference between Different	
	Floating Pads Configuration	74
3.34	HPK2 Wafer 28 and Wafer 43 IV Curves with Floating Pads	75
3.35	HPK2 Broken Sensor and Zoom of the Burn Mark	75
3.36	HPK2 W37 Example of IV Curves with Floating Pads	76
3.37	HPK2 Wafer 37 RMS Noise with 1 Floating Pad	77
3.38	HPK2 Wafer 37 RMS Noise with 2 Floating Pads	77
3.39	Inter-pad Current Expected with Inter-pad IV Characteristics	79
3 40	Standard IV Characteristic and Inter-pad IV Characteristics	80
3.41	Inter-pad Resistance Studies Experimental Setup	82
3.42	Inter-pad Resistance on LIFSD3 1 Wafer 14 at different Vhias	84
3/12	Inter-pad Resistance on UFSD3 1 Wafer 14 at different Vhias	85
3 11	Inter-nad Resistance as a Function of the Temporature	86
3/5	Inter-pad Resistance on LIESD3 1 Wafer 12 Wafer 14 and Wafer 18	86
3.40	Inter-pad Resistance on HPK2 Water 13, Water 14 and Water 10	00 97
0.40	111111111111111111111111111111111111	07

List of Tables

Comparison Between Significant HEP Worldwide Experiments	7
MTD Nominal Radiation Dose and Fluence	11
Summary of Main Features of the BTL and the ETL	12
Summary of Some Expected Impacts of the MTD on the CMS Physics	
Program	16
UFSD3.2, Shot A.1: Ratio $R_{BD} = RMS_{BD} / \langle V_{BD} \rangle$	46
UFSD3.2, Shot A.1: Ratio $R_I = \sigma_I / \mu_I$	49
UFSD3.2, Shot B: Ratio $R_I = \sigma_I / \mu_I$	58
UFSD3.2, Shot B: Yield of Good Sensors	62
UFSD3.2, Shot B: Bad Pad Probabilities	64
UFSD3.2, Shot A.1 and Shot A.2: Ratio $R_{FD} = \sigma_{FD}/\mu_{FD}$	68
Measured Sensors Within Floating Pads Characterization	72
Measured Sensors Within Inter-pad Resistance Characterization	83
	Comparison Between Significant HEP Worldwide Experiments MTD Nominal Radiation Dose and Fluence Summary of Main Features of the BTL and the ETL

List of Abbreviations

APD	Avalanche PhotoDiode
ASIC	Application-Specific Integrated Circuit
ATLAS	A Toroidal LHC AparatuS
BTL	Barrel Timing Layer
CE	High Granularity Calorimeter Endcap
CMS	Compact Muon Solenoid
CNM	Centro National de Microelectrónica
СоМ	Center of Mass
CV	Capacitance Voltage
ECAL	Crystal Electromagnetic CALorimeter
ETL	Endcap Timing Layer
ETROC	Endcap Timing ReadOut Chip
FBK	Fondazione Bruno Kessler
GUT	Grand Unified Theories
HEP	High Energy Physics
HL-LHC	High Luminosity Large Hadron Collider
HPK	Hamamatsu Photonics K.K.
HV	High Voltage
INFN	Istituto Nazionale di Fisica Nucleare
IV	Current Intensity Voltage
JTE	Junction Termination Extension
LEP	Large Eelectron Positron collider
LGAD	Low Gain Avalanche Diode
LHC	Large Hadron Collider
LS1	Long Shutdown 1 (same for LS2, LS3, LS4, LS5)
MIP	Minimum Ionizing Particle
MTD	MIP Timing Detector
PCM	Process Control Monitor
PDF	Parton Distribution Function
QCD	Quantum Chromo Dynamics
QSCV	Quasi Static Capacitance Voltage
R&D	Research & Development
RMS	Root Mean Square
SiPM	Silicon PhotoMultiplier
SMU	Source Measure Unit
SNR	Signal to Noise Ratio
SPS	Super Proton Synchrotron
SUSY	SUperSYmmetry
TDC	Time to Digital Converter
UFSD	Ultra-Fast Silicon Detector

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