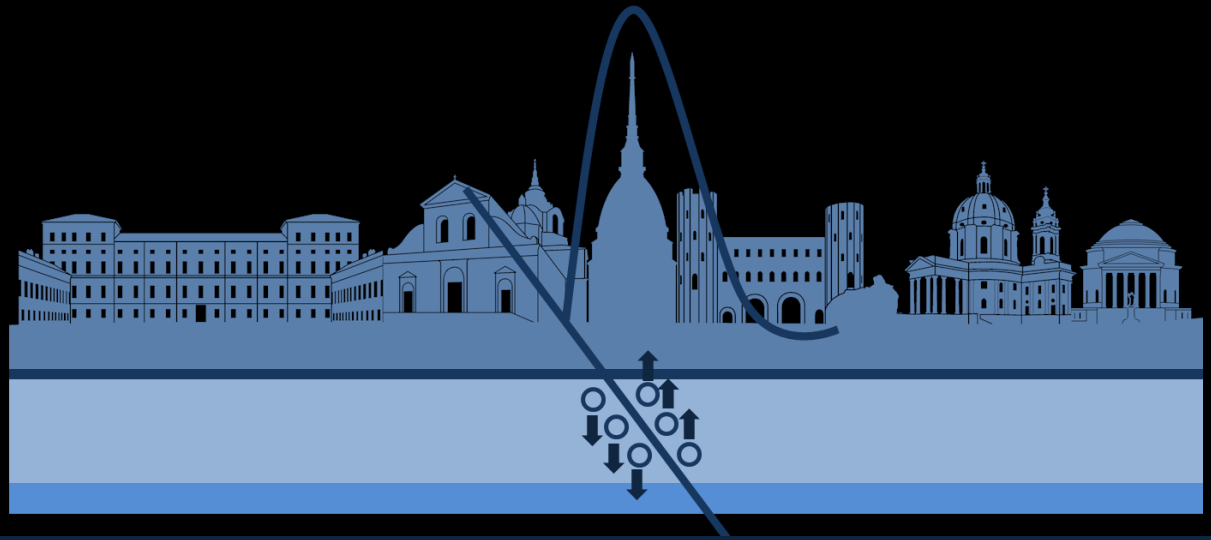
July 9th 2018



Front-End electronics optimization for time tagging with Ultra-Fast Silicon Detectors

Review of Front-End design

ST15
UFSD μe design

Federico Fausti, Jonhatan Olave
On behalf of the UFSD collaboration

INFN TORINO

Outline

- Introduction: Total Jitter
- Electronics Jitter:
  - Theory to minimize noise
  - Examples of suitable amplifiers
  - Technology choice: what is important?
  - Results with a CSA
- System sensor + very front end
  - Simulation with Landau noise + time walk + electronics jitter
- Future strategies

Introduction

Time resolution

$$\sigma_t^2 = \sigma_{LandauNoise}^2 + \sigma_{Distortion}^2 + \sigma_{Jitter}^2 + \sigma_{TDC}^2 + \sigma_{TimeWalk}^2$$

SENSOR ELECTRONICS

- $\sigma_{Landau\ Noise}$: *depends on the sensor thickness . For 55 um sensors is~ 30 ps*
- $\sigma_{Distortion}$:
  - *generated by the non – uniform weighting field.*
  - *Depends on the sensor dimension*
- σ_{Jitter} : *Depends on the very front – end*
- σ_{TDC} : *Depends on the TDC (internal or external)*
- $\sigma_{Time\ Walk}$: *Depends* on the signal amplitude variation, vth

$$\sigma_{Jitter}^2 = \left(\frac{t_{rise}}{S/N}\right)^2$$

$$\sigma_{TDC}^2 = \left(\frac{TDC_{bin}}{\sqrt{12}}\right)^2$$

$$\sigma_{TimeWalk}^2 = \left(\left[\frac{t_{rise}V_{th}}{S}\right]_{RMS}\right)^2$$

Introduction

Time resolution

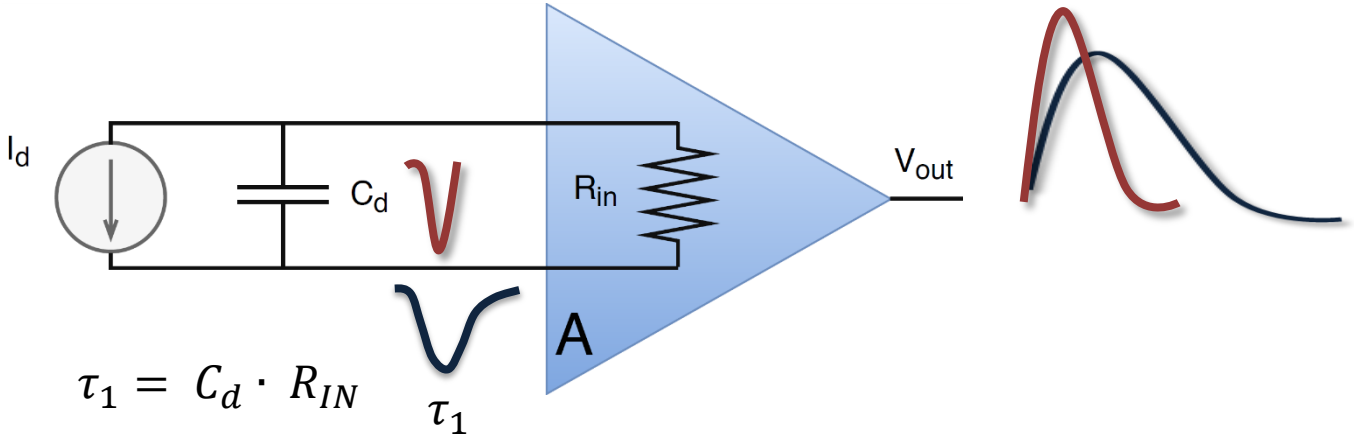
$$\sigma_t^2 = \sigma_{LandauNoise}^2 + \sigma_{Jitter}^2 + \sigma_{TimeWalk}^2$$

SENSOR + ELECTRONICS

More realistic simulations allow to have a better prediction of the performance obtained with a system sensor + electronics

Electronics Jitter

Theory to minimize noise



Rule: minimizing τ_1 as much as possible!!

If *Cd is fixed, the optimization must be done with Rin*

Electronics Jitter

Theory to minimize noise

Broadband:

- ***Rin can be low*** (50Ω) ***and thus it allows to preserve the input signal properties***
- ***Noise is higher*** $(\textit{than the CSA configuration})$

CSA:

- ***Rin is*** $\backsim \frac{1}{g_m}$ ***and thus it can not preserve the input signal properties. Cdet plays a fundamental role in the final time resolution. This is the optimal choise in case of having thick sensors or small pads***
- ***Noise is very low.***

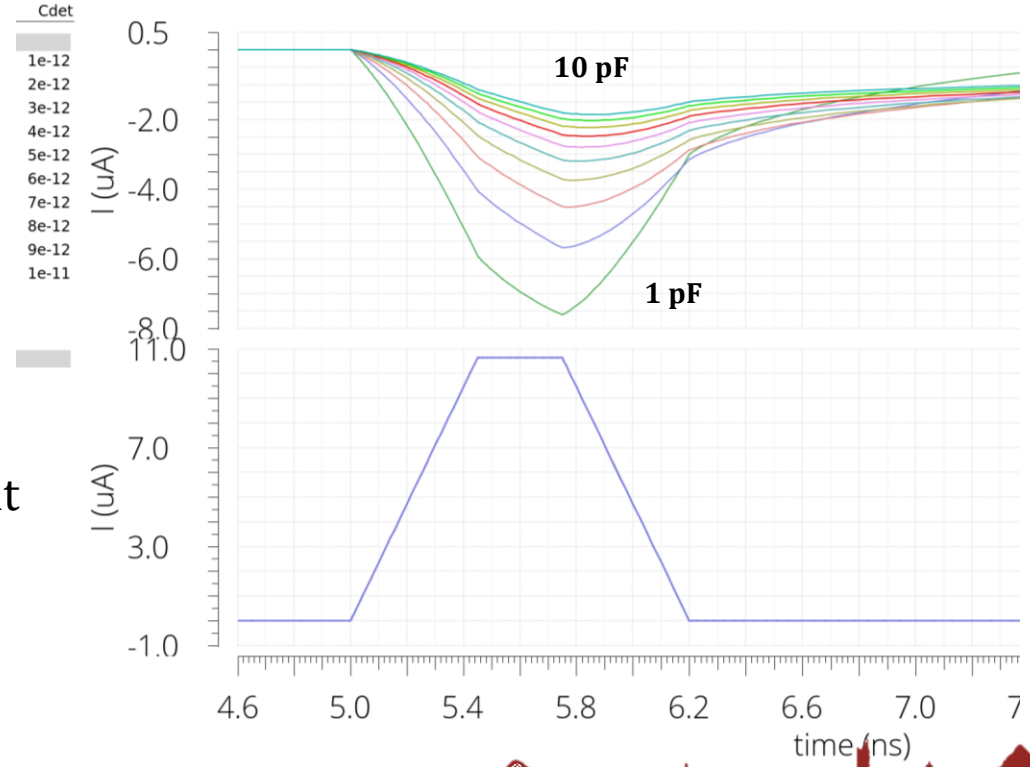
Electronics Jitter

Theory to minimize noise

CSA:

injected current

generated current

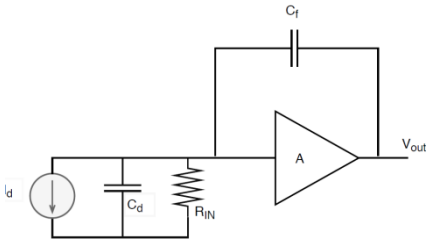


Electronics Jitter

Examples of suitable amplifiers

Capacitive feedback.

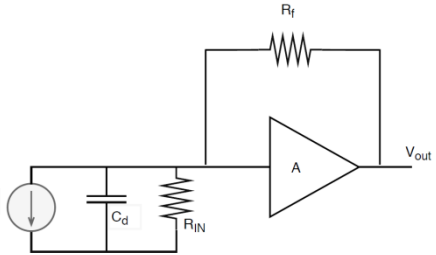
CSA



$V_{out} = -1/C_f \int i(t)dt$

Resistive feedback

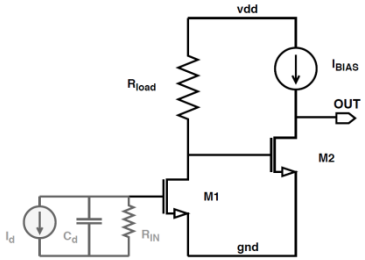
R_f_TIA



$V_{out} = -R_f \; i(t)$

Broad-Band

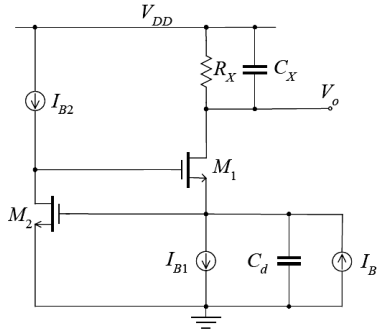
BB



$V_{out} = -(Z_{IN} \; i(t)) \; gm_1 \; R_{load}$

Regulated Common Gate

RCG



Vout (t) =

$$\frac{Q_{in}}{Cf} \frac{\tau_1}{\tau_1 - \tau_2} \left(e^{-\frac{t}{\tau_1}} - e^{-\frac{t}{\tau_2}} \right)$$

$$\tau_1 = \frac{C_d}{g_{m1} A} \qquad \tau_2 = R_X \, C_X$$

= Charge sensitive

= Current sensitive

Electronics Jitter

Technology choice: what is important?

Looking for a low-power, 20 ps Jitter VFE:

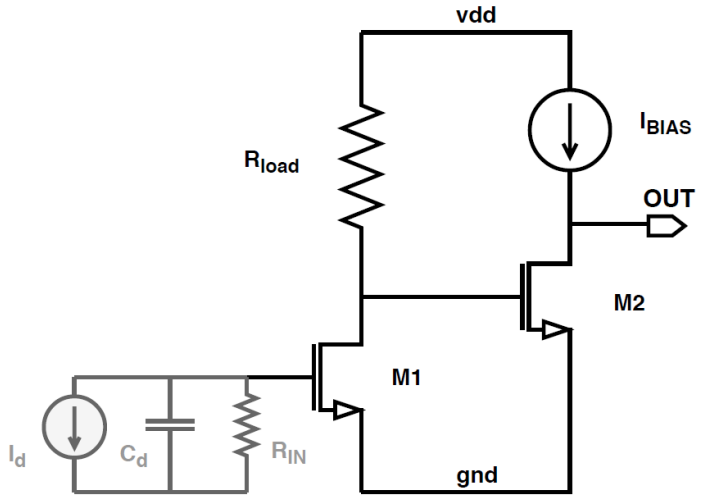
- Parasitics control → layout techniques
- Light architectures → minimum number of MOSFETs
- Low power → small MOSFETs → less parasitics → faster transients

$$\text{Area} \propto I_{bias}$$

- S/N optimization → larger g_m

Electronics Jitter
Technology choice: what is important?

- S/N optimization → larger g_m



Example: the **Broad-Band**

$$V_{out} = -(Z_{IN}\ i(t))\ g_m\ R_{load}$$

$$\sigma^J_t = \frac{t_r}{V_{out}/_N}$$

$$\delta_{Jitter} \sim \sqrt{\frac{T_C^2 + T_r^2}{T_r}} \cdot \frac{C_d \cdot \sqrt{T}}{\sqrt{g_m}}$$

$$\min \delta_{Jitter} \rightarrow T_c = T_r$$

Electronics Jitter

Technology choice: what is important?

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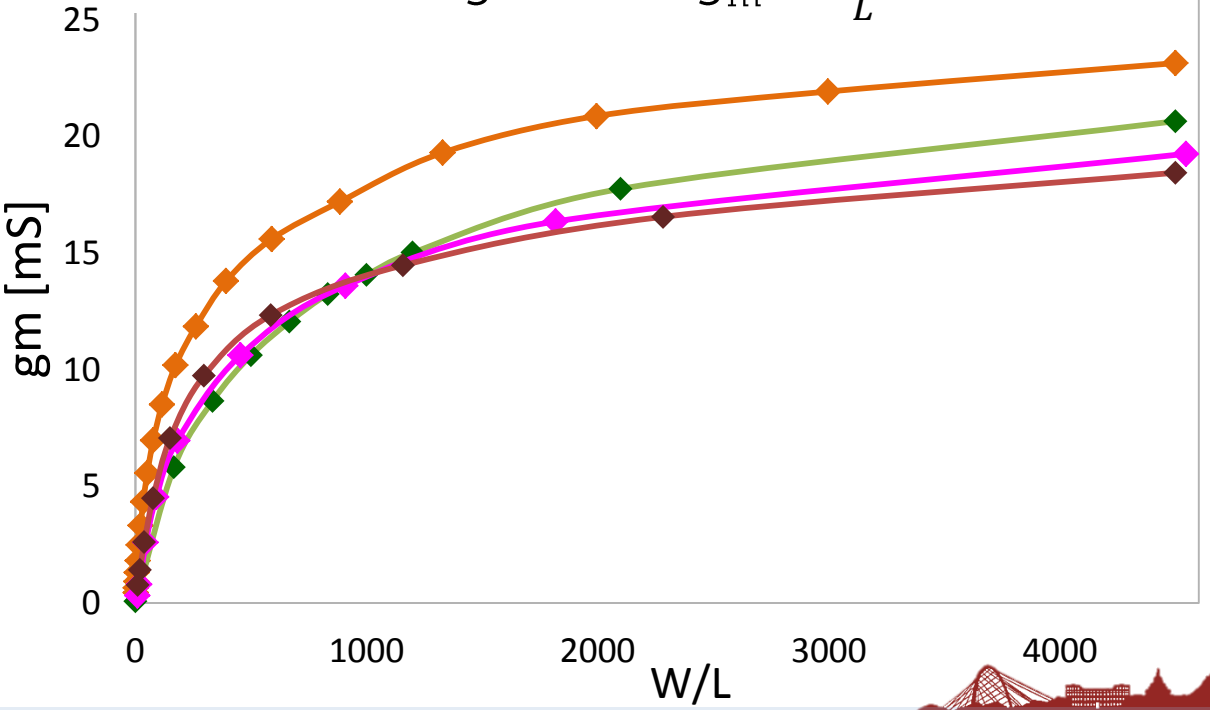
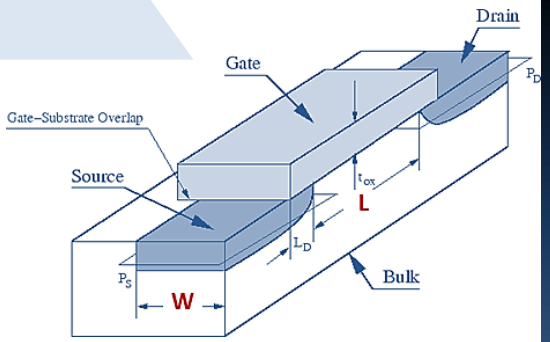
- Low power → small MOSFETs → less parasitics → faster transients
- S/N optimization → larger g_m
- Different technology nodes comparison → g_m scaling effect
  - 350 nm
  - 110 nm
  - 65 nm
  - 28 nm

Electronics Jitter

Technology choice: what is important?

NMOS scaling effect: g_m vs $\frac{W}{L}$

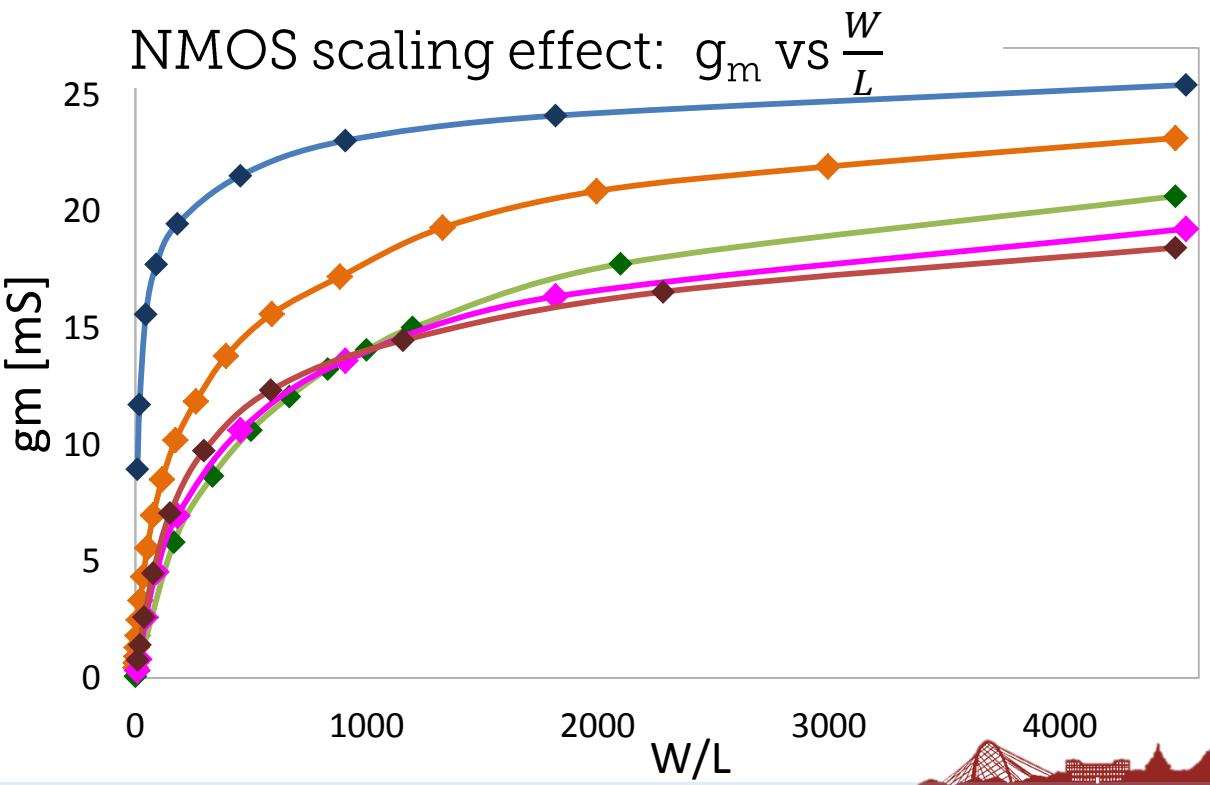


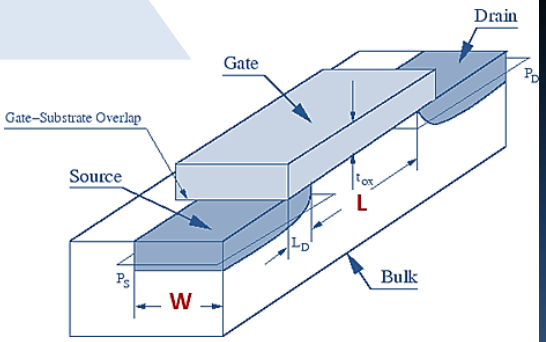


$$gm = \frac{\partial V_{GS}}{\partial I_{DS}} | V_{DS} = const$$

Electronics Jitter

Technology choice: what is important?





$$gm = \frac{\partial V_{GS}}{\partial I_{DS}} | V_{DS} = const$$

Electronics Jitter

Technology choice: what is important?

Looking for a low-power, 20 ps Jitter VFE:

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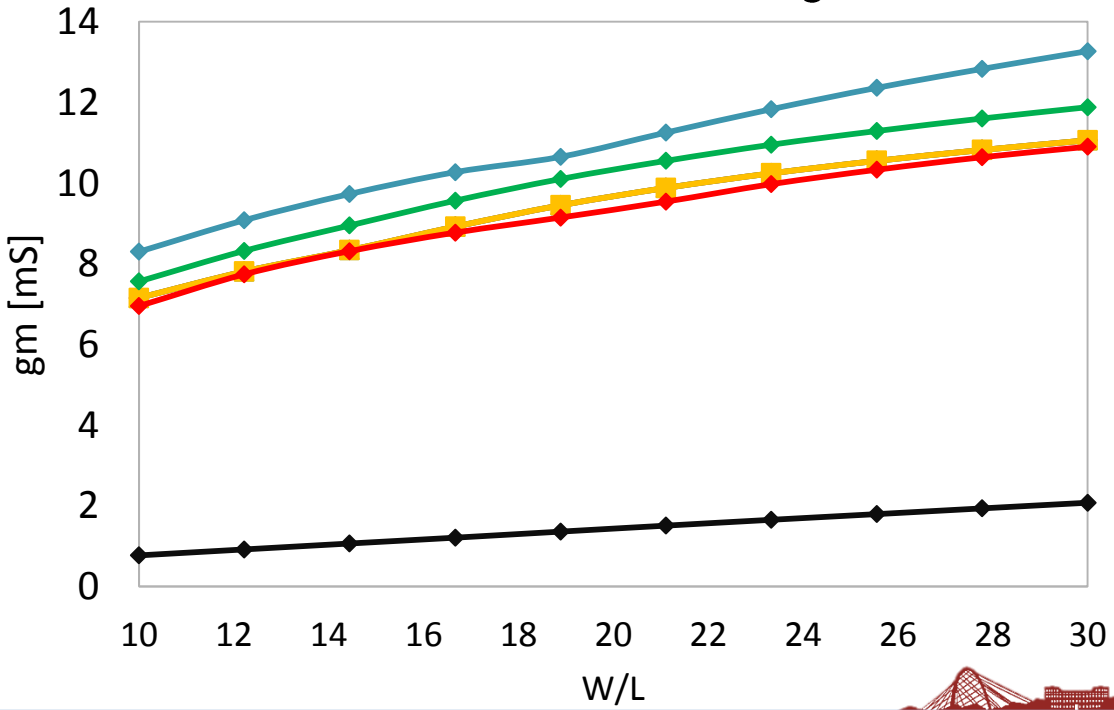
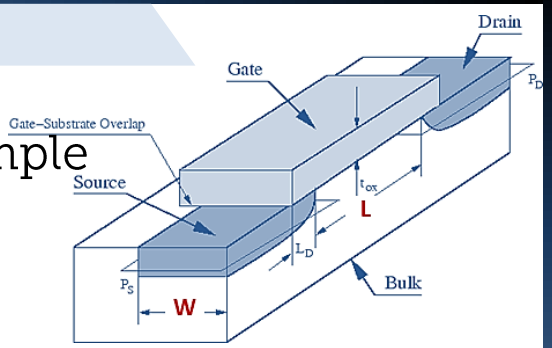
- Light architectures → minimum number of MOSFETs
- Low power → small MOSFETs → less parasitics → faster transients
- S/N optimization → larger gm
- Different technology nodes comparison → g_m scaling effect
- MOSFETs characterization for timing (RVT, LVT, HVT, RF…)

Electronics Jitter

Technology choice: what is important?

MOSFETs characterization for timing: the 65 nm example





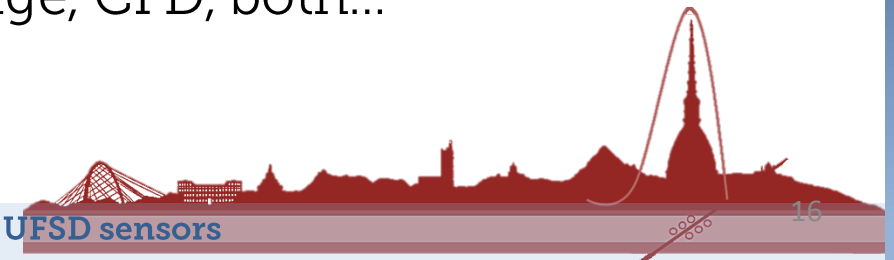
$$gm = \frac{\partial V_{GS}}{\partial I_{DS}} | V_{DS} = const$$

Electronics Jitter

Technology choice: what is important?

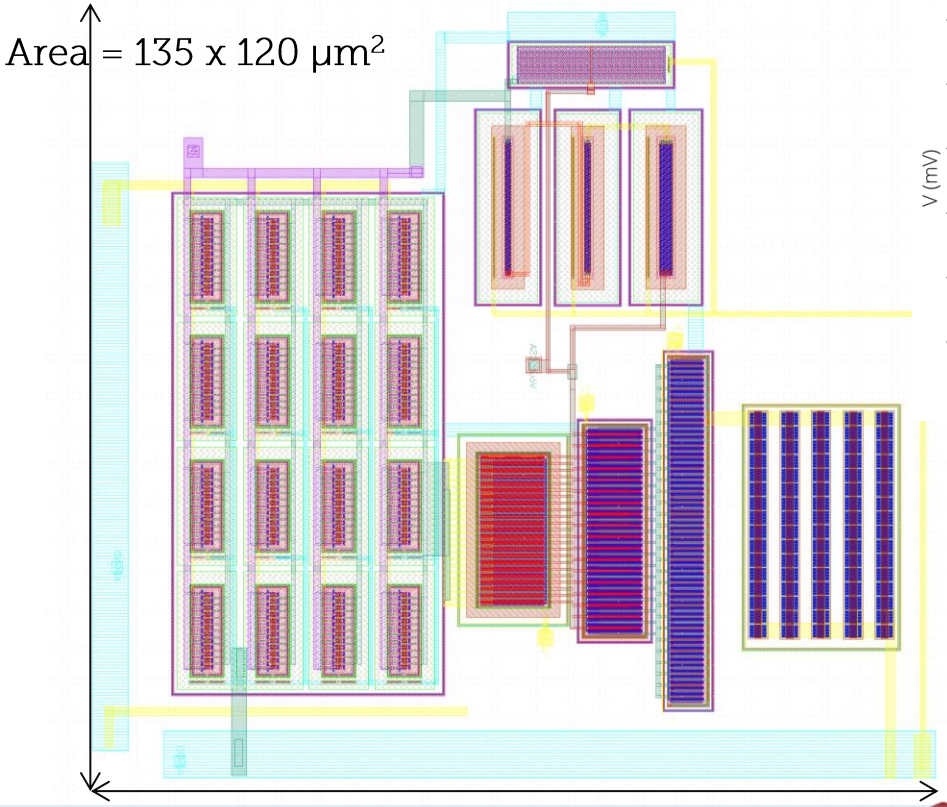
Looking for a low-power, 20 ps Jitter VFE:

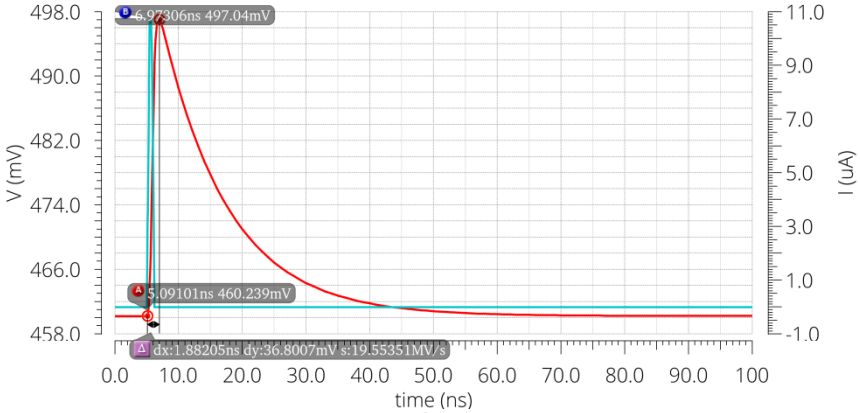
- Parasitics control → layout techniques
- Light architectures → minimum number of MOSFETs
- Low power → small MOSFETs → less parasitics → faster transients
- S/N optimization → larger g_m
- Different technology nodes comparison → g_m scaling effect
- MOSFETs characterization for timing (RVT, LVT, HVT, RF…)
- Discriminator type → leading edge, CFD, both…

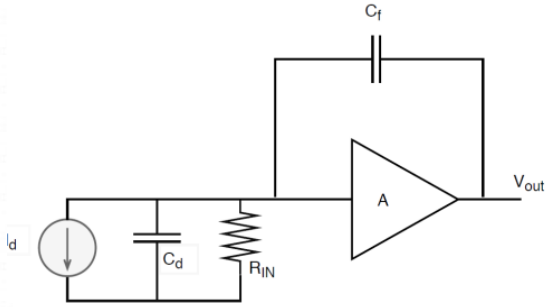


Electronics Jitter

Results with a CSA: schematic and layout







Electronics Jitter

Results with a CSA: different power budget

J vs Q_{in} , schematic level design

Qin [fC]	I_{bias} = 1mA	I_{bias} = 1.5mA	I_{bias} = 6mA	rmsNoise [uV]
3	41,8	36,4	24,4	335
4	31,3	27,2	18	347
6	20,8	18,1	11,7	285
8	15,5	13,5	8,6	
10	12,4	10,7	6,7	

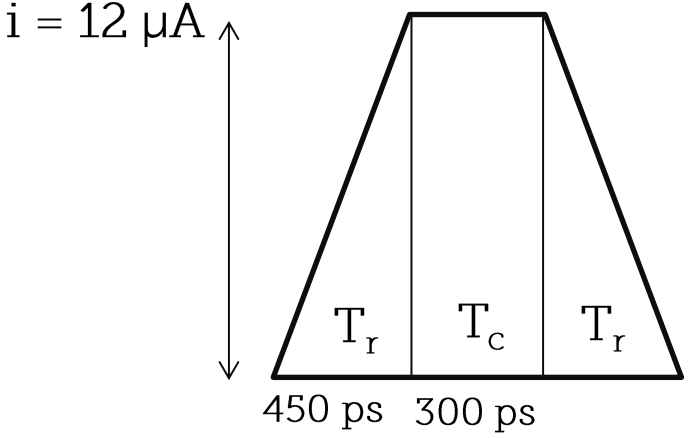
J [ps]

C_{det} = 6 pF

Electronics Jitter

Results with a CSA: simulation assumptions

Reference signal for a 50 μm sensor with gain 15



Q_{in} [C] = 75 e/h * d * G * 1.6 e-19

A = 9 fC

C_{det} [F] = 6 *1 e-12 * (50 /d)

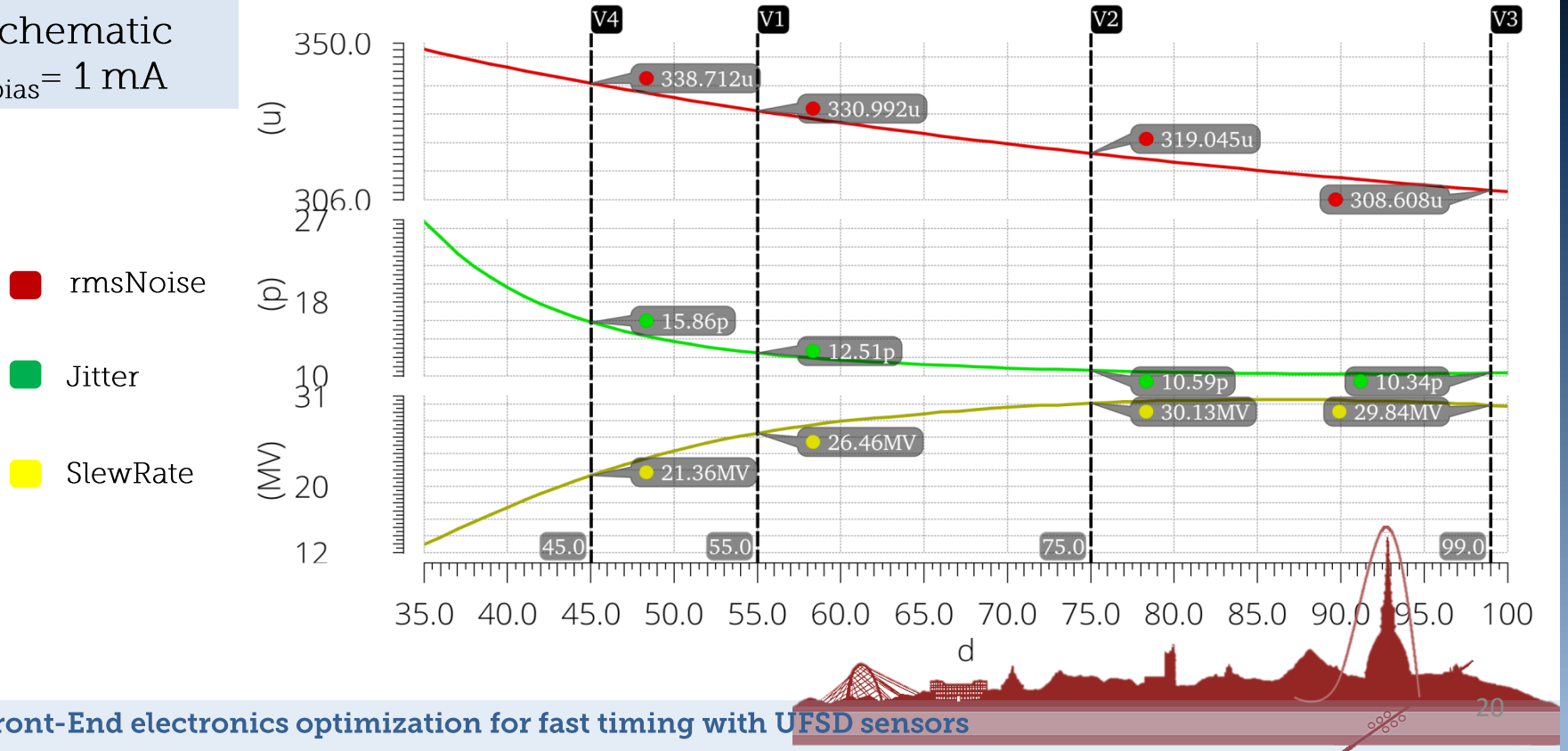
Relationship

T_c [s] = (d/50) * 1.2 ns

T_r [s] = (d/50) * 450 * 1 e-12

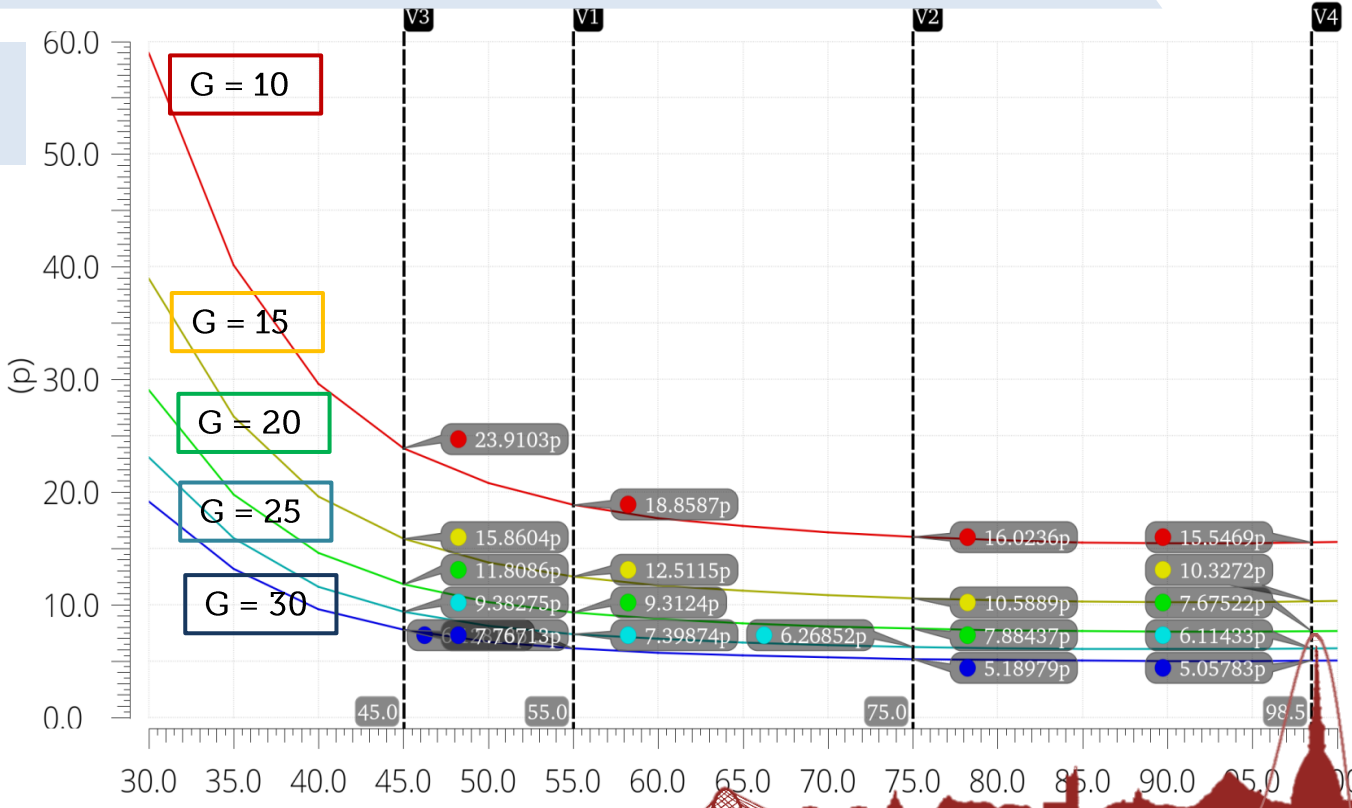
Electronics Jitter
Results with a CSA

Schematic
I_{bias}= 1 mA

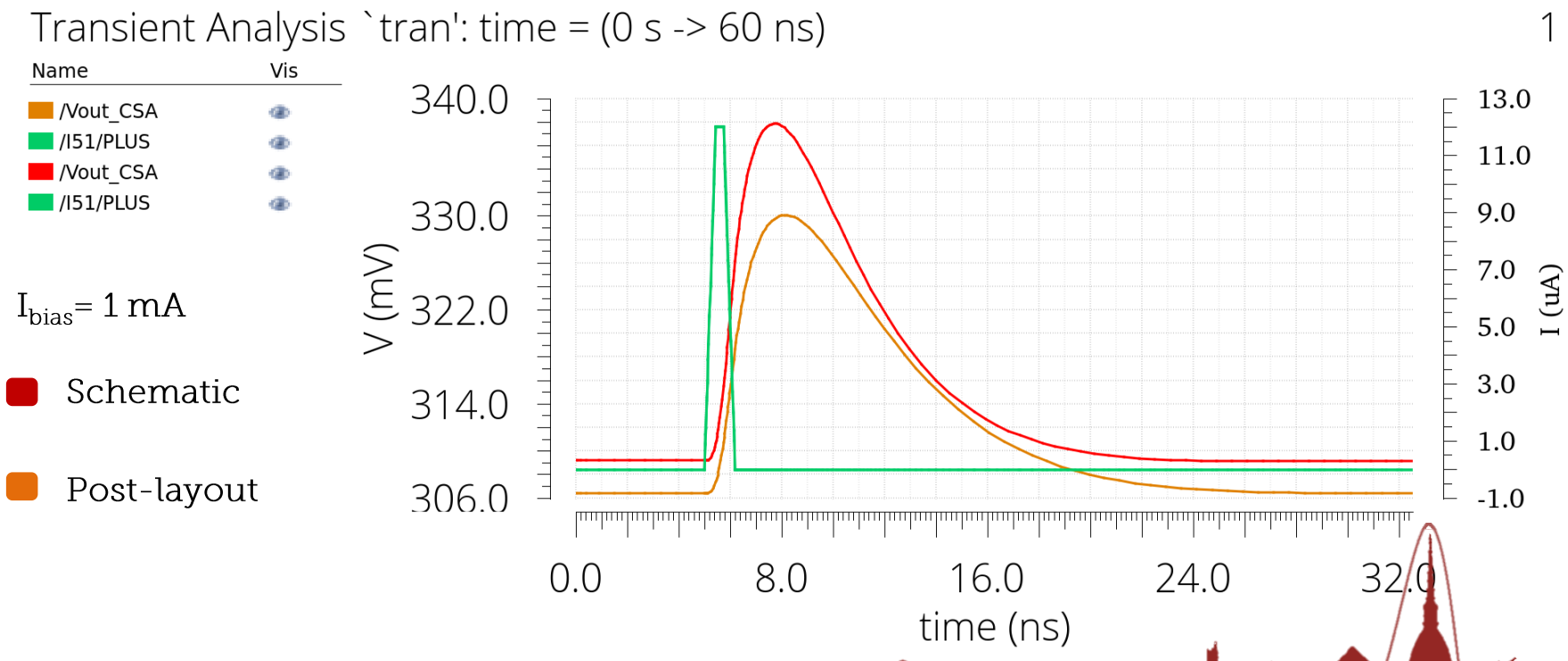


Electronics Jitter
Results with a CSA

Schematic
I_{bias}= 1 mA



Electronics Jitter
Results with a CSA



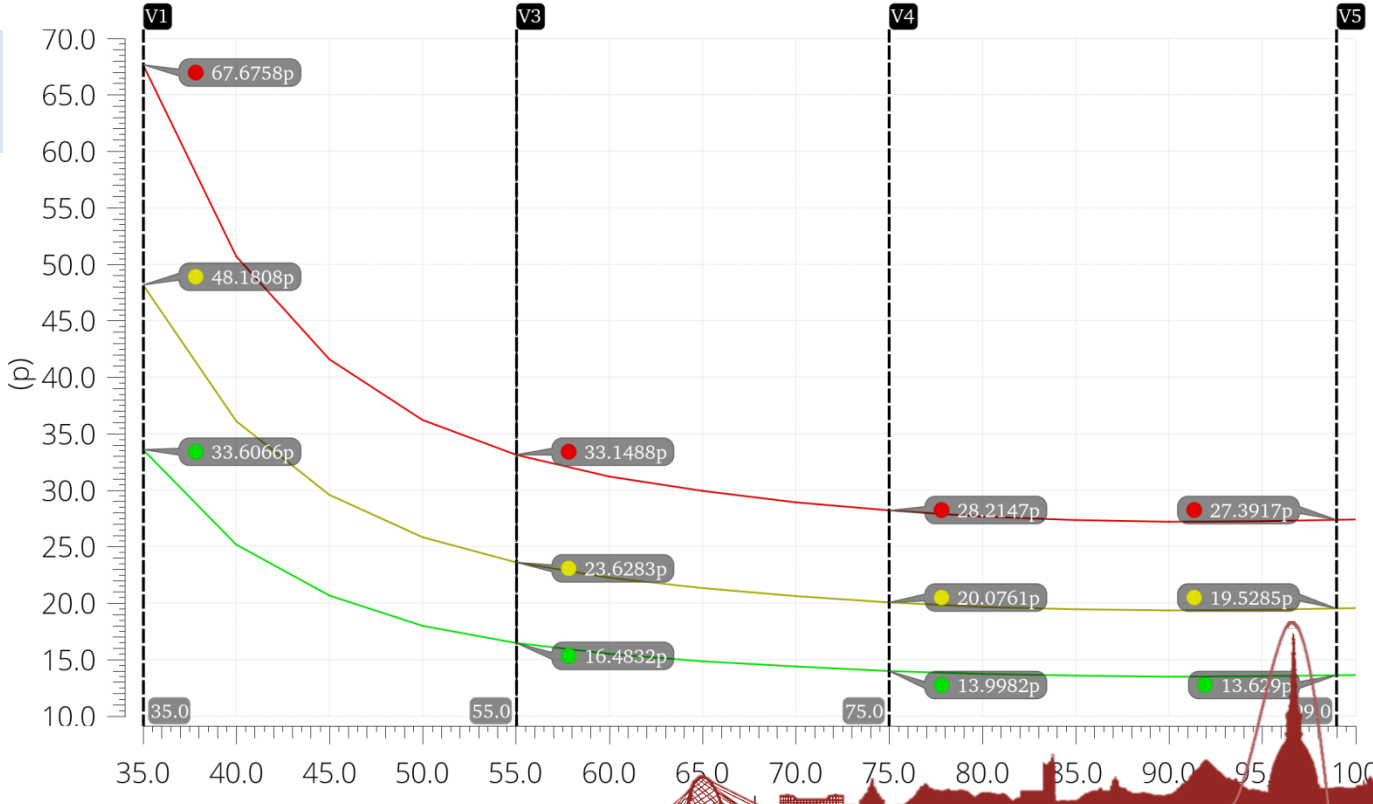
I_{bias}= 1 mA

Schematic

Post-layout

Electronics Jitter
Results with a CSA

Layout
I_{bias}= 1 mA



MPV * 0.5

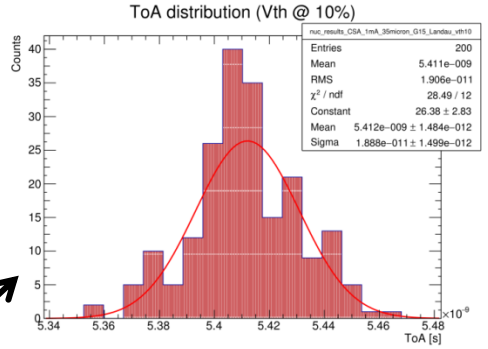
MPV * 0.7

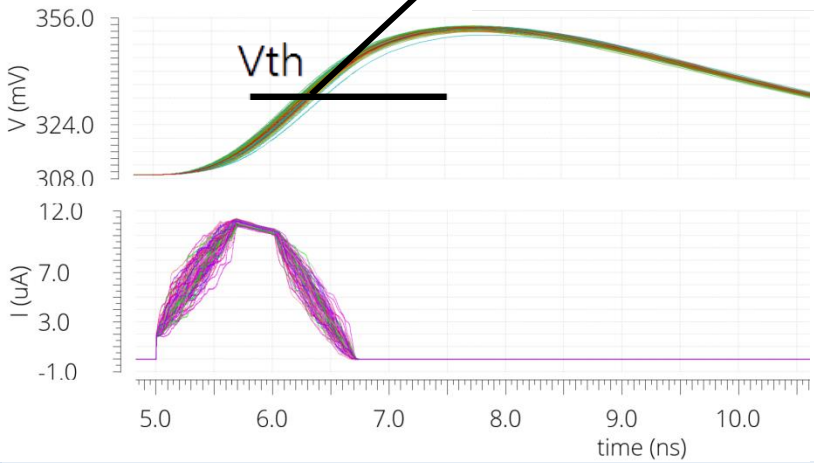
MPV

I_{bias}= 1 mA

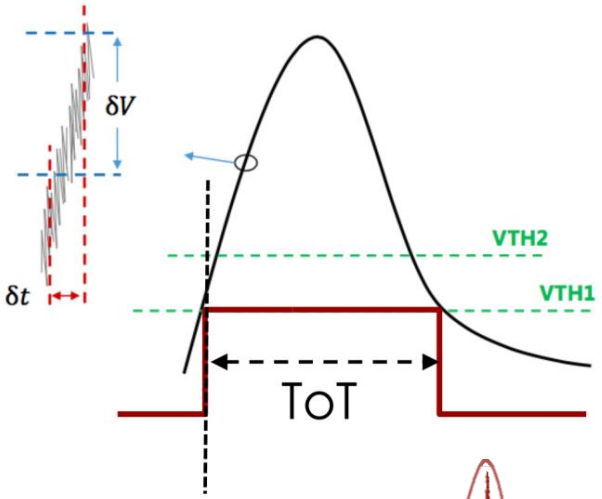
System sensor + very front end
Jitter simulations

$\sigma_{Landau\ noise}$



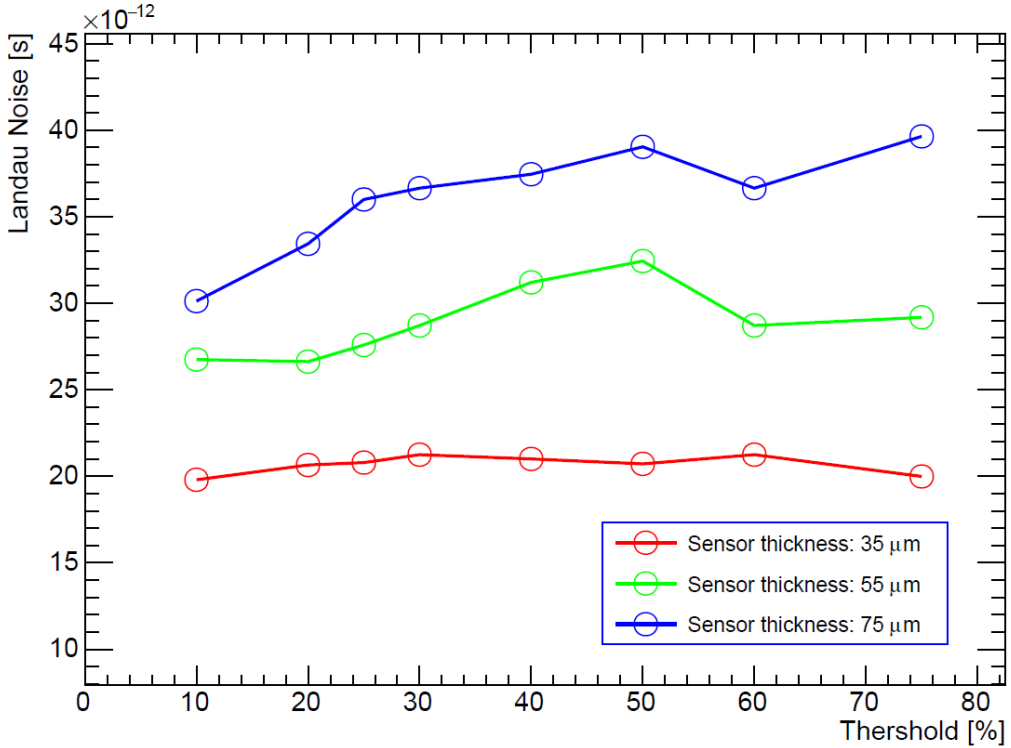


σ_{jitter}



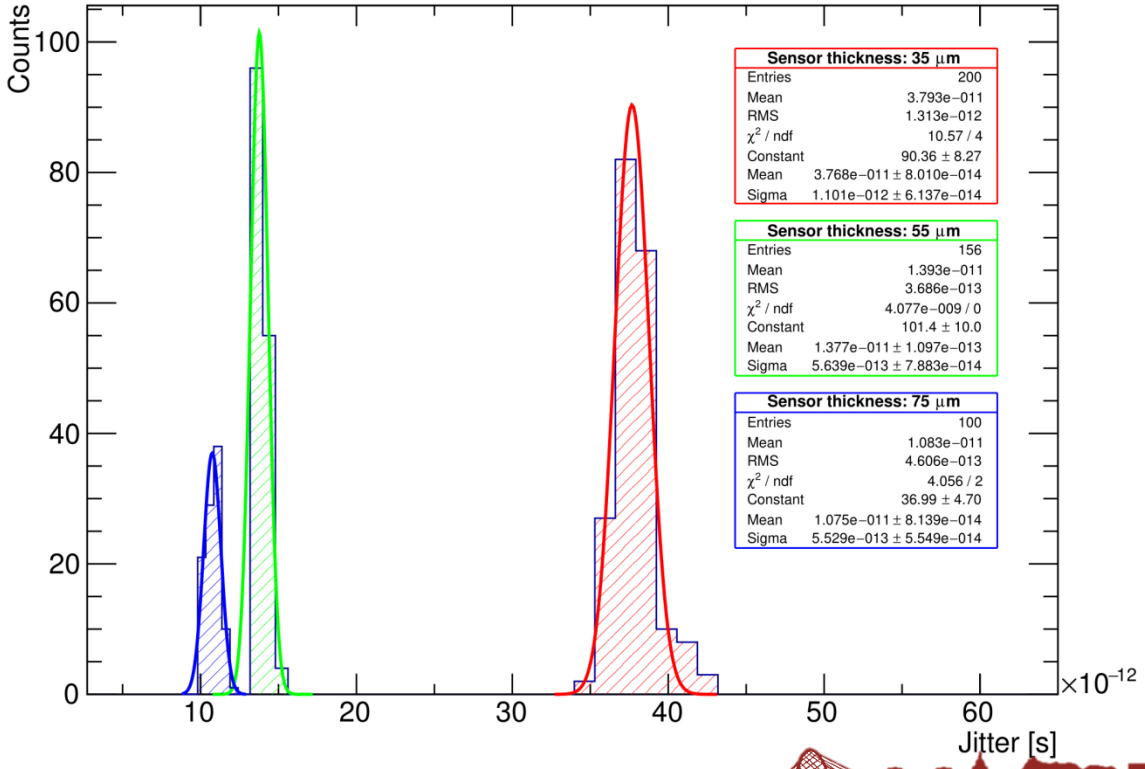
System sensor + very front end

Results with a CSA: Landau noise vs thickness



System sensor + very front end

Results with a CSA: Jitter vs thickness



System sensor + very front end

Results with a CSA: cumulative effect

$$\sigma_t{}^2 = \sigma_{Landau\ noise}{}^2 + \sigma_{Jitter}{}^2$$

Sensor thickness	Jitter
35 mu	42.5 ps
55 mu	31 ps
75 mu	35 ps

Future strategies

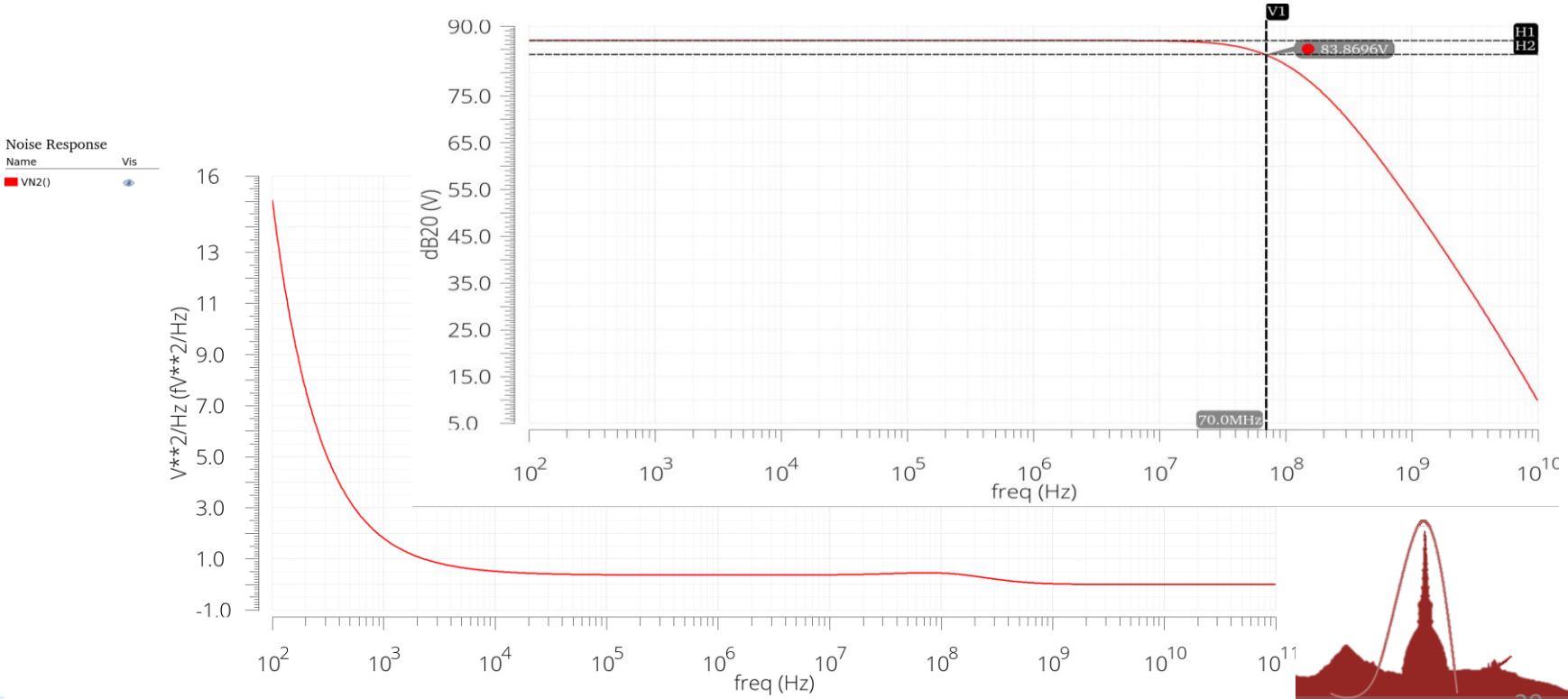
Design

- others preamplifier topologies (1mA)
- CFD + LE discriminators
- Full channel (Sept. 18)

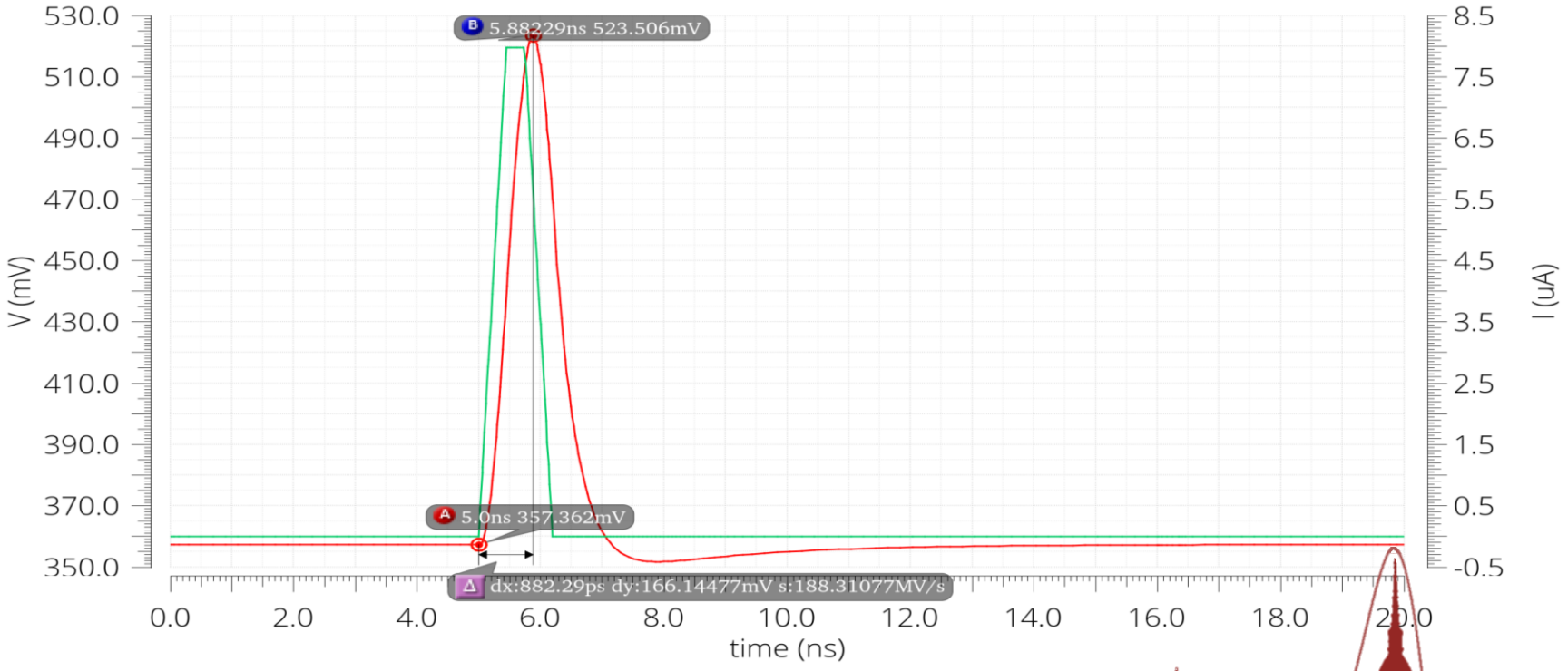
Simulation

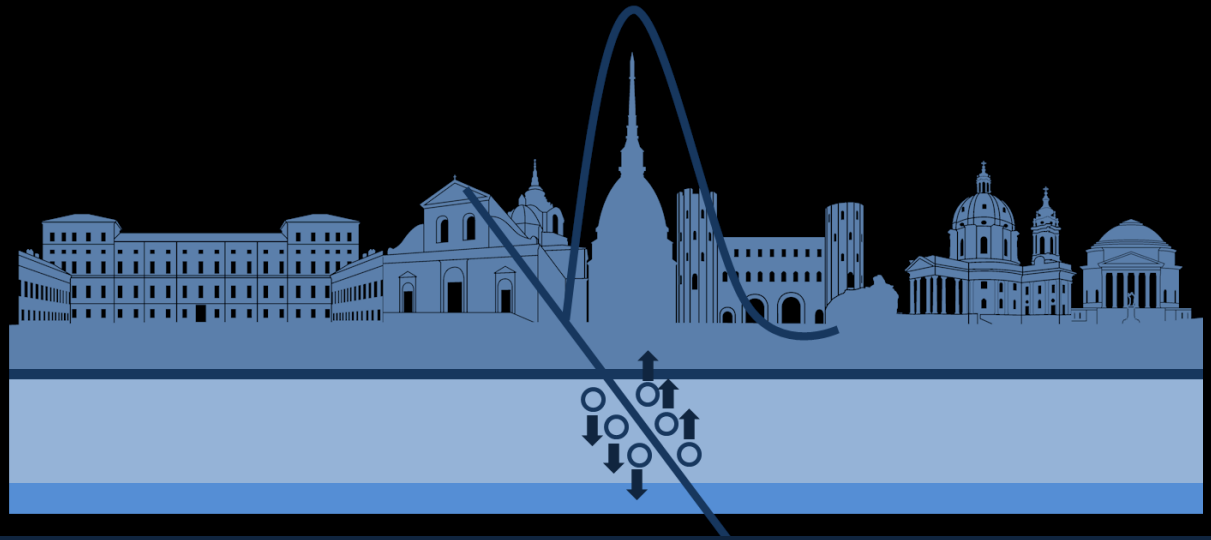
- Landau noise + TW + electronics noise (transient noise)
- Simulation with signals generated by irradiated sensors up to 3^15 neq/cm2
  - Set 1: generic un-irradiated UFSD sensors (n-in-p), fixed gain = 15:
  - Set 2: generic un-irradiated UFSD sensors (n-in-p), no time walk, fixed gain = 15:
  - Set 3: FPK W6: 55 microns, Boron+Carbon
  - Set 4: HPK G35: 35 microns, Boron

Future strategies
Pole-zero cancellation



Future strategies
Pole-zero cancellation





Thank you for your attention

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INFN – GruppoV
Horizon 2020 Grant URC 669529
Ministero degli Affari Esteri, Italy, MAE

ST15
UFSD μe design

INFN TORINO

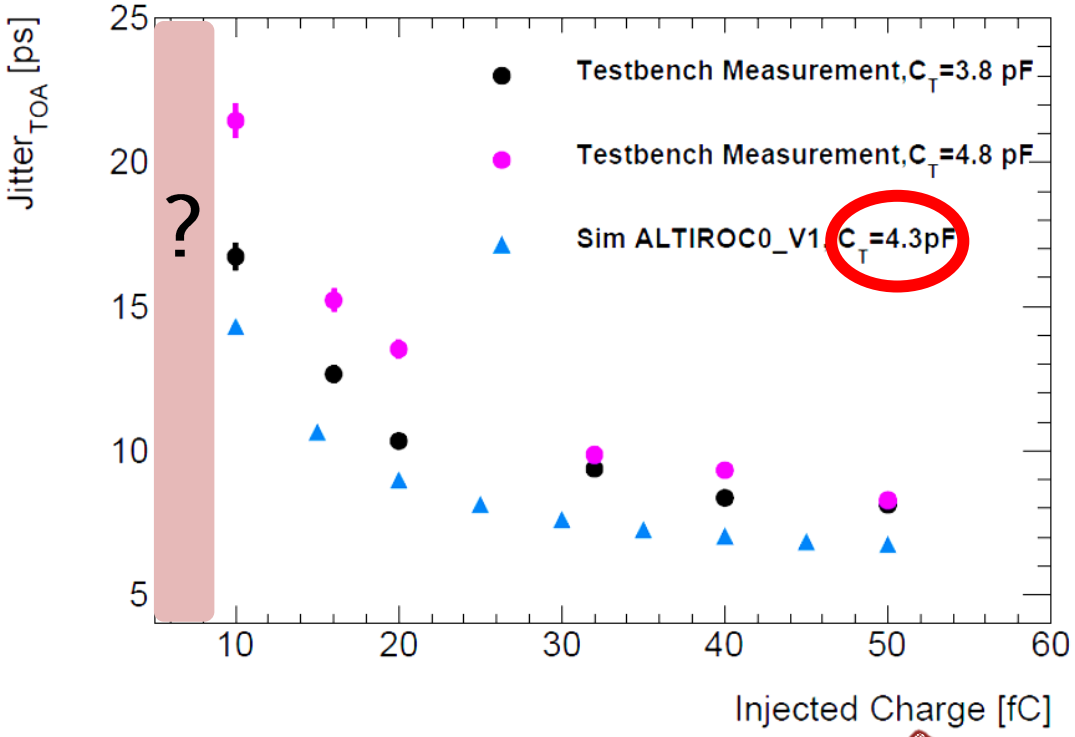
Backup

The ATLAS High Granularity Timing Detector for HL-LHC

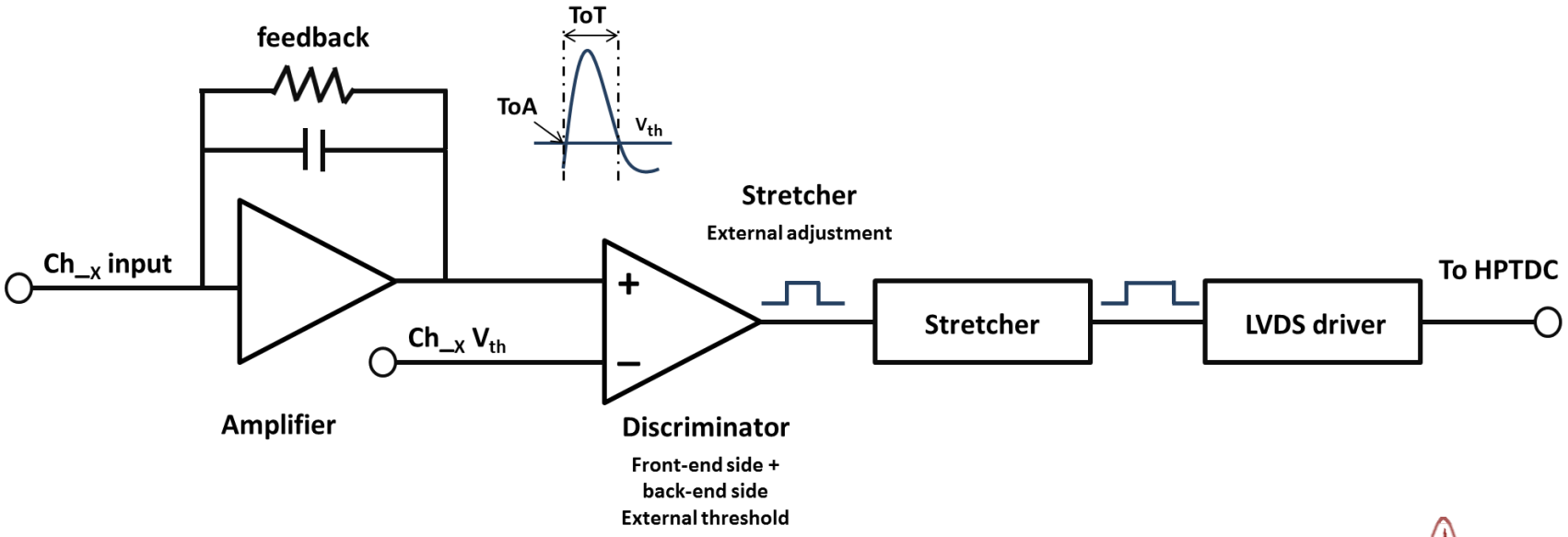
L. Serin (CNRS/IN2P3/LAL)

Institutes involved in HGTD : CERN, LPNHE, LAL, Omega (France), Mainz, Giessen (Germany), Casablanca (Morocco), IFAE, CNM (Spain), JSI (Slovenia), KTH (Sweden), Sinica Academia, National Tsing-Hua University (Taiwan), BNL, Stony Brook, Iowa, Ohio, SMU, SLAC, UCSC (US), JINR (Russia) +….

Most of the material is from the ATLAS HGTD TP to be made public mid June


Jitter$_{TOA}$ [ps]
25
20
15
10
5
?
Testbench Measurement,C$_T$=3.8 pF
Testbench Measurement,C$_T$=4.8 pF
Sim ALTIROC0_V1 C$_T$=4.3pF
10
20
30
40
50
60
Injected Charge [fC]

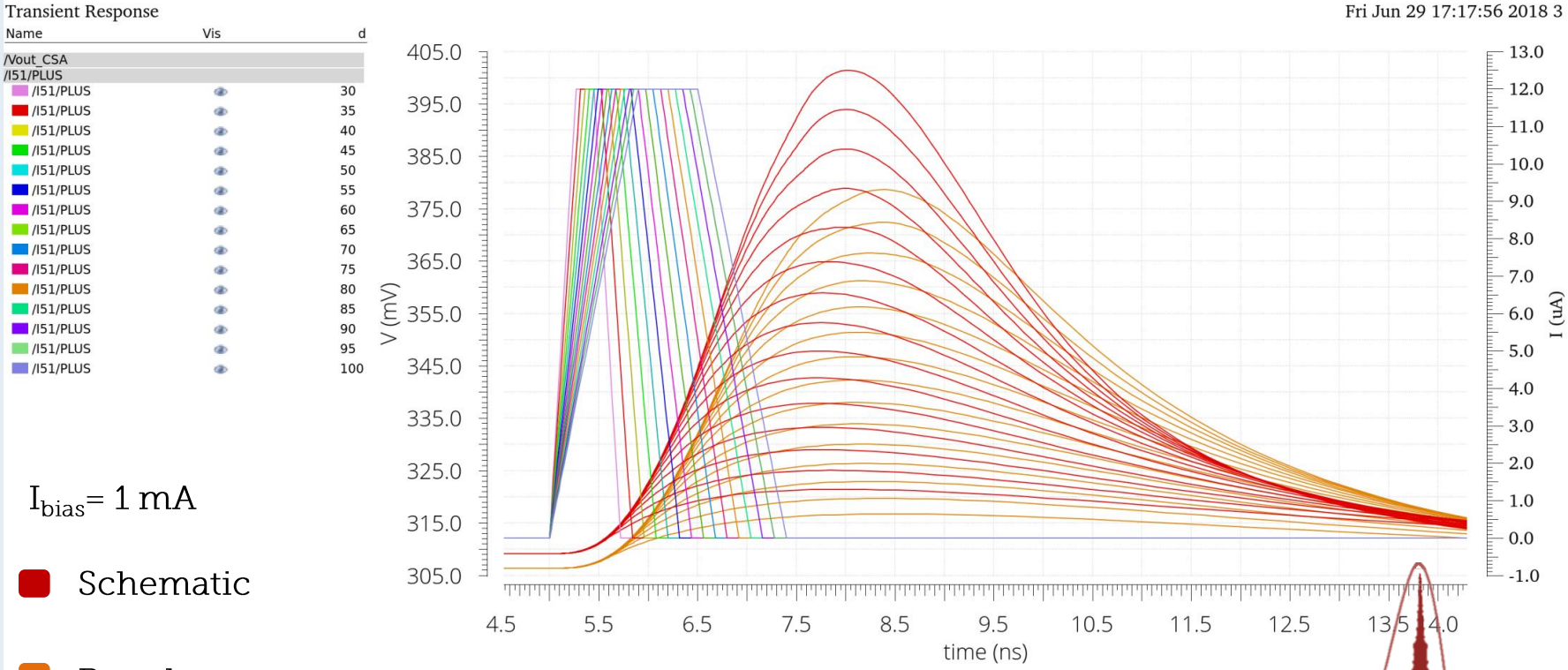
The TOFFEE Example



The TOFFEE Example: simulation outcomes

	BLOCK	JITTER [ps]			
CURRENT [mA]		2		12	
CHARGE [fC]		3	8	3	8
LAYOUT	Preamp	120	46	104	40
	Discriminator 1	132	47	106	39
	Discriminator 2	131	47	110	40
	Delay line	131	47	111	40
	LVDS	131	47	111	40
SCHEMATIC	Preamp	42	16	42	11
	Discriminator 1	52	17	53	12
	Discriminator 2	46	16	43	12
	Delay line	47	15	43	12
	LVDS	47	16	43	13

Case study: a fast CSA in 110 nm



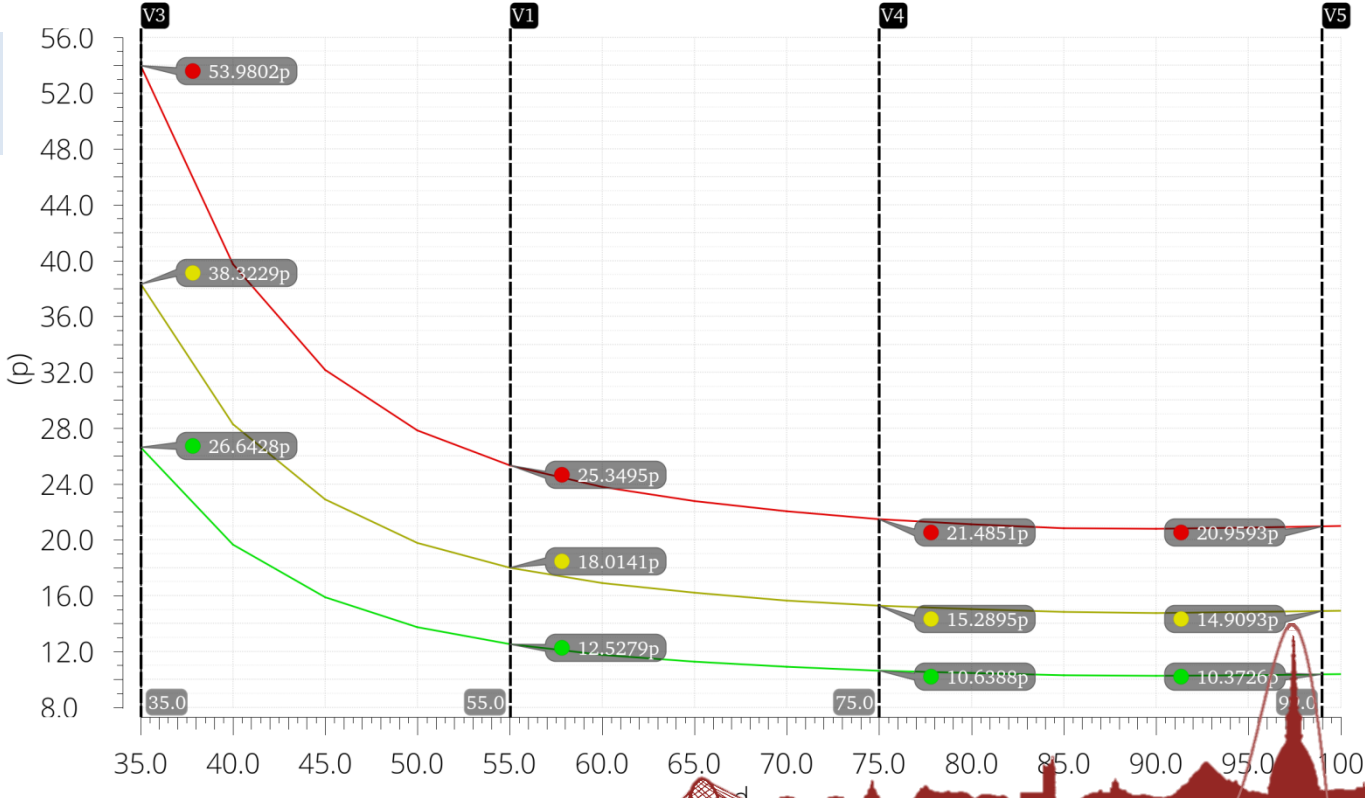
I_{bias}= 1 mA

Schematic

Post-layout

Electronics Jitter
Results with a CSA

Schematic
I_{bias}= 1 mA



MPV * 0.5

MPV * 0.7

MPV

I_{bias}= 1 mA