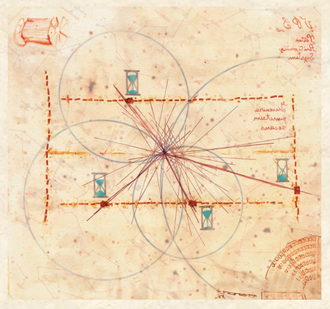
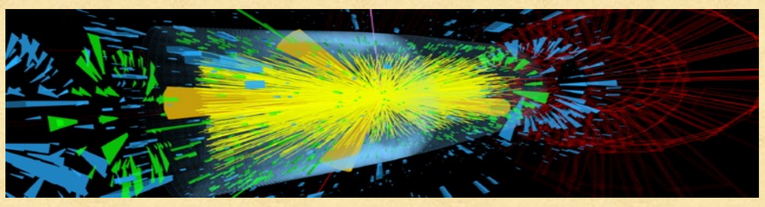
Present status and future perspectives of the Endcap Timing Layer for the CMS MTD

V. Sola on behalf of the CMS Collaboration



Motivations

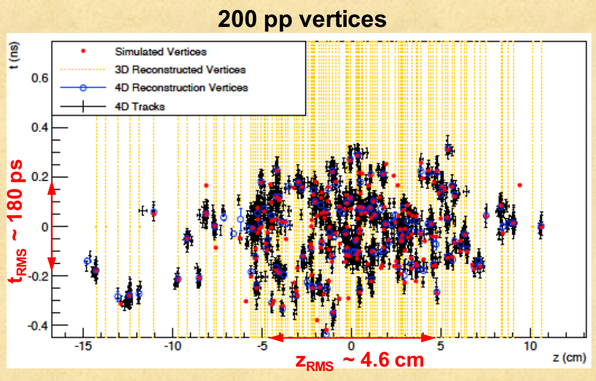


Simulation of a VBF H → ττ in 200 pile-up pp collisions

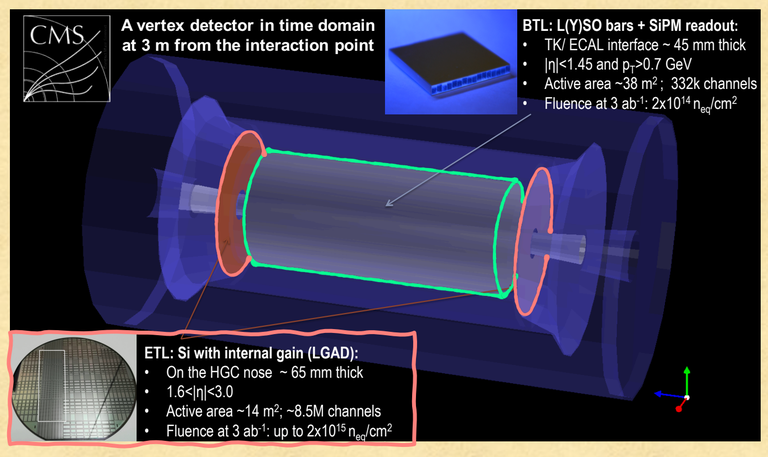
Conditions at HL-LHC very challenging
→ at the edge of tracker performances

Spread of ~180 ps in time collisions
→ slices of 35 ps will reject a factor of 5 more pile-up

200 pp vertices



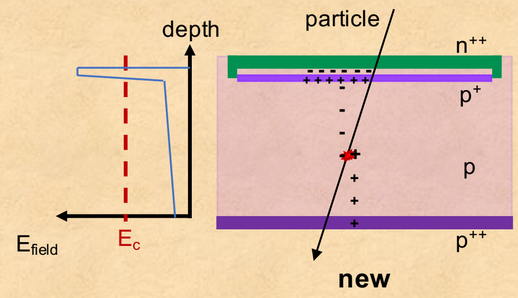
⇒ With 35 ps time resolution, instances of vertex merging are reduced from 15% in space to 1% in space-time, as in LHC operation



Starting from Run 4 (2029)[1] CMS will be equipped with a MIP Timing Detector[2]

The Endcap component will be equipped with ~ 14 m² of Low-Gain Avalanche Diodes[3]

Sensors

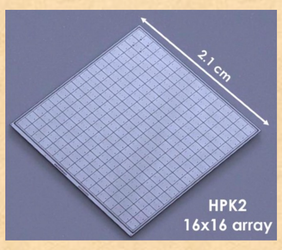


Low-Gain Avalanche Diodes (LGADs)

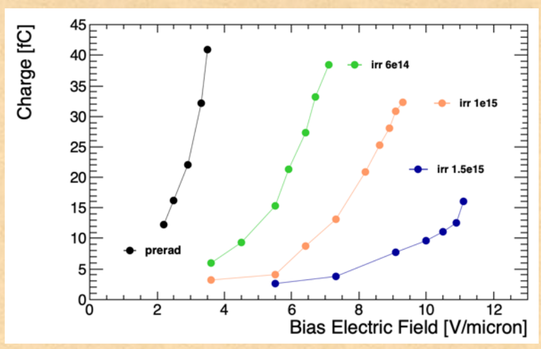
Impact ionisation occurs when $E_{field} > E_c = 25$ V/µm

In LGADS the E_{field} is above E_c for short distance well controlled by V_{bias}

With an active thickness of ~ 50 µm, timing resolution is of ~ 30ps[4]

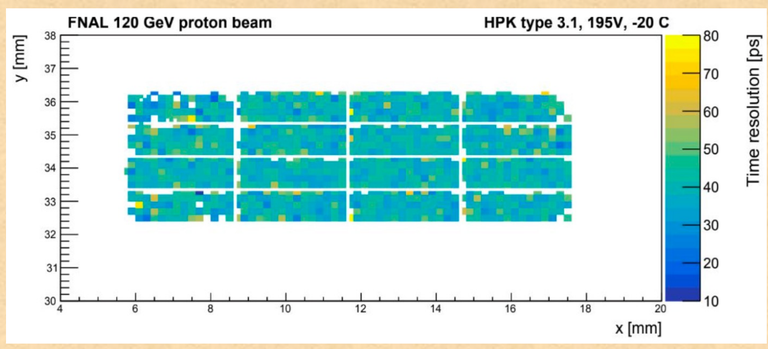


For ETL
16×16 pad sensors
1.3×1.3 mm² pad area



High collected charge with fluence from FBK sensors

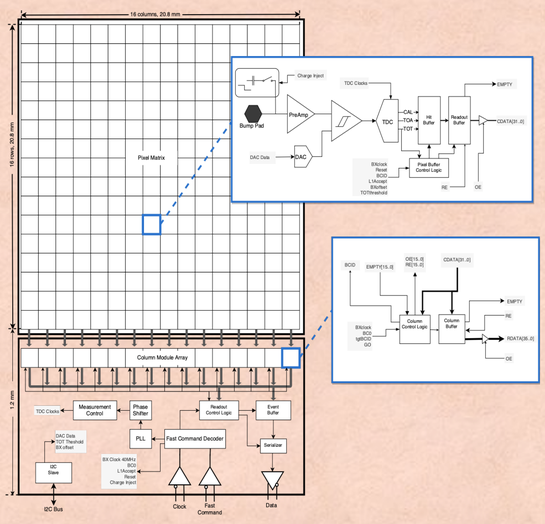
Many tests ongoing to:
- ▻ define the production parameters
- ▻ enhance the radiation tolerance
- ▻ check the production quality
- ▻ control the uniformity over big areas



Uniform timing resolution of HPK sensors

→ ETL sensor market survey almost complete
→ ETL sensor design choice in September 2023
→ ETL sensor production completion expected by mid-2025

Electronics



Endcap Timing ReadOut Chip (ETROC)[5]

- ▻ Extract precision timing from small LGAD signal (~5fC at end of life)
- ▻ Low power budget of 1W/chip, ~3 mW/channel → low power TDC
- ▻ ASIC contribution to time resolution < 40ps

Timeline

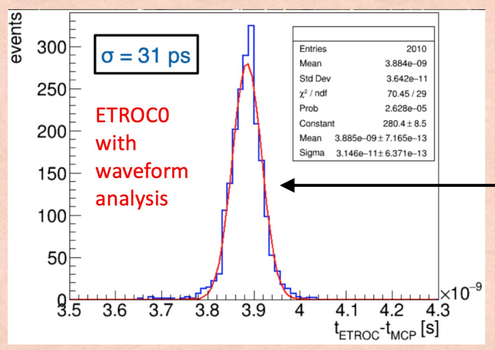
ETROC0 – Submission Dec. 2018
→ single analog channel

ETROC1 – Submission Aug. 2019
→ 4×4 pixel array with full front-end
→ TDC brand new design optimized for low power

ETROC2 – Submission Jul. 2022
→ 16x16 full size and functionality
→ H-tree clock distribution

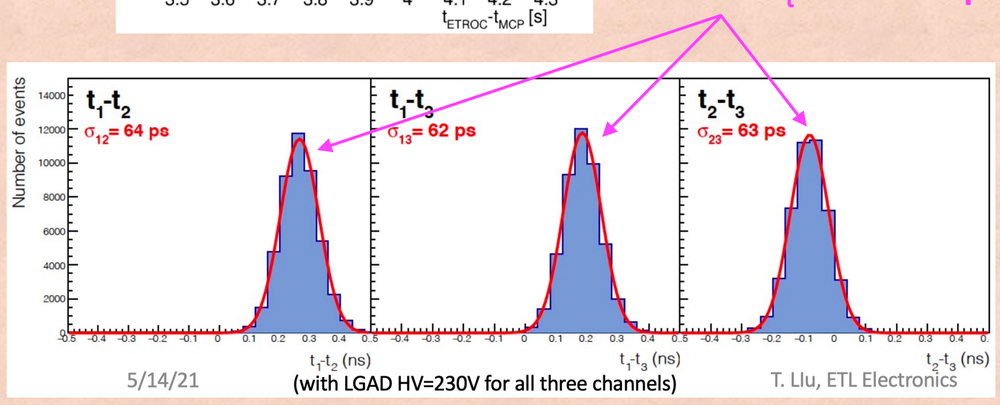
ETROC3 – Submission Mar. 2024
→ pre-production chip

From beam tests at the FNAL facility

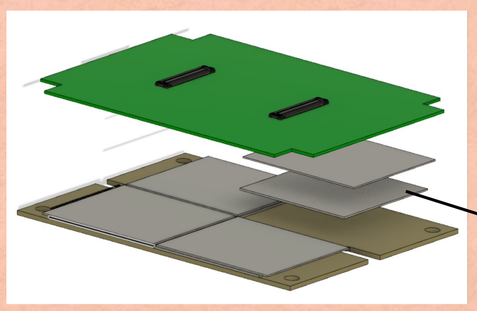


ETROC0: σ_t ~ 30 ps

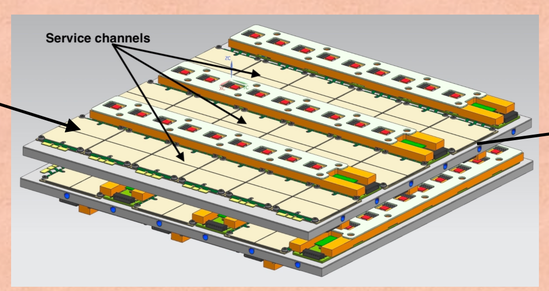
ETROC1: σ_t ~ 42 – 46 ps



Integration

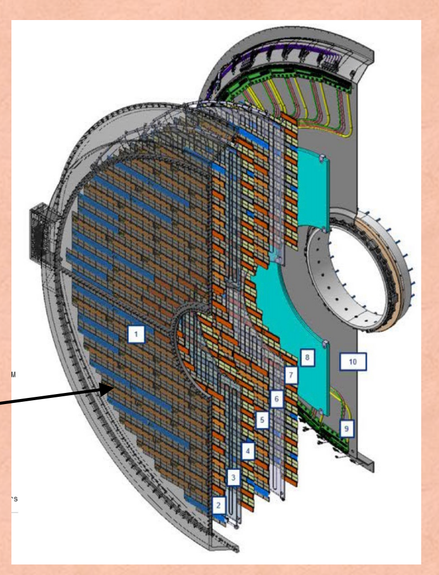


- ETL will be placed on the HGCAL nose
- Two disks for each endcap, on both sides
- Track resolution < 35 ps



Modules:

- ▻ 4 16×16 LGAD sensors bump bonded to the ETROCs
- ▻ Sensors glued on AlN baseplate in contact with the cooling disk (-20°C)
- ▻ PCB with connectors to ETL readout board



Strong effort to combine inputs from studies into a complete detector design and layout
~ 8000 modules on 2 endcaps
~ 8M channels in total

⇒ The Endcap Timing Layer is expected to provide a timing resolution per track < 40 ps up to the end-of-lifetime in most of its volume

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[1] High Luminosity LHC Project, available at https://hilumilhc.web.cern.ch/content/hl-lhc-project
[2] CMS Collaboration, A MIP Timing Detector for the CMS Phase-2 Upgrade, CERN-LHCC-2019-003, CMS-TDR-020, https://cds.cern.ch/record/2667167
[3] G. Pellegrini et al., Technology developments and first measurements of Low Gain Avalanche Detectors (LGAD) for high energy physics applications, Nucl. Inst. Meth. A 765 (2014) 12, doi:10.1016/j.nima.2014.06.008
[4] N. Cartiglia et al., Beam test results of a 16 ps timing system based on ultra-fast silicon detectors, Nucl. Inst. Meth. A 850 (2017) 83, doi:10.1016/j.nima.2017.01.021
[5] Q. Sun et al., The Analog Front-end for the LGAD BasedPrecision Timing Application in CMS ETL, doi:10.48550/arXiv.2012.14526