

Embedded D/A Converters for High Energy Physics Instrumentation

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Abstract— Three digital-to-analog converters (D/A) have been developed for High Energy Physics (HEP) applications : a voltage output 10-bits D/A for adjusting the reference of a comparator and two current output 4 and 5-bits D/As for driving laser diodes. The 10-bits D/A occupies an area of less than $0.05mm^2$ and the current output D/As occupy areas less than $0.06mm^2$ each. Voltage and current output D/As were developed in $350nm$ and $130nm$ commercially available technologies, respectively.

Requirements from the HEP point of view, architectures chosen, motivations, implementations, simulation results, and preliminary test results are presented.

I. INTRODUCTION

Modern particle detectors employ highly integrated and custom designed electronics. High integration is needed because of required detection precision in terms of time and spatial resolutions. The space allowed for the electronics due to required detector granularity is also a severe concern. Even though, almost any kind of building blocks are available commercially, they are not compiled onto chips dense enough in accordance to High Energy Physics (HEP) requirements. Thus, building an experimental HEP system composed of commercial components exceeds most of the form factor standards in the field. Custom design is needed because of the inexistence of commercially available chips which could be used for specific functionality required by experimental systems. Also the heavily radioactive environment leads to custom layout design, since commercial products are not built for radiation hardness[1]. Using special layout techniques[2][3] to make the circuits radiation tolerant is a decision made at the cost of relatively bigger and, thus, slightly slower layouts.

In HEP instrumentations, D/As are needed not for fast signal processing purposes as in speech applications but rather to fix and tune critical parameters that can not be set precise enough on-chip during the design phase. This is either because the parameters change with time[1] or the technology used is not able to provide good-enough matching and process variation characteristics.

A common example could be the binary read-out (BRO) architectures which come with the difficulty of producing identical-enough read-out channels. BRO architecture is commonly used in tracking detectors for nuclear and HEP experiments. In this architecture, each single detector component (e.g. one pad of an array of pads located on a planar surface) is expected to produce "yes" or "no" information as result of a detection. The detected analog value is compared to a

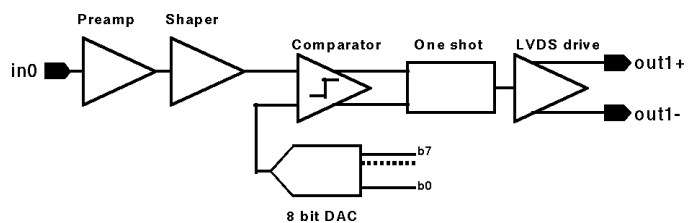


Fig. 1. Binary read-out architecture.

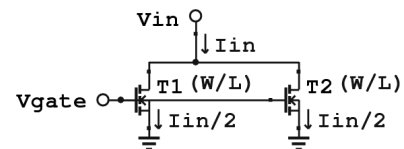


Fig. 2. Linear current division technique used in R-2R D/A.

reference value, then the binary result is sent to the next stage on the signal path. As shown in Fig. 1, the input stage is a front-end amplifier normally formed by an integrator followed by a shaper. As soon as the signal at the output of the front-end exceeds a certain value (i.e. threshold of the comparator, adjusted by a D/A) due to the charge provided by the detector, the comparator triggers a logic pulse. The pulse is, then, further processed by the next stage, e. g. a counter CN.

In applications requiring such comparisons, a global D/A can not be used, since each of the read-out channels needs its own comparator that operates independently from the rest. This brings the necessity of a low power and small area D/A architecture, since it would be used for each read-out channel and thus more than once per chip. Concerning the above requirements, CMOS-only R-2R architecture is a suitable solution as it is composed of only transistors that are compact and that consume very low power. In such an architecture, transistors in the ladder do not necessarily emulate identical resistor values but instead, the successful operation is based on linear current division principle[4] as seen in Fig. 2. The accuracy of the division technique used is based on the characteristic I-V curve matching of the two transistors but not on their linearity[5].

Another practical example is in adapting the biasing level of a circuit to different operating conditions. This could be the case for an ASIC which is used for two different systems. If a circuit operates in a mode in which speed is not a concern, then

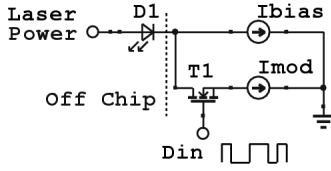


Fig. 3. Two current mode D/As driving a laser diode.

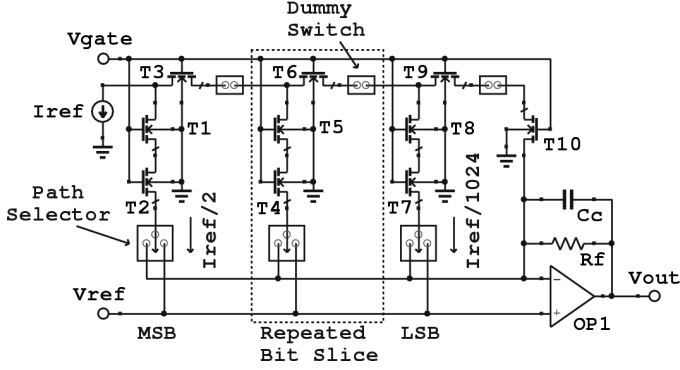


Fig. 4. Full structure of 10-bits R-2R MOST-only ladder.

reducing the biasing current is reasonable as it decreases the power consumption and the amount of energy used for cooling. Cooling is also an important parameter for granular detector systems with highly dense electronics. Such big systems tend to introduce differences due to aging and radiation, and placing the electronics far from the radioactive environment is not a remedy, since long transmission lines are required. This approach is much worse in terms of timing and signal shape integrity on which the interpretation of the detection is directly based.

Driving an off-chip laser diode which is used within an optical link is a further example of usage of biasing D/As in HEP applications. Optical links are used in DAQ systems of large scale HEP experiments[6]. They use radiation hard laser diode drivers[7] which function within a highly radioactive environment. Fig. 3 represents the concept. For such implementations, there may be two current components adjustable for optimum operation : one for biasing which keeps the laser diode just above its threshold (I_{bias}) and one for modulating which turns the diode on and off with a very high speed (I_{mod}). Especially in cases where there are different types of diodes requiring different levels for the two current components or in case the diode itself changes parameters during the operation (e. g. because of radioactive damage), two current mode D/As can serve as a dynamic power supply couple. Since almost all the current which flows through the D/As is used in the diode, current steering is the most power efficient architecture for such a functionality.

II. ARCHITECTURES

A. MOST-Only Ladder

Fig. 4 shows the complete circuit of MOST-only R-2R ladder. The circuit is biased by the reference current source

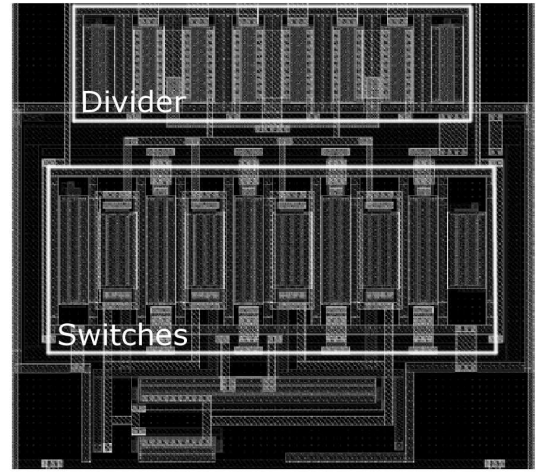


Fig. 5. Bit slice layout of 10-bits voltage output D/A.

I_{ref} which determines the full scale output current of the ladder. This current is sunk from the output stage of the opamp back through the resistor R_f to convert the steered current to the output voltage, V_{out} . Special care has been taken, since the current drive capability of the opamp plays a non-trivial role at this stage.

In Fig. 4, the value of resistor R_f in the feedback configuration plays an important role, since its value determines V_{out} , the output of the D/A, together with I_{ref} . In the actual implementation of I_{ref} , the final current level is determined by absolute value of a resistor. The ratio between this resistor and R_f is constant which keeps the product of $I_{ref} \cdot R_f$ at its nominal value. That is, in case I_{ref} increases due to a decrease in the resistor value because of process variations, resistor R_f would be affected accordingly, keeping V_{out} at its nominal value. This makes the output voltage less dependent on process variations. Dummy switches have also been used to preserve the R-2R ratio, since the path selectors introduce additional resistance decreasing the current flowing through themselves. Matching of identical T4, T5 and T6 transistors in terms of I-V curve and matching of transistors which form the path selector and dummy switch in terms of additional resistivity are important. As seen in Fig. 5, the current divider transistors are merged together at the top side of the layout and the transistors forming the path selector and the dummy switch are also merged below them.

The same functionality could also be implemented by a current mirror architecture. But that would require a much bigger silicon area whereas achieving a comparable Integral and Differential Non Linearities (INL and DNL). The current division technique used does not depend on the operating region of the transistors but on the matching of their I-V curves[4]. Therefore, the transistors are allowed to operate even in weak inversion. In terms of power consumption, R-2R structure is far ahead compared to its current mirror counterpart. The mismatch of drain currents is inversely proportional[8] to the square root of transistor area. It is calculated that for a binary

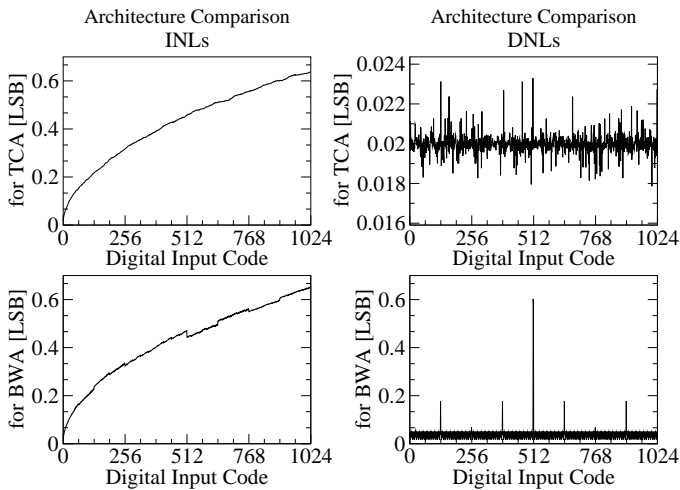


Fig. 6. RMS of 1000 Monte Carlo simulation results for $N=10$.

weighted current mirror architecture to be able to provide a comparable DNL characteristic, an area of the order of at least a few mm^2 is needed[9].

An R-2R D/A was implemented in the CMAD ASIC[10] designed for the upgrade of RICH-1[11] detector system of COMPASS[6] experiment at CERN SPS. The task of the CMAD is amplifying the signals coming from fast multi-anode photomultipliers and comparing them against a threshold adjustable on-chip on a channel by channel basis.

B. Current Mirroring

Current mirroring D/As are based on an array of well matched unit current sources that are switched to the output. Three different schemes are possible depending on the implementation, namely the binary weighted (BWA), thermometer coded (TCA) and segmented architectures.

In BWA which is also the one implemented in this work, every switch steers a current to the output which is twice as large as the next least significant bit. Also the digital input code itself directly controls the switches, that is, decoder logic is not needed. Hence, the layout can fit onto a small chip area; however, a relatively large DNL error is intrinsically associated with it. Even though, TCA has a better DC behavior, it requires more space as well as decoding logic. Segmentation could be used to benefit from the two architectures.

For an ideal comparison between BWA and TCA, a C++ code was developed in ROOT environment[12]. N being the number of bits, 2^N unit current sources were created. The currents they provide were acquired randomly from a Gaussian distribution with a sigma of 0.02 separately for each unit current source. These sources were used to form both the D/As in BWA and TCA. In BWA, first 2^{N-1} unit current sources were summed to form the Most Significant Bit (MSB), then similarly the sum of next 2^{N-2} unit sources were used as the next bit to MSB and so on. Fig. 6 shows the simulation results. Coherent with the theoretical expectations[13], INL variations for both architectures are almost identical and equal to $\sqrt{2^N}\sigma = 32\sigma$. TCA represents a 32 times (σ) better DNL

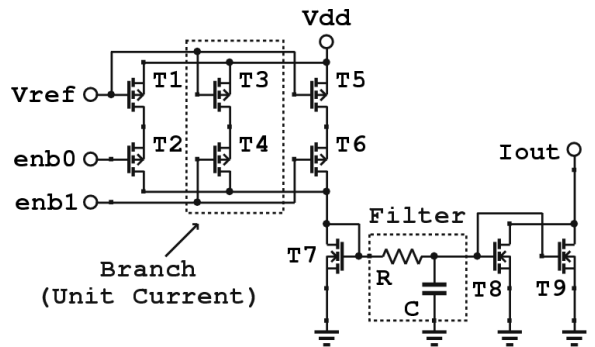


Fig. 7. Schematic of parallel current sink.

behavior than BWA does (32σ). However, considering the number of bits, which are 4 and 5, for the current output D/As presented in this work and properties of the technology used, a fully BWA is concluded to be the most convenient structure in terms of analog space-DC behavior trade-off. A similar analysis has been detailed in [13] for an implementation of 10-bits segmented D/A.

Fig.7 shows the implemented architecture employing 3 unit current branches, conceptually for two digital inputs, enb0 and enb1. The implemented layout, which consists of 16 binary current sinks operate in parallel, is shown in Fig. 8. There are two types of current sinks on the grid according to the digital input they accept : v1 and v2 that are composed of 8 and 7 identical branches of current mirrors, respectively. Sink v1 accepts one digital input (for enb3 and enb4 input bits) and switches 8 branches of unit current to the output, whereas v2 accepts three digital inputs (for enb0, enb1 and enb2 input bits) and switches 1, 2 and 4 branches of unit current to the output. Thus, the full scale current is determined by 124 branches of unit current sources.

Considering device matching and process variation issues as well as the amount of current which must be driven (i. e. 62.5mA for full scale), one Least Significant Bit (LSB) is provided by four current branches in the 5-bits D/A used for biasing laser diodes. Also the 4-bits modulating D/A has a similar architecture.

The D/A presented in this section is implemented in the linear laser driver block of giga bit transceiver being designed for Super-LHC at CERN. It is going to replace the existing transceiver for higher speed, to provide more flexibility and to preserve some of the old functionality under heavier radiation environment.

III. SIMULATION AND TEST RESULTS

The D/As presented are needed to control static parameters; so the performance of interest is limited to INL and DNL, but not to spurious-free dynamic range (SFDR) and inter modulation distortion (IM) that are typically used for high speed data converters. The simulations are summarized in Fig. 9. As shown in the Monte Carlo (MC) results for 5-bits current mode D/A on the left side, in which both process variation and device mismatch have been taken into account,

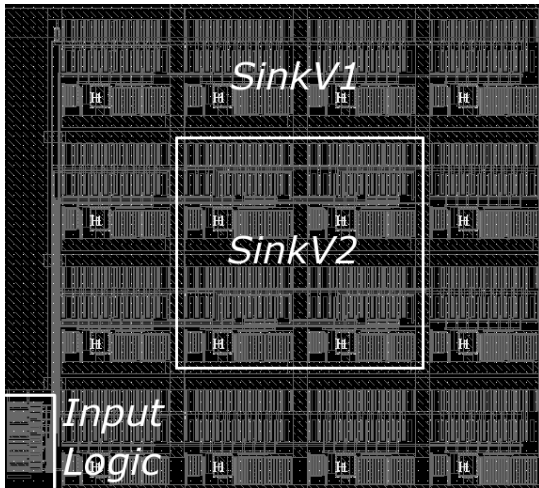


Fig. 8. Layout of 5-bit current mode D/A.

INLs and DNLs are selected from nominal condition and from the corners of the process. The spread in MC simulations basically comes from components like reference sources for which component ratio matching principle is not applicable. External pins have also been provided which could be used for disabling the on-chip reference sources in order to use external replacements instead. Even though, the INL and DNL characteristics are within a desired window, the systematic error shown in MC results could be further minimized by designing a hybrid architecture in which some of the bits were implemented as binary weighted and some of them as thermometer coded. Such an implementation is presented in [13]. The biasing could also be local for each current sink or even a smaller unit segment could be used. However, considering the space requirement, none of the techniques mentioned above has been implemented, since the simulation results showed that the DC behavior is already as desired.

INL and DNL data, calculated with typical mean (tm) simulation parameters, for 10-bit D/A are as shown in the right side of Fig. 9. It must be stated that the simulation results provided for 10-bit D/A must be interpreted with care. They have been obtained by using the BSIM3v3 model parameters, and as reported in [5], the current division technique used could not be modeled by the simulators as precise as it is actually. The mismatch between the simulator model and the actual response of the fabricated circuit results in a bigger error in design phase. Thus, a better set of INL and DNL characteristics is expected from the tests of actually fabricated circuits.

Fig. 10 shows the threshold scan measurement results of a single channel in the CMAD ASIC. First plot shows the expected plateau where 50% of the input signals is successfully cut (region marked with an A) whereas the input signals larger than the threshold passed through the comparator (region marked with a B). The middle figure shows the same distribution with a threshold very close to baseline (the peak is due to noise) and no input signal. Lastly the right figure

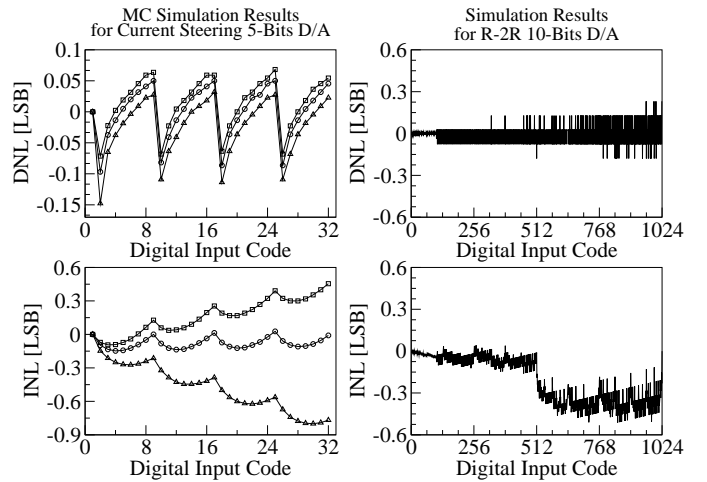


Fig. 9. Simulation results for 5-bit (left) and 10-bit (right) D/As.

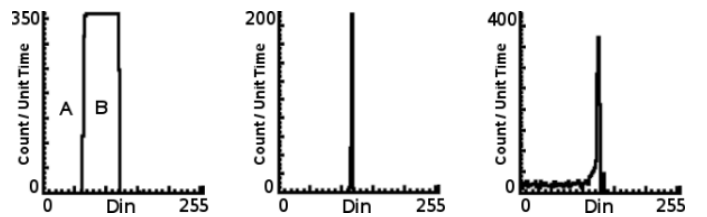


Fig. 10. Threshold scan measurement results.

shows the results from the same measurement performed with PMTs and LEDs imitating Cherenkov radiation. In the final plot, there is not cut-signal-region, since the input signal was larger than the largest threshold value settable, thus all the signals passed through the comparator. Even though, they are currently preliminary, all the measurement results so far are coherent with simulations as expected.

IV. CONCLUSION

A voltage output 10-bit D/A to set the threshold of a comparator and two current output D/As, 4 and 5-bit, to drive a laser diode were discussed for intended use in HEP applications. The implementations occupy areas of less than $0.05mm^2$ for 10-bit D/A and less than $0.06mm^2$ for 4 and 5-bit D/As each, developed in $350nm$ and $130nm$ commercial technologies, respectively. The power consumptions are $90mW$ for 4 and 5-bit D/As each and $165\mu W$ for the core of 10-bit R-2R D/A.

The ASICs, on which the D/As presented in this work reside, have been fabricated and are being tested extensively. Concerning the 10-bit D/A, preliminary test results were also presented.

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REFERENCES

- [1] Snoeys W., Anelli G., et al., Integrated circuits for particle physics experiments, *IEEE Journal of Solid-State Circuits*, Vol. 35, No. 12, 2000
- [2] Snoeys W.J., Gutierrez T.A.P., Anelli G., A new NMOS layout structure for radiation tolerance, *IEEE Transactions on Nuclear Science*, Vol. 49, No. 4, Part 1, 2002
- [3] G. Anelli, et al., Radiation tolerant VLSI circuits in standard deep submicron CMOS technologies for the LHC experiments: practical design aspects, *IEEE Transactions on Nuclear Science*, Vol. 46, No. 6, 1999
- [4] K. Bult, et al., An Inherently Linear and Compact MOST-Only Current Division Technique, *IEEE Journal of Solid State Circuits*, Vol. 27, No. 12, 1992
- [5] C.M. Hammerschmied, et al., Design and Implementation of an Untrimmed MOSFET-Only 10-Bits A/D Converter with -79-dB THD, *IEEE Journal of Solid State Circuits*, Vol. 33, No. 8, 1998
- [6] COMPASS Proposal, CERN/SPSLC 96-14, SPSC/P 297, March 1, 1996
- [7] P. Moreira, et al., G-Link and Gigabit Ethernet Compliant Serializer for LHC Data Transmission, *IEEE Nuclear Science Symposium Conference Record*, October 15-20, 2000, Lyon, France, pp. 9.6-9.9
- [8] M.J.M. Pelgrom, et al., Matching properties of MOS transistors, *IEEE Journal of Solid-State Circuits*, Vol. 24, No. 5, 1989
- [9] Austria Micro Systems, *0.35 μ m Process Manual*, ENG-228
- [10] Ö. Çobanoğlu, et al., "CMAD", a Full Custom ASIC for the Upgrade of COMPASS RICH-1, *LECC2006, 12th Workshop on Electronics for LHC and Future Experiments*, 25-29 September 2006, Valencia Spain
- [11] COMPASS Status Report 2006, CERN/SPSC 2006-013, SPSC-SR-007 April 18, 2006
- [12] R. Brun and F. Rademakers, ROOT An object oriented data analysis framework, *Nuclear Instruments and Methods in Physics Research Section A*, Volume 389, Issues 1-2, 11 April 1997
- [13] Chi-Hung Lin and K. Bult, A 10-b 500-MSample/s CMOS DAC in $0.6\mu\text{m}^2$, *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 12, 1998