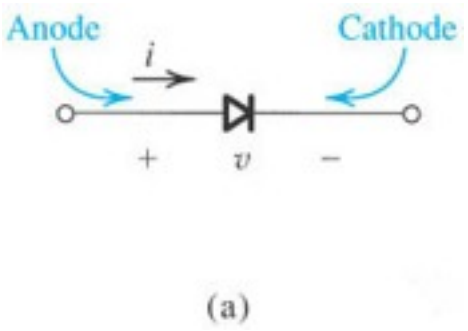
Laboratorio Avanzato di Elettronica

A.A. 2011/12

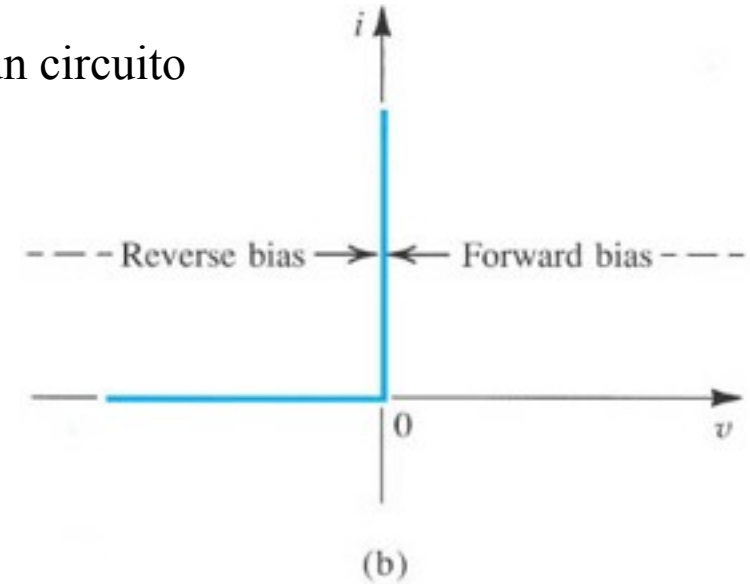
Diode

Il diodo ideale : caratteristica I-V

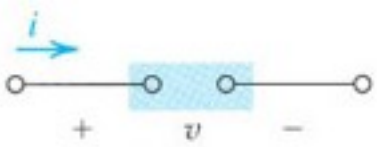
Elemento non lineare fondamentale di un circuito



(a)

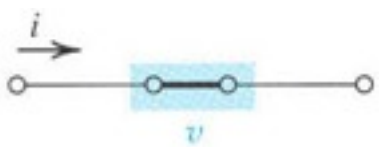


(b)



$v < 0 \Rightarrow i = 0$

(c)



$i > 0 \Rightarrow v = 0$

(d)

Figure 3.1 The ideal diode: **(a)** diode circuit symbol; **(b)** *i*–v characteristic; **(c)** equivalent circuit in the reverse direction; **(d)** equivalent circuit in the forward direction.

Il circuito esterno deve essere tale da limitare la corrente nel F-B, e determinare la tensione nel R-B

diodo in conduzione,(cortocircuito)
la corrente determinata
dalla tensione +10 V
e dalla resistenza di 1kΩ

diodo interdetto,(aperto)
non passa corrente,
la tensione ai capi del diodo
e' la tensione applicata.

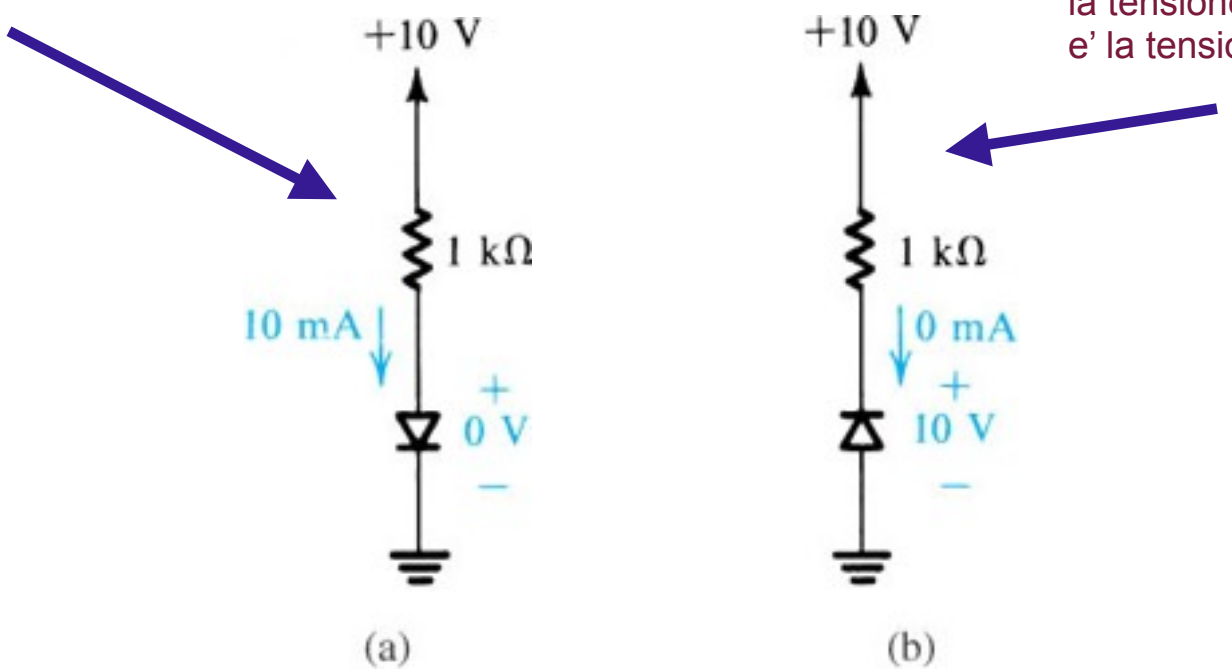
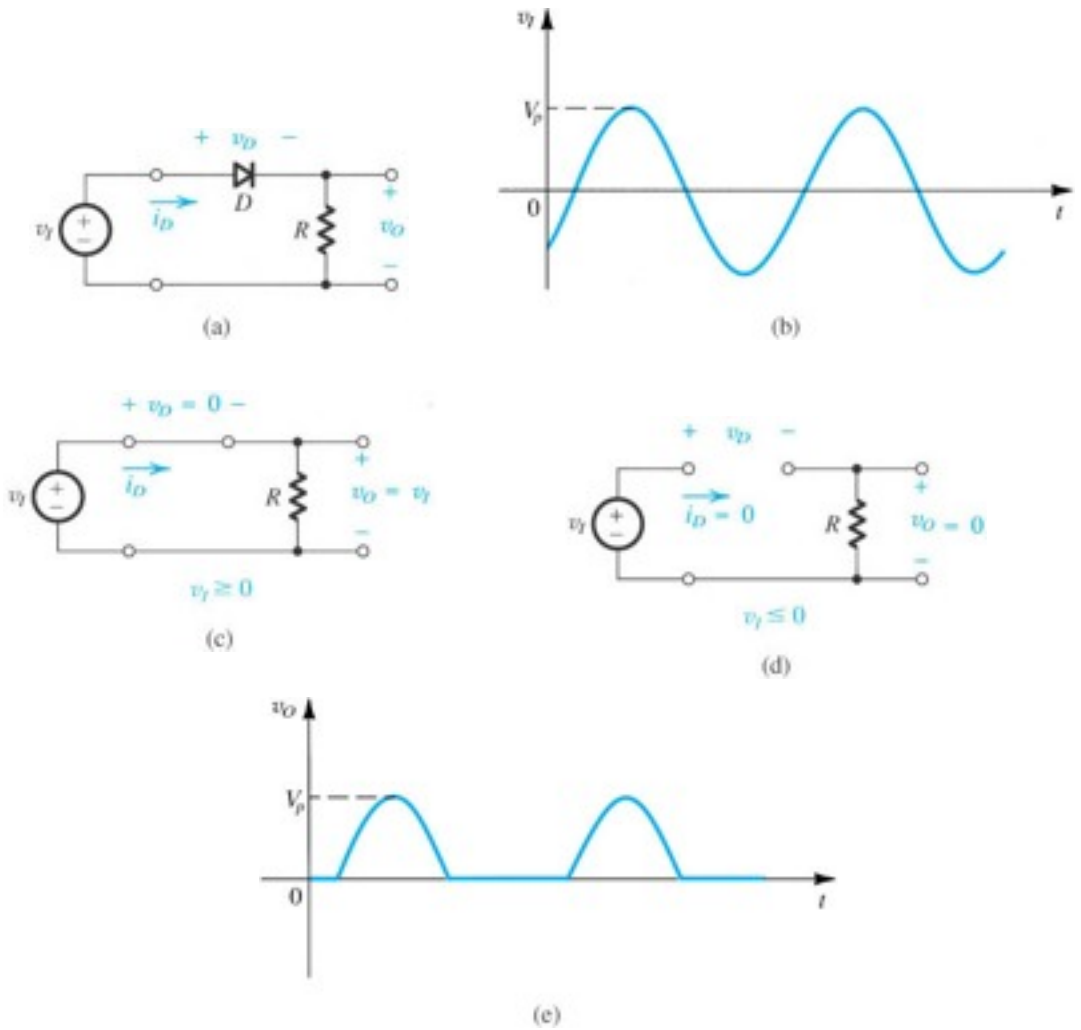


Figure 3.2 The two modes of operation of ideal diodes and the use of an external circuit to limit the forward current **(a)** and the reverse voltage **(b)**.

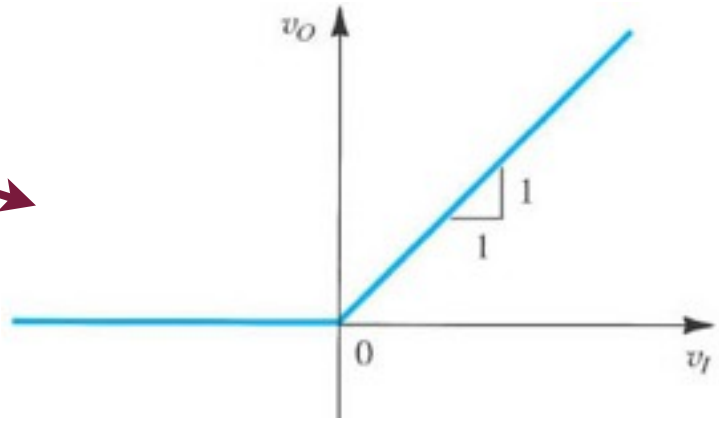
Un semplice circuito: il rettificatore



Notare come v_i in input ha valore medio nullo, mentre v_o ha valore medio diverso da zero.

Figure 3.3 **(a)** Rectifier circuit. **(b)** Input waveform. **(c)** Equivalent circuit when $v_I \geq 0$. **(d)** Equivalent circuit when v_I ² 0. **(e)** Output waveform.

Caratteristica Vi vs Vo
del circuito rettificatore



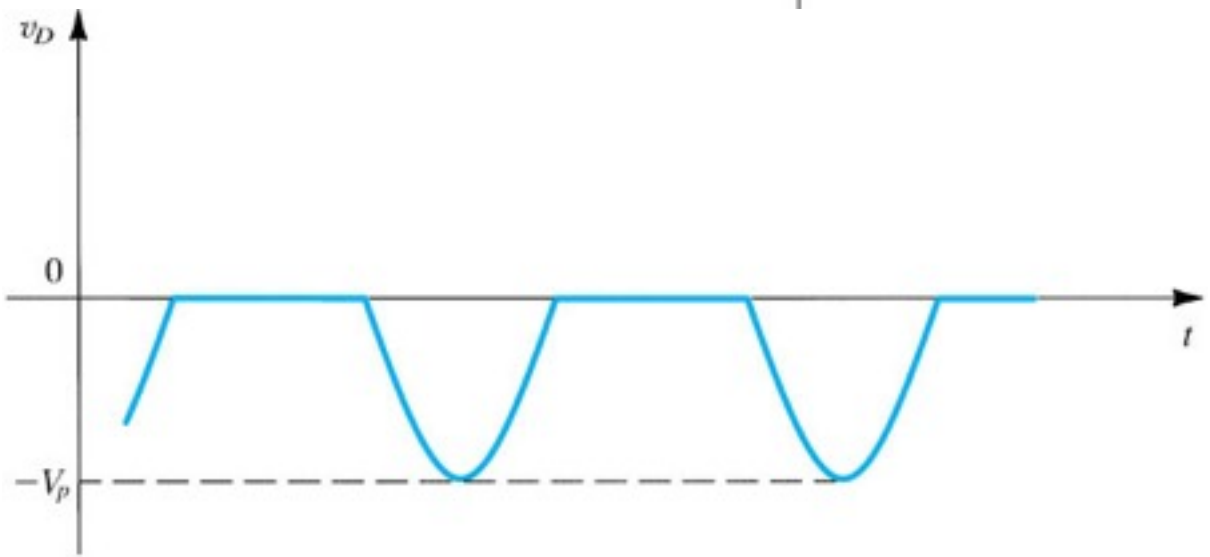
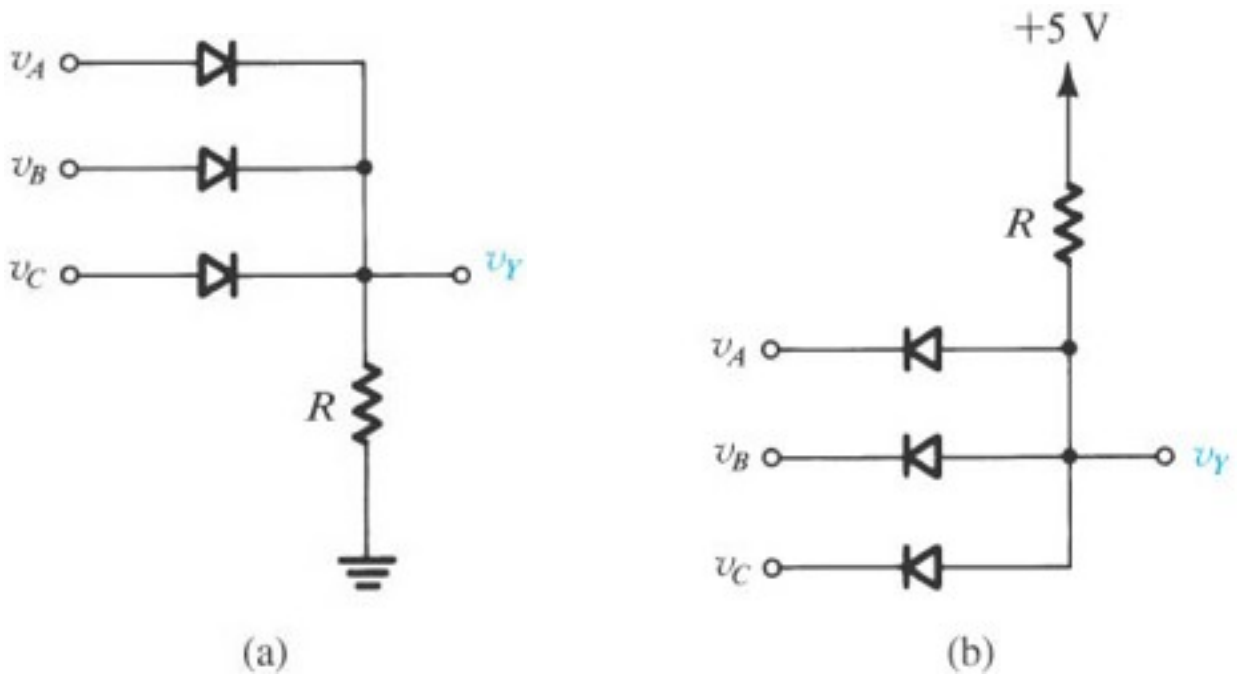


Grafico di V_D del diodo del circuito rettificatore

Applicazione: gate logici con diodi



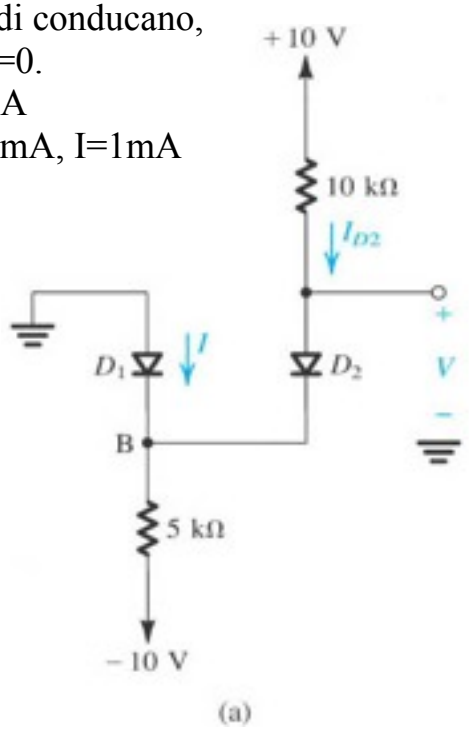
OR function Y=A+B+C

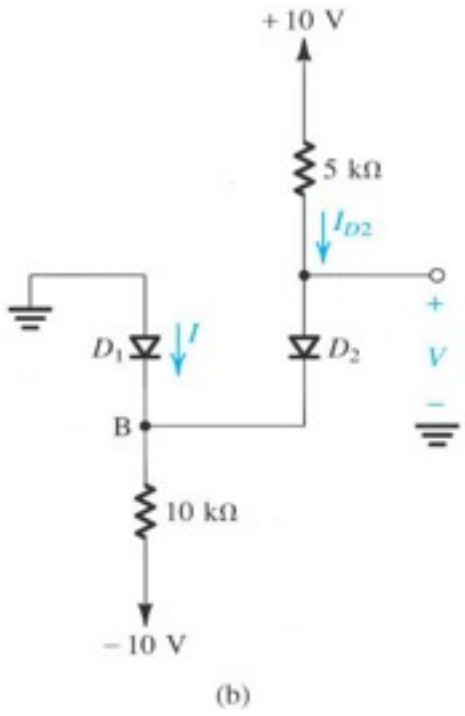
AND function Y=A·B·C

Figure 3.5 Diode logic gates: **(a)** OR gate; **(b)** AND gate (in a positive-logic system).

Analisi di un circuito con diodi
va fatto partendo da ipotesi sulla conduzione o meno dei diodi

Caso (a):
Ipotesi che i 2 diodi conducano, quindi $V_B = 0$ e V=0.
I_{D2}=(10-0)/10=1mA
I+1=(0-(-10))/5=2mA, I=1mA
Ipotesi OK





Caso (a):
Ipotesi che i 2 diodi conducano, quindi $V_B = 0$ e V=0.
I_{D2}=(10-0)/5=2mA
I+2=(0-(-10))/10=1mA, I=-1mA
Ipotesi NOT_OK.
Altra ipotesi:
D_1=OFF, D_2=ON
I_{D2}=(10-(-10))/15=1.33 mA
V_B=-10+10x1.33=+3.3V
Risultato OK:
I=0, V=3.33V

Figure 3.6 Esercizio: calcolare Id2 e I per entrambi i circuiti

Altri esercizi

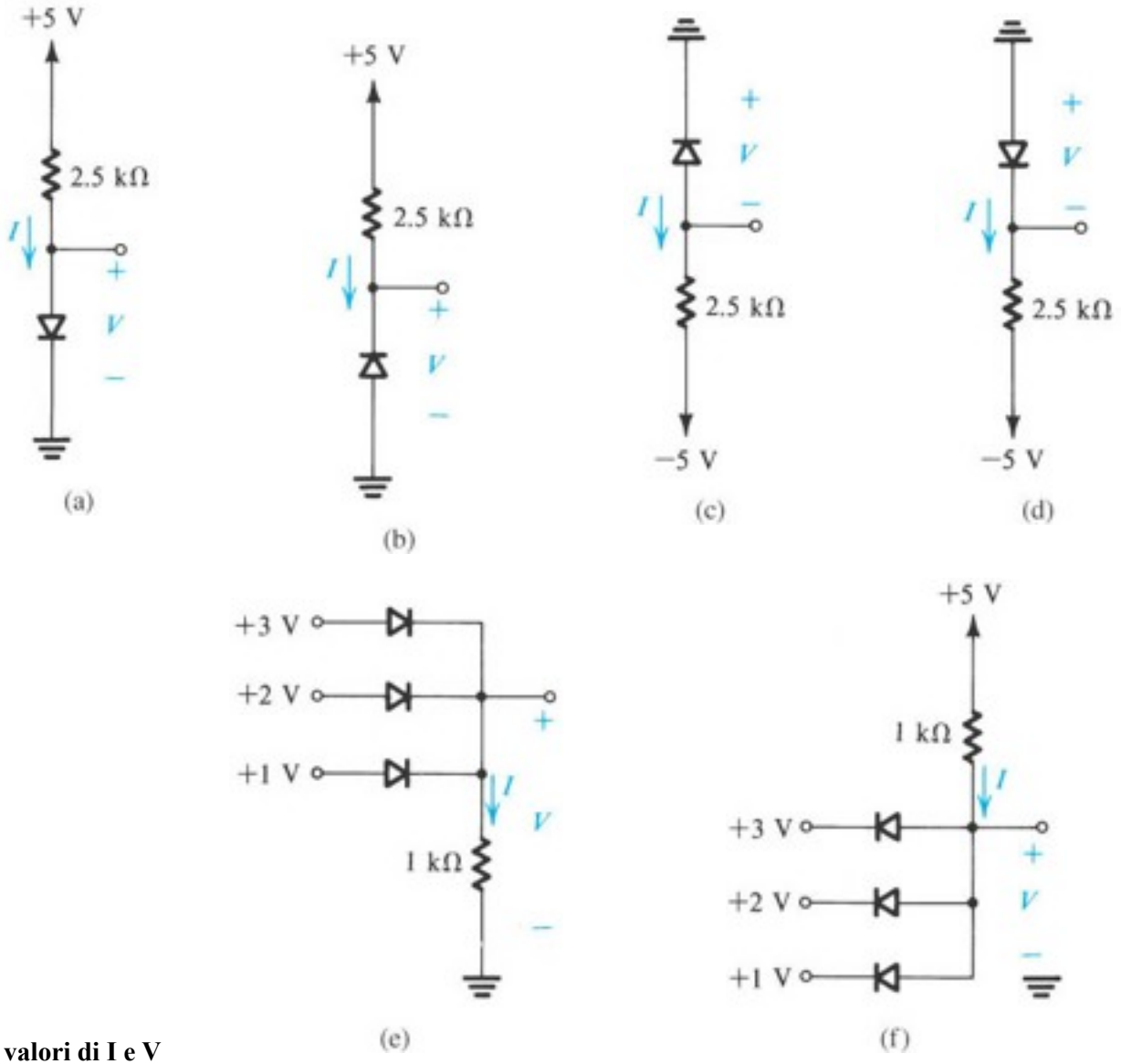
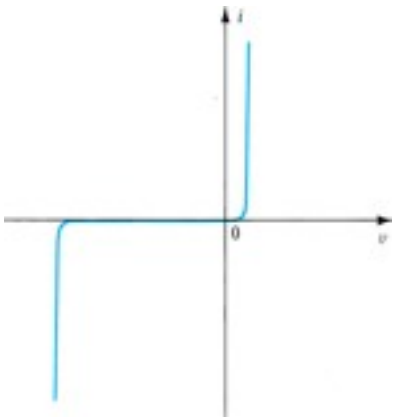
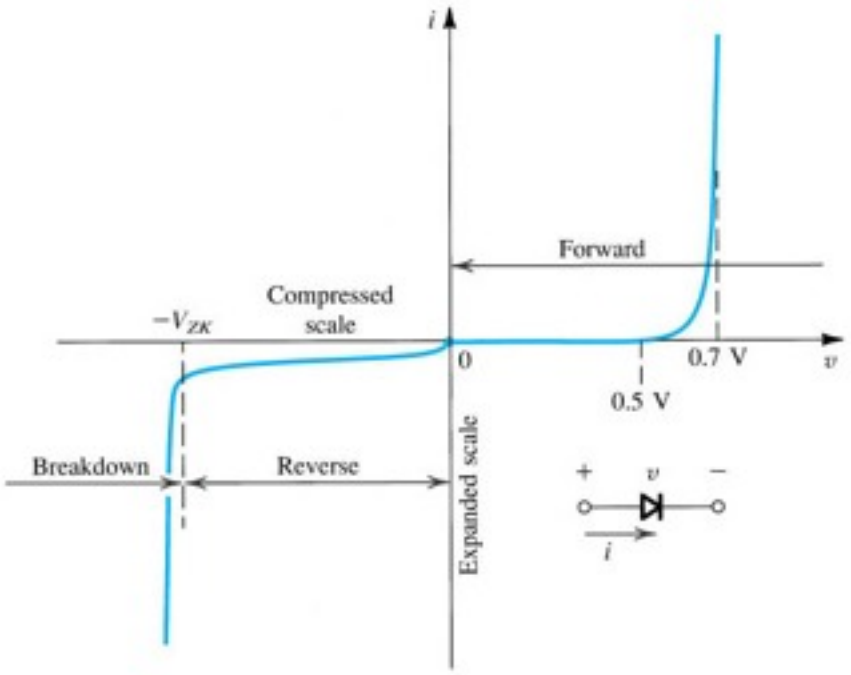


Figure E3.4 Trovare i valori di I e V

Caratteristica di un diodo a giunzione di semiconduttore



Espandiamo



Tre regioni:

1. regione forward, determinata da v > 0
2. regione backward, determinata da v< 0
3. regione di breakdown, determinata da $v<V_{zk}$

Figure 3.7 The *i*–v characteristic of a silicon junction diode.

Regione Bias-Forward

La regione forward e' attivata quando la tensione **v** ai terminali del diodo e' positiva

$$i = I_S(e^{v/nV_T} - 1)$$

n per diodi integrati vale 1,
per quelli discreti vale 2

La I_s e' la *corrente di saturazione o corrente di scala*. Ha un valore, per piccoli segnali, di 10^{-15} A
Dipende dalla temperatura, si raddoppia per ogni 5 ^oC di aumento della temperatura.

V_T e' invece la *Tensione Termica,* e vale a 20 ^oC 25.2 mV
approssimata per i calcoli a 25.0 mV.

$$V_T = \frac{kT}{q}$$

k costante di Boltzman,
T temperatura in Kelvin,
q carica elettrica

Con valori di corrente i >>I_s la relazione si approssima a

$$i \approx I_S e^{v/nV_T} \longrightarrow v = nV_T \ln(\frac{i}{I_S})$$

La relazione esponenziale **i-v** copre abbondantemente fino a 7 ordini di grandezza

Se la tensione al diodo e' V_1 la corrente i_1 sara' data da $i_1 = I_S e^{V_1/nV_T}$

e per V_2 $i_2 = I_S e^{V_2/nV_T}$

$$V_2 - V_1 = nV_T \ln(\frac{I_2}{I_1}) \quad \text{o in base10} \quad V_2 - V_1 = 2.3nV_T \lg(\frac{I_2}{I_1})$$

Queste relazioni semplicemente dicono che per una cambiamento di un fattore 10 in corrente, decade, la tensione del diodo cambia di un fattore $2.3nV_T$, che equivale a 60 mV con n=1 e 120 mV con n=2.

Se si plotta la caratteristica i-v, la relazione precedente mostra che se si usa una scala semilogaritmica, la v su asse verticale lineare e la corrente i su asse logaritmico la caratteristica e' una retta con una slope di $2.3nV_T$ per decade di corrente, **che si approssima quasi sempre a 0.1 V/decade di corrente**

dalla caratteristica i-v , si vede che per v<0.5V la corrente e' molto piccola, questo valore e' usualmente indicato come **cut-in voltage.**
Il diodo lo si puo' considerare in conduzione piena tra 0.6V e 0.8V, semplificando si puo' fissare la tensione di conduzione a 0.7 V; la corrente a questo valore limite dipendera' dal tipo di diodo.

Per piccoli segnali, un diodo avra' una corrente di 1 mA a 0.7V, mentre per un diodo di potenza la corrente sara' di 1A a 0.7V

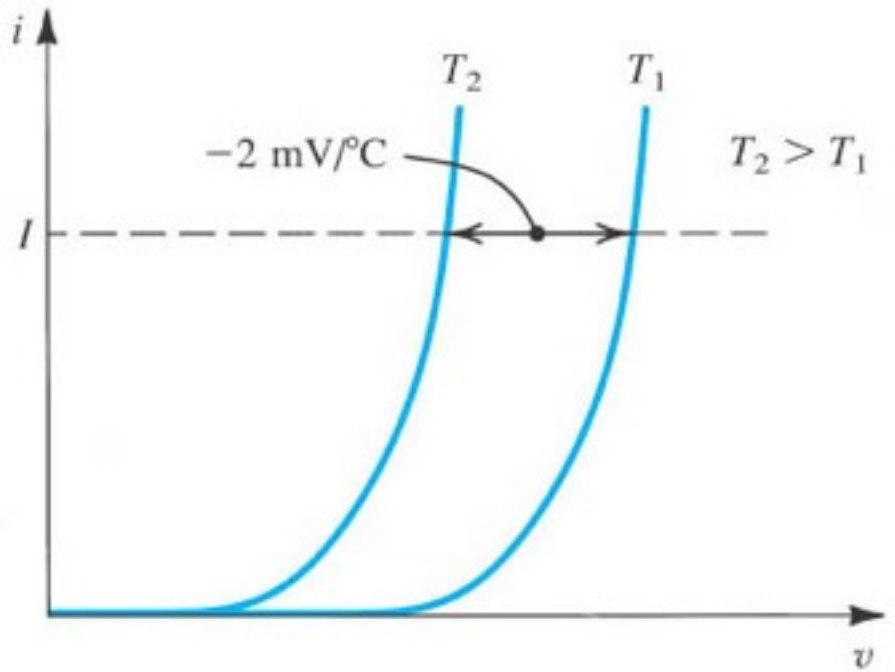


Figure 3.9 Illustrating the temperature dependence of the diode forward characteristic. At a constant current, the voltage drop decreases by approximately 2 mV for every 1°C increase in temperature.

La regione reverse-bias

Il diodo entra in reverse mode quando ha una tensione negativa.
Dall'equazione

$$i = I_S(e^{v/nV_T} - 1)$$

si vede che per v<0 e maggiore
in grandezza di nVT (~25mV)
il termine esponenziale diventa trascurabile
per cui si puo' usare la relazione

$$i \approx -I_S$$

che indica che la corrente inversa e' praticamente costante
Corrente di Saturazione o reverse current.

I diodi reali hanno correnti di saturazione
di circa 10 nA, contro i 10 fA previsti,
questo e' dovuto al fenomeno del leakage,
che dipende dall'area della giunzione.
La corrente inversa cresce anche con la temperatura ed
una regola pratica dice che la corrente inversa si
raddoppia
ad ogni aumento di temperatura di 10 oC.

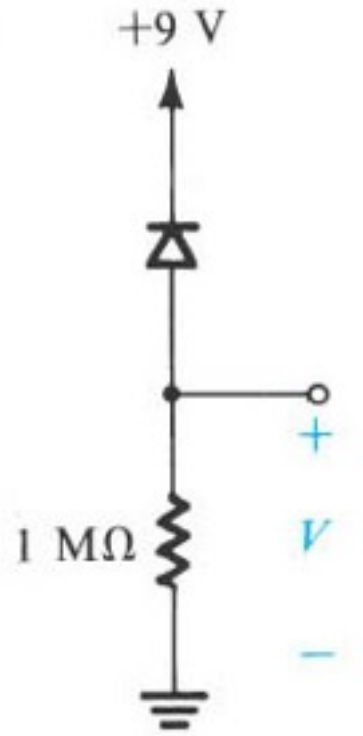
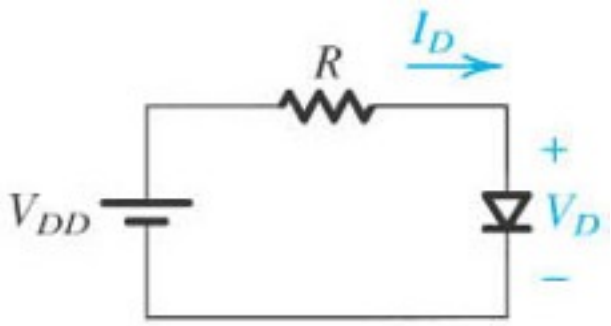
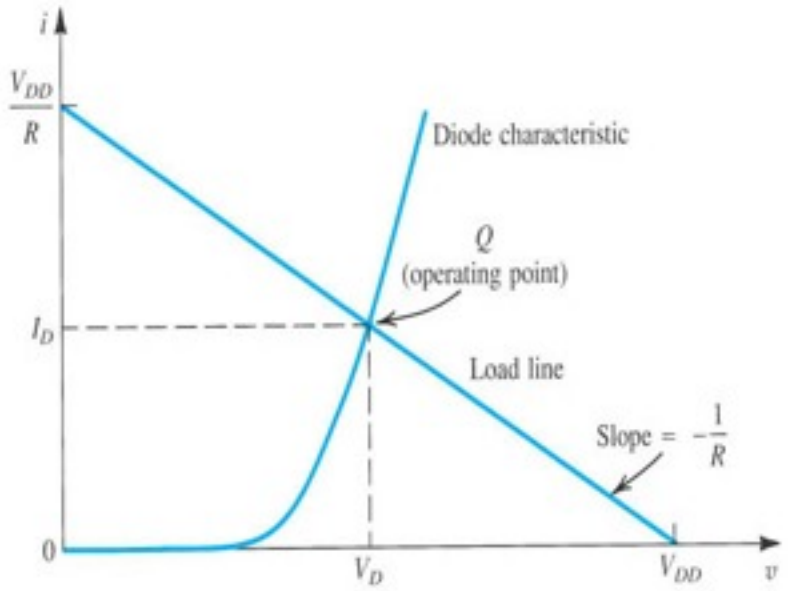


Figure E3.9

Modelli di caratteristica i-v forward

Il modello esponenziale e' il piu' accurato, ma il piu' difficile data la sua non linearita'.





Dal circuito e con $V_{DD} > 0.5$ V, la $I_D >> I_S$, per cui

$$I_D = I_S e^{V_D/nV_T}$$

Con Kirchhoff ottengo la seconda espressione

$$I_D = \frac{V_{DD} - V_D}{R}$$

Ho due incognite, I_D e V_D e due espressioni, per cui posso risolvere il sistema.
Un metodo pratico e' usare l'analisi grafica.

Figure 3.10 A simple circuit used to illustrate the analysis of circuits in which the diode is forward conducting.

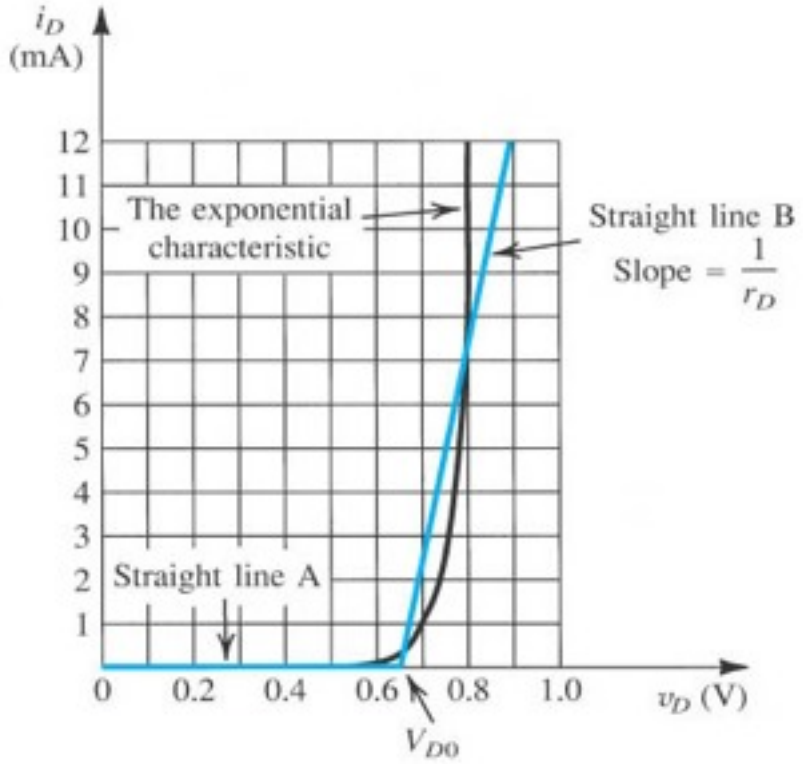
Modello lineare a pezzi

La curva esponenziale
si modella con due rette,
retta A con slop nullo
e retta B con slop1/r_D

Come si vede dal grafico, per
una corrente da 0.1 mA a 10 mA
la differenza di tensione e' < 50mV.

Natualmente la scelta della retta
dipende dalla regione di lavoro.

Il modello lineare puo' essere descritto da



$$i_D = 0, \qquad v_D \le V_{DD}$$

$$i_D = \frac{v_D - V_{D0}}{R}, \qquad v_D \ge V_{D0}$$

nel grafico $r_D = 20\ \Omega$

Figure 3.12 Approximating the diode forward characteristic with two straight lines: the piecewise-linear model.

Il circuito equivalente del modello lineare include un diodo lineare per costringere la i_D solo nella direzione forward.

Questo modello e' detto modello **batteria + resistenza**

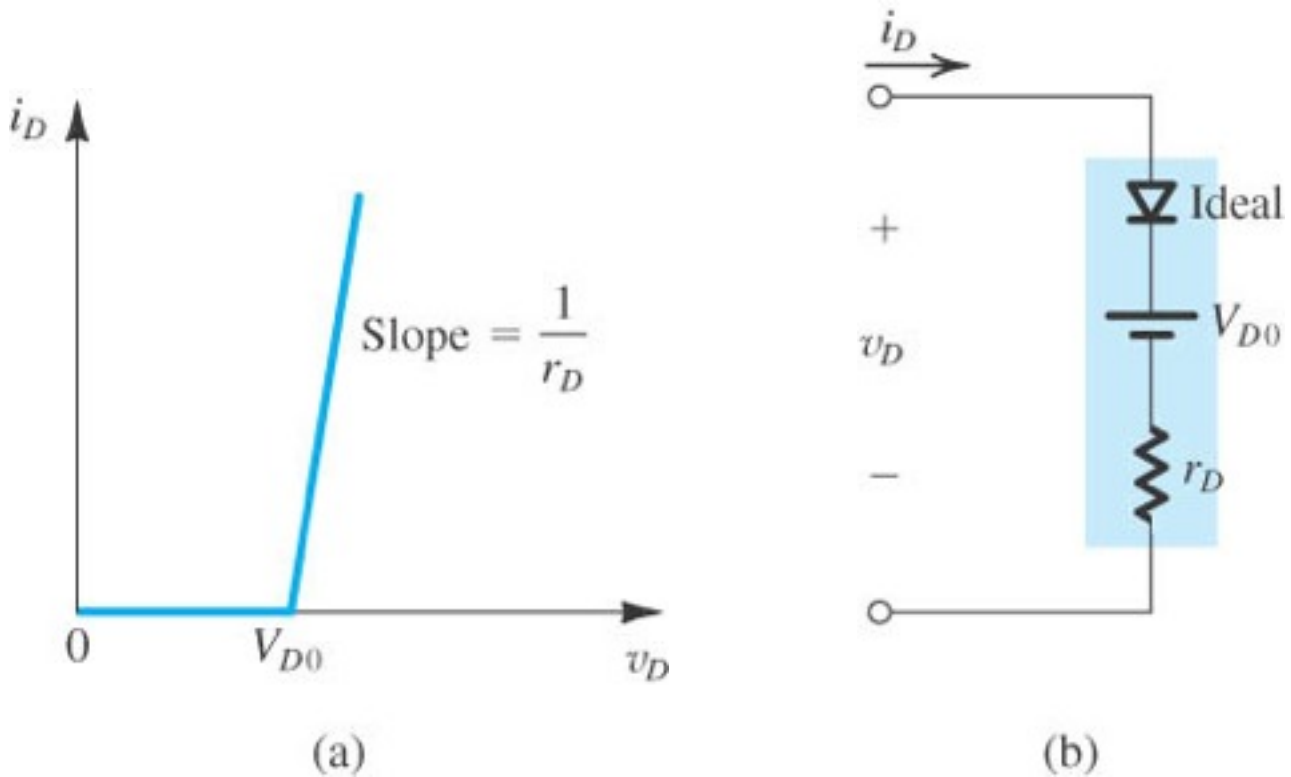
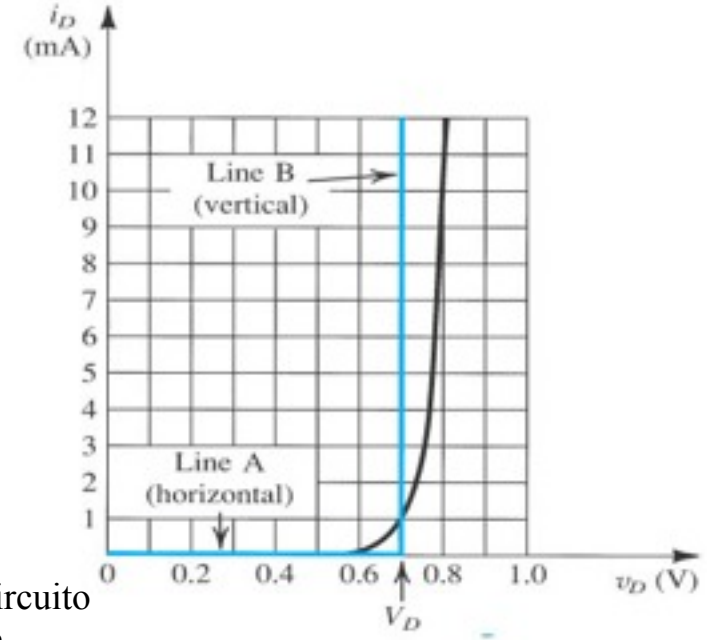


Figure 3.13 Piecewise-linear model of the diode forward characteristic and its equivalent circuit representation.

Modello a caduta costante di tensione

Questo semplice modello assume che nella parte forward, ad un valore fissato di V_D, la tensione rimanga costante al variare della corrente, nei limti da 0.1 mA a 10 mA. Si fa un errore di +-0.1 V.



Per risolvere l'equazioni si usano le relazioni

$$V_D = 0.7V$$

$$I_D = \frac{V_{DD} - 0.7}{R}$$

con V_{DD} la tensione di alimentazione del circuito e R la resistenza di controllo della corrente

Circuito equivalente

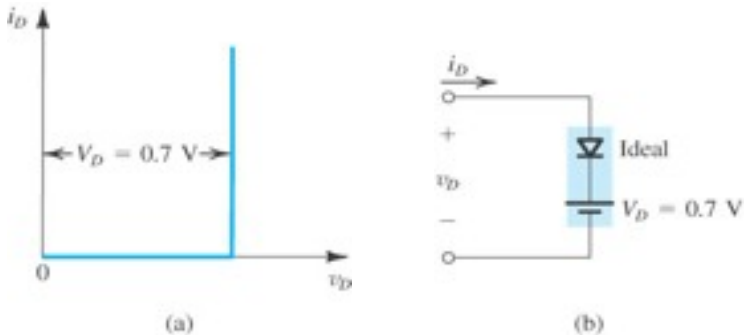
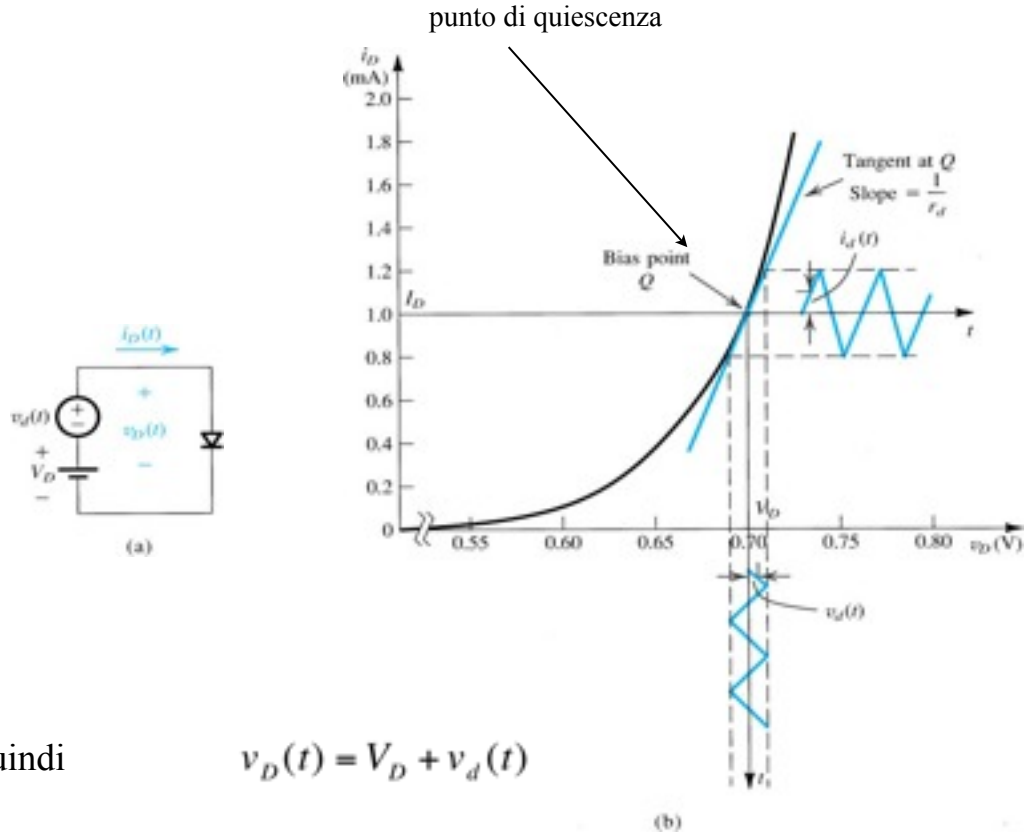


Figure 3.15 Development of the constant-voltage-drop model of the diode forward characteristics. A vertical straight line (B) is used to approximate the fast-rising exponential. Observe that this simple model predicts V_D to within ±0.1 V over the current range of 0.1 mA to 10 mA.

Modello Piccoli Segnali

Il diodo puo' lavorare ad un punto di bias tale che per piccoli segnali in quel punto la caratteristica e' considerata lineare.
Con il DC bias a 0.7 V, il modello del diodo e' quello con resistenza pari all'inverso della slope della tangente alla curva I-V nel punto di bias.



Al diodo e' applicata una tensione DC V_D ed a questa e' sovrapposto un segnale $v_d(t)$ arbitrario.

In asseza del segnale $v_d(t)$ la tensione ai capi del diodo sarebbe V_D e la corrente sarebbe

$$I_D = I_S e^{V_D/nV_T}$$

Col segnale applicato la tensione istantanea sara' quindi

$$v_D(t) = V_D + v_d(t)$$

e la corrente di conseguenza

$$i_D(t) = I_S e^{v_D/nV_T}$$

Figure 3.17 Development of the diode small-signal model. Note that the numerical values shown are for a diode with $n = 2$.

Sostituendo si ottiene $$I_D(t) = I_D e^{v_d/nV_T}$$

Se il segnale e' sufficientemente piccolo cosicche' $$\frac{v_d}{nV_T} << 1$$

Si puo' espandere in serie e troncare al primo termine, si ricava cosi' l'espressione per la corrente per il modello a piccoli segnali- **approssimazione piccoli segnali**

$$i_D(t) \cong I_D(1 + \frac{v_d}{nV_T})$$ Valida per segnali v(t)<=5mA

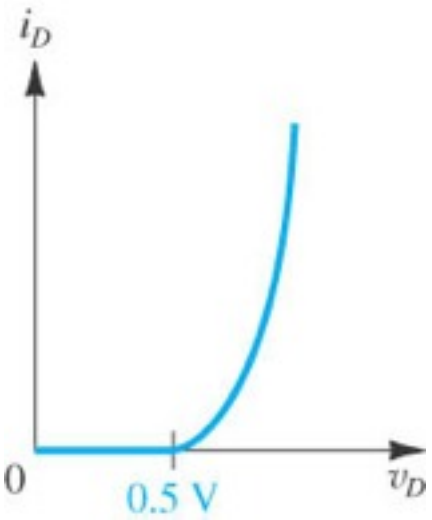
$$i_D(t) = I_D + \frac{I_D}{nV_T} v_d$$

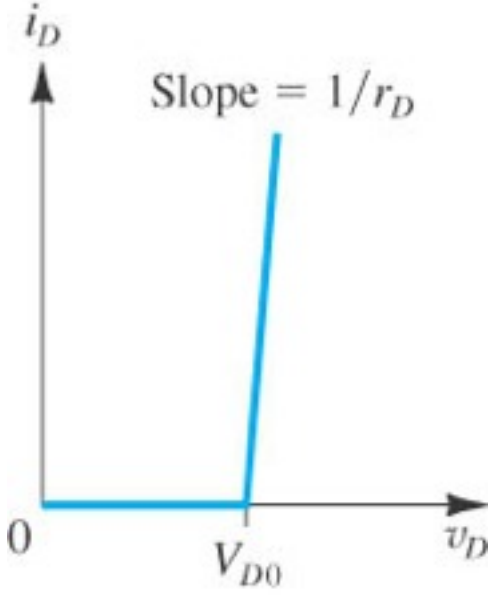
$$i_D(t) = I_D + i_d \quad , \quad \text{con} \quad i_D = \frac{I_D}{nV_T} v_d$$

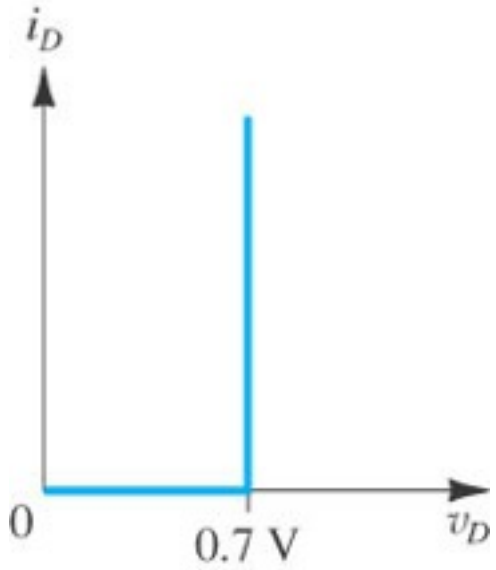
sovrapposta alla corrente DC c'e' una corrente di segnale direttamente proporzionale alla tensione di segnale v(t)

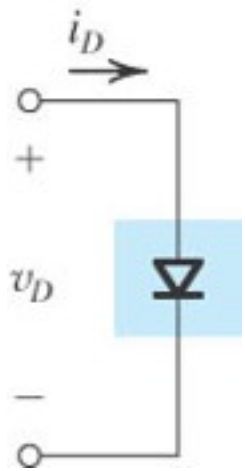
Il termine di proporzionalita' ha dimensioni di una **conduttanza**, Ohm $^{-1}$, e' chiamata **conduttanza di piccoli segnali** del diodo; la **resistenza r_d** di piccoli segnali del diodo e' l'inverso della conduttanza ed e' proporzionale inversamente alla corrente di bias I_D.

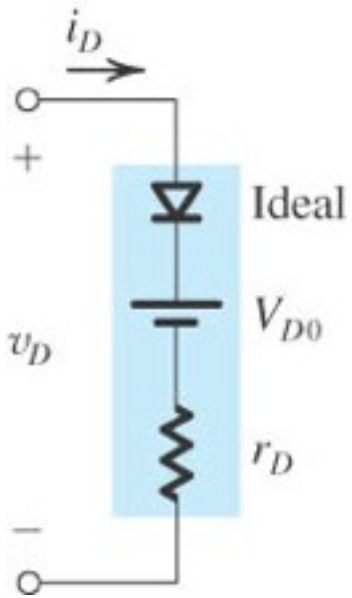
$$r_d = \frac{nV_T}{I_D}$$











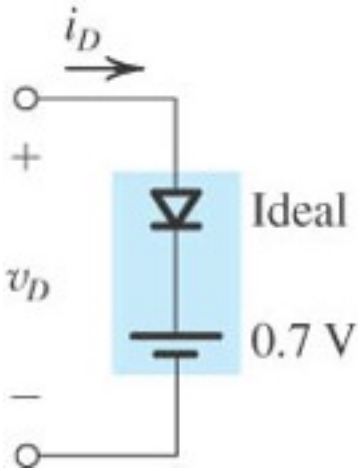
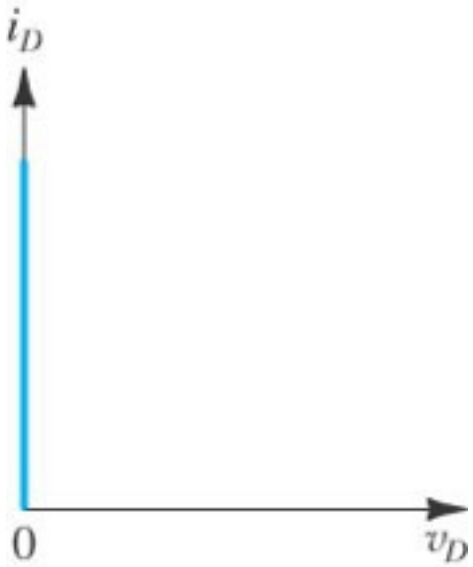
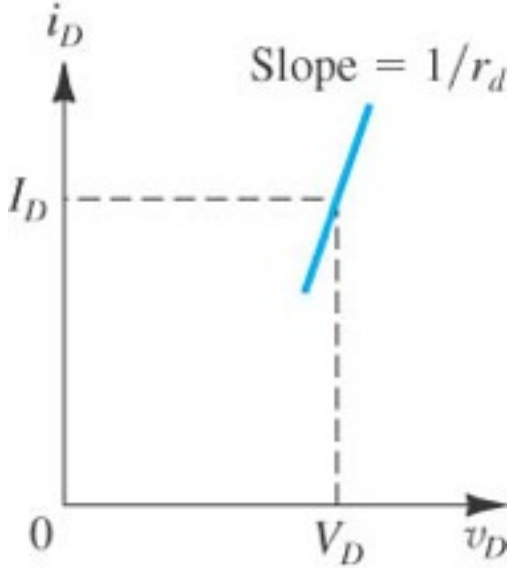
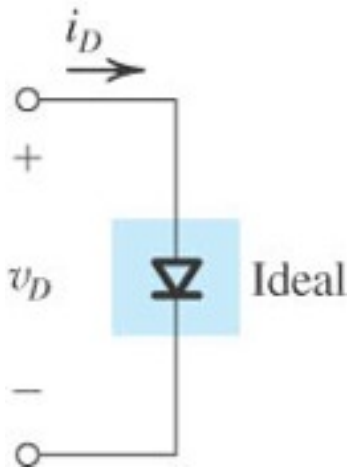


Table 3.1 Modeling the Diode Forward Characteristic







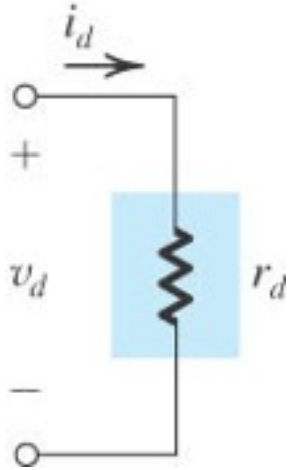


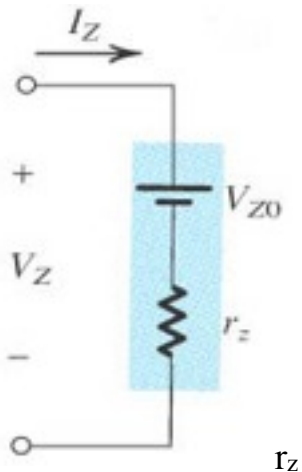
Table 3.1 ***(Continued)***

Diodi Zener

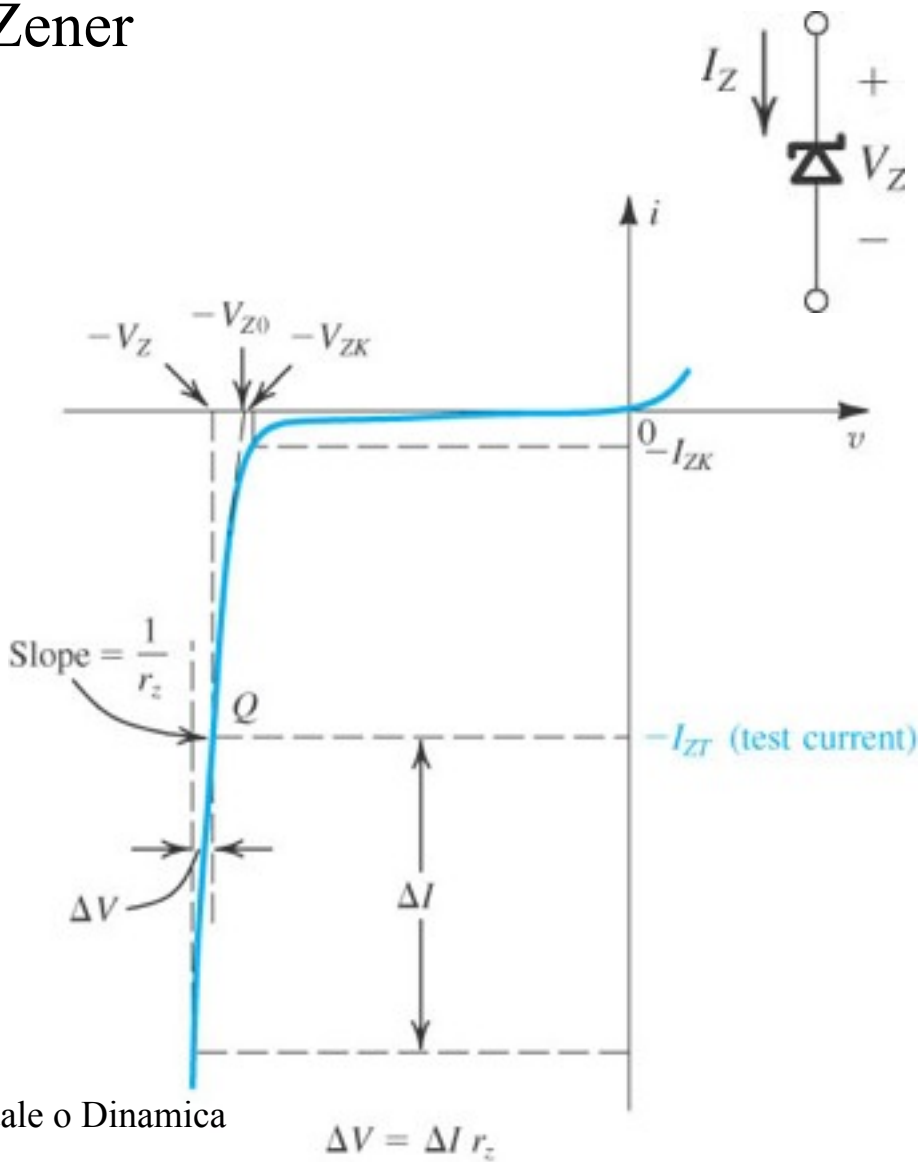
Operano nella regione reverse-breakdown

Un diodo zener e' caratterizzato dal valore di V per una determianta corrente I_{ZT}

Un diodo Zener puo' essere modellato secondo il seguente circuito equivalente che e' descritto dalla relazione i-v, come:



$$V_z = V_{z0} + r_z I_z$$



r_z = Resistenza Incrementale o Dinamica

The diode *i*–v characteristic with the breakdown region shown in some detail, e il suo modello

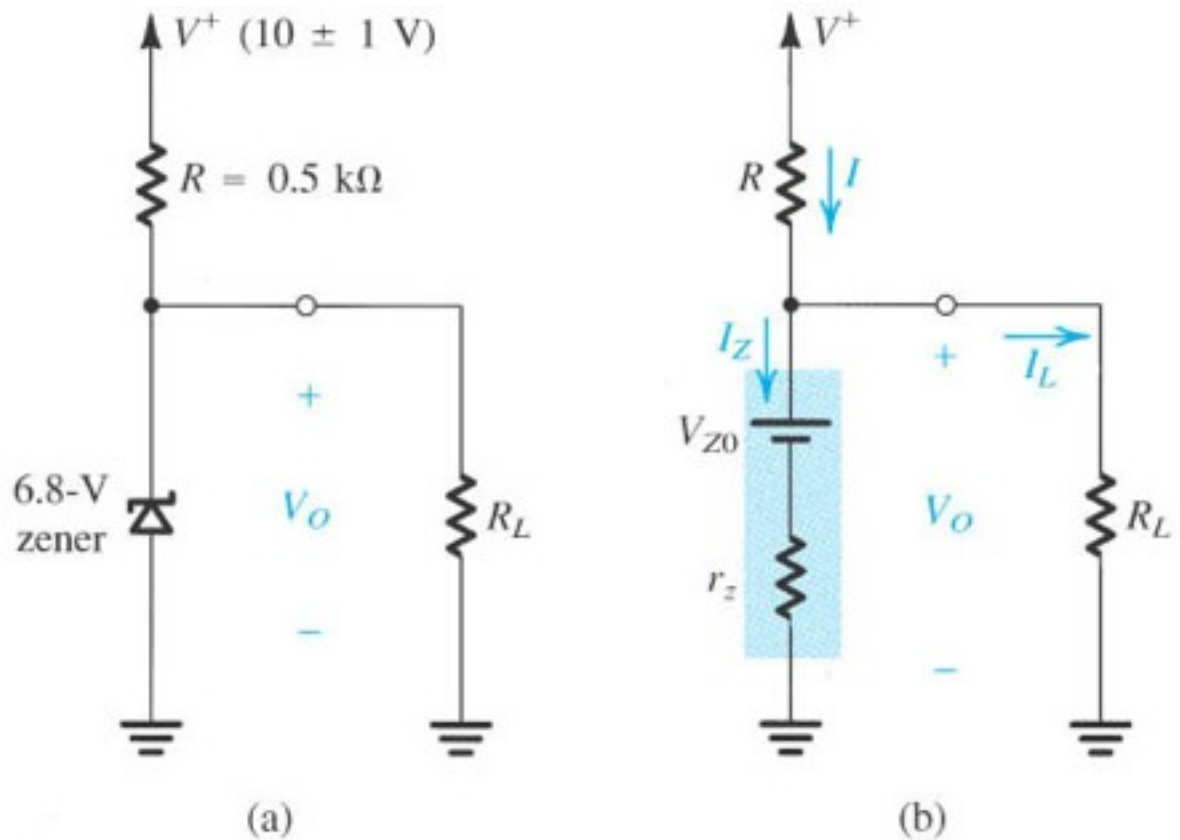


Figure 3.23 **(a)** Circuit for Example 3.8. **(b)** The circuit with the zener diode replaced with its equivalent circuit model.

Circuiti Rettificatori

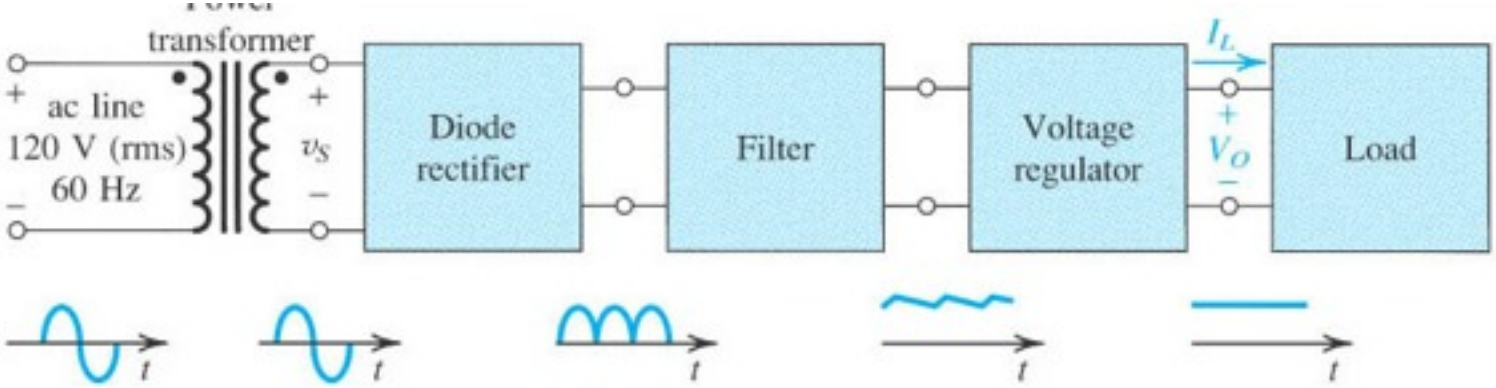
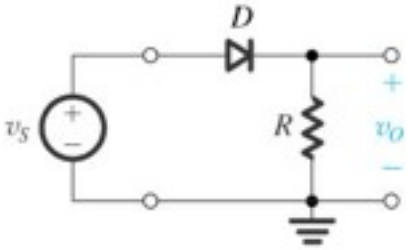
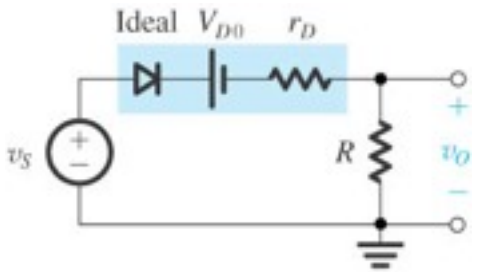


Figure 3.24 Block diagram of a dc power supply.

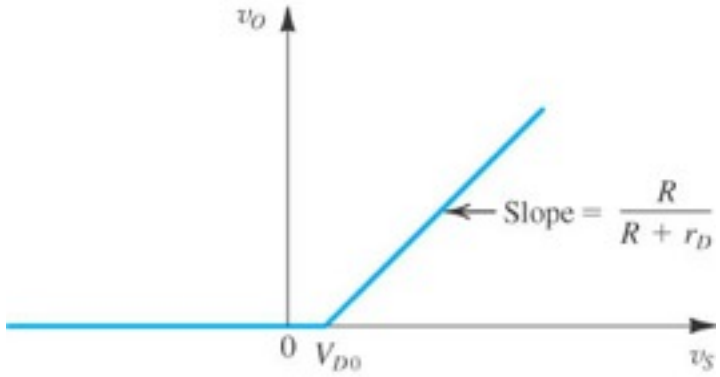


$$v_0 = 0, \qquad \text{(a) } v_s < V_{D0}$$

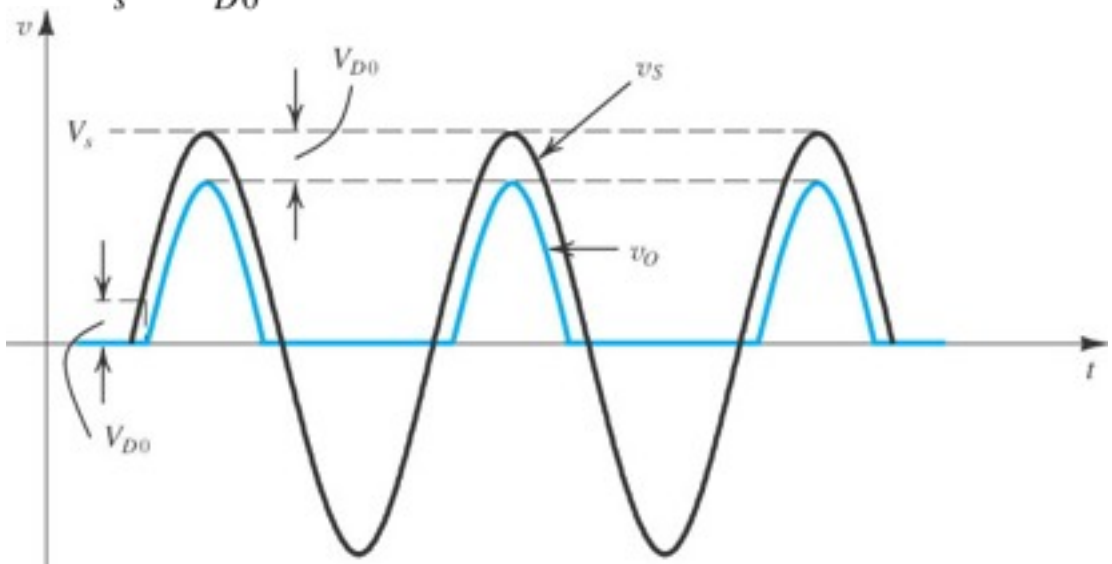
$$v_0 = \frac{R}{R + r_D} v_S - V_{D0} \frac{R}{R + r_D}, \qquad v_s \geq V_{D0}$$



(b)



(c)

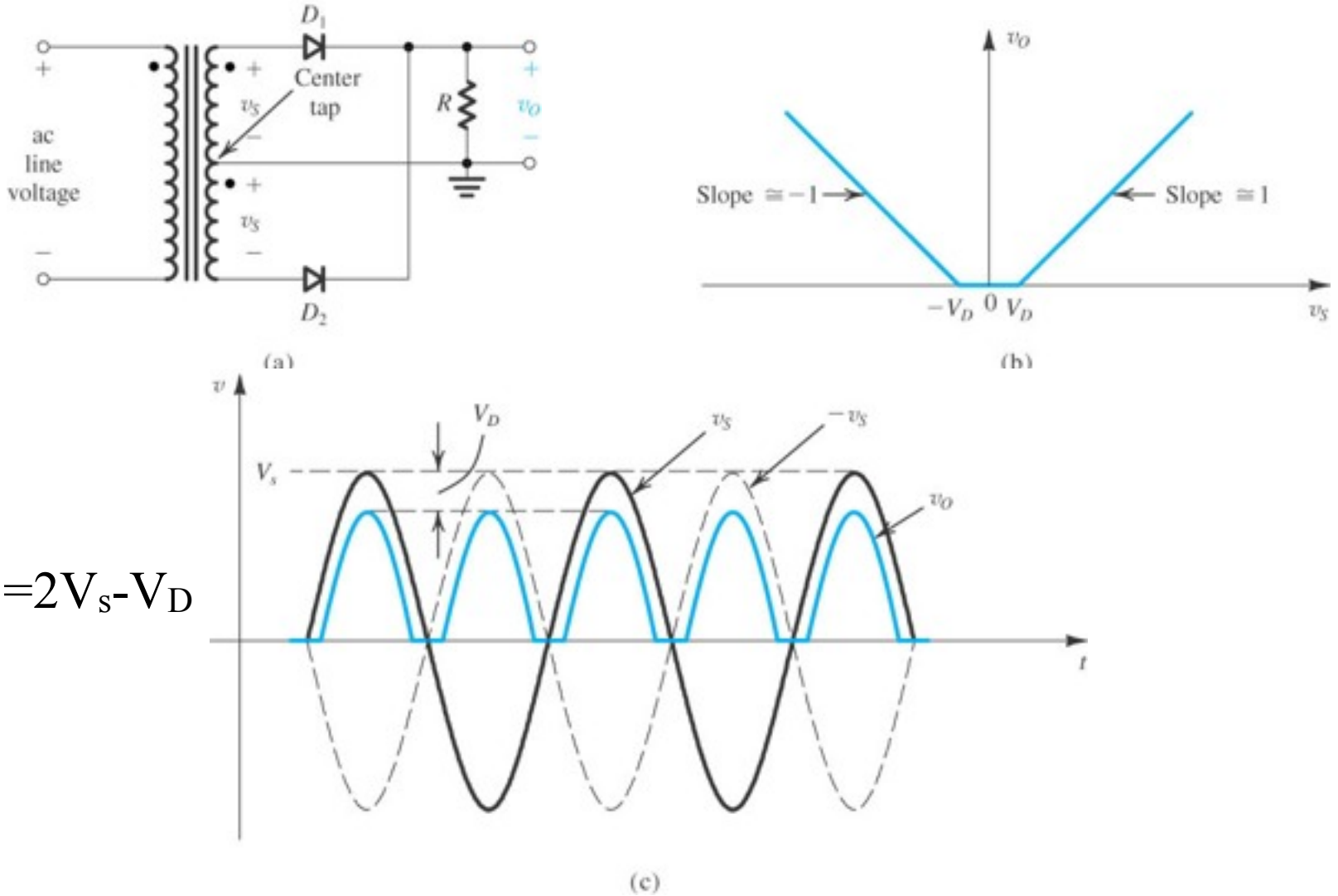


(d)

Due parametri importanti:
- Max. corrente che puo' condurre
- Peak Inverse Voltatge, PIV. PI<Vs, per evitare breakdown

Figure 3.25 **(a)** Half-wave rectifier. **(b)** Equivalent circuit of the half-wave rectifier with the diode replaced with its battery-plus-resistance model. **(c)** Transfer characteristic of the rectifier circuit. **(d)** Input and output waveforms, assuming that r_D ! R.

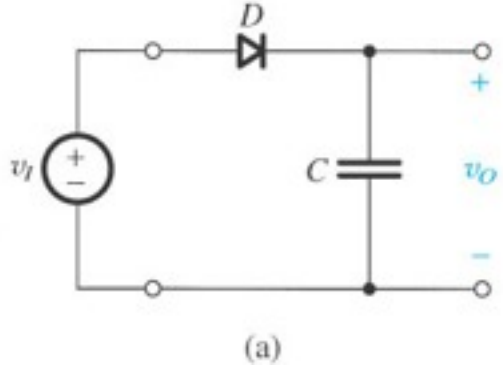
Full wave rectifier



PIV $=2V_s-V_D$

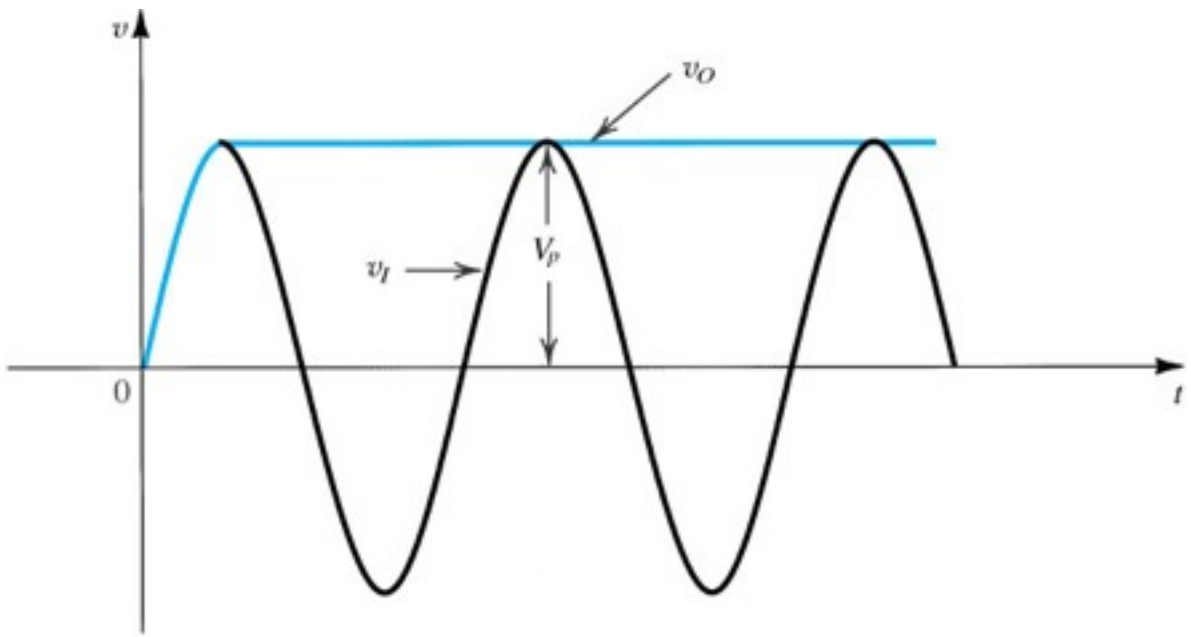
Figure 3.26 Full-wave rectifier utilizing a transformer with a center-tapped secondary winding: **(a)** circuit; **(b)** transfer characteristic assuming a constant-voltage-drop model for the diodes; **(c)** input and output waveforms.

Diodo con filtro capacitivo rettificatore



(a)

Caso ideale

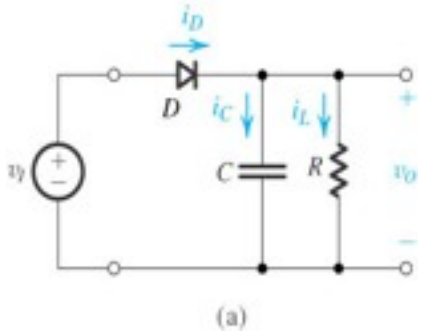


(b)

Figure 3.28 (a) A simple circuit used to il
an ideal diode. Note that the circuit provides a dc voltage equal to the peak of the input sine wave. The circuit is therefore known as a peak rectifier or a peak detector.

Caso reale, diodo ideale

Condizioni stazionarie, RC>>T



$$i_L = v_0 / R$$

e la corrente del diodo

$$i_D = i_C + i_L = C\frac{dv_i}{dt} + i_L$$

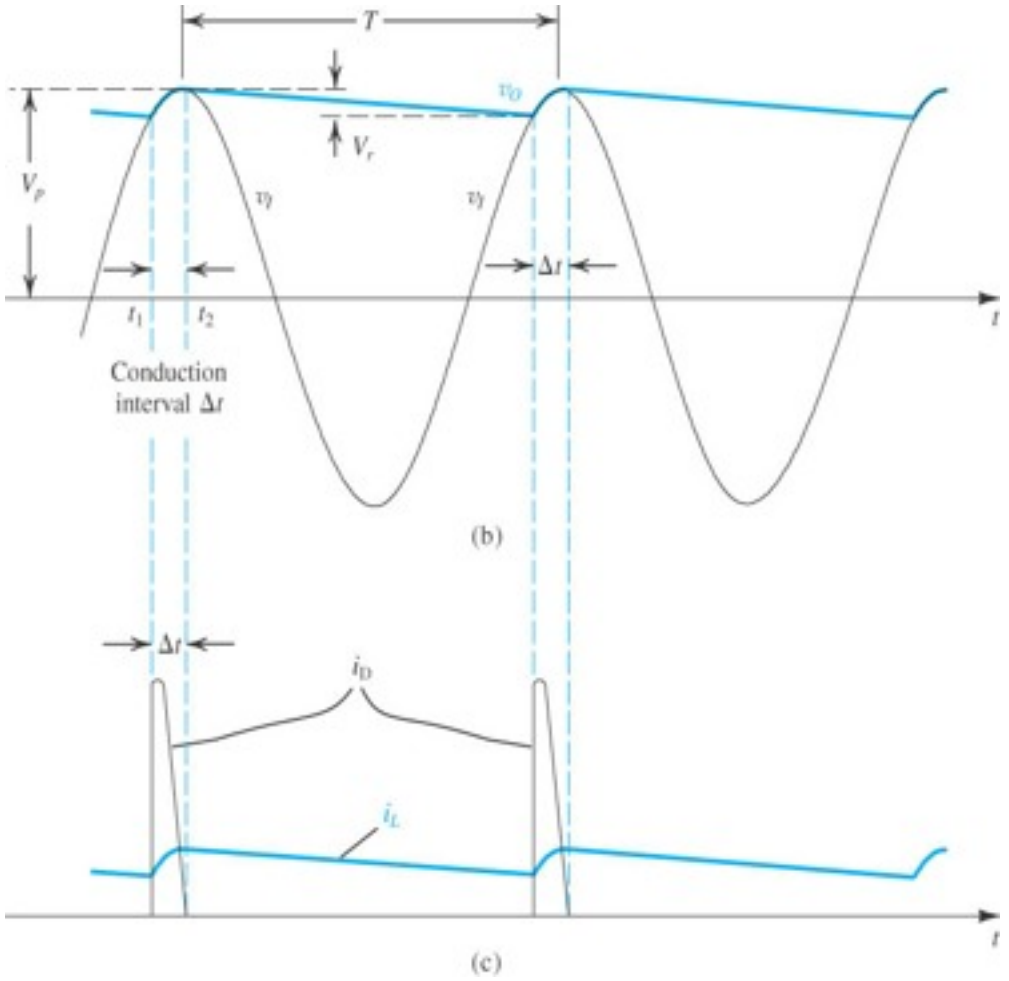


Figure 3.29 Voltage and current waveforms in the peak rectifier circuit with *CR* @ *T*. The diode is assumed ideal.

Osservazioni:

1. Il diodo conduce per un tempo breve, Δt vicino al picco del segnale
2. la conduzione del diodo inizia al tempo t1 quando la vi uguaglia la v^0
3. quando il diodo e' off il condensatore si scarica attraverso R, se CR>>T, V_r molto piccolo
4. quando V_r piccolo, v_0 quasi uguale al valore di picco di v_i per cui $I_L=V_p/R$ e si [uo' scrivere $V_0=V_p-1/2\ V_r$

Con queste osservazioni si puo' ricavare l'epressione per Vr e per la media ed il valore di picco della corrente del diodo

$$v_0 = V_p e^{-t/CR}$$

al termine della discarica $$V_p - V_r \cong V_p e^{-T/RC}$$

ma per CR >>T, $$e^{-T/RC} = 1 - T/CR$$

quindi per avere la Vr piccola, **tensione di ripple piccola,** si deve scegliere C tale che CR>>T

cosi' con f=1/T si puo' scrivere che $$V_r = \frac{V_p}{fCR}$$

Quanto sara' grande l'intervallo di conduzione?

Se si suppone che la conduzione del diodo cessi al picco vi allora si puo' scrivere $V_p \cos(\omega \Delta t) = V_p - V_r$

dove $\omega = 2\pi f$ e' la frequenza angolare di v_I

Ora $\omega \Delta t$ e' un angolo piccolo e possiamo approssimare $\cos(\omega \Delta t) \simeq 1 - 1/2(\omega \Delta t)^2$

$$\omega \Delta t \simeq \sqrt{2V_r/V_p}$$

che conferma che per Vr<<Vp l'angolo sara'piccolo e quindi piccolo il ripple

La corrente media del diodo in conduzione, i_{Dav}

$$Q_{Cond} = i_{Cav} \Delta t \quad , ma \quad i_{Cav} = i_{Dav} - I_L \quad e\, Q_{disc} = CV \quad nell'\,\text{int}\, ervallo\, della\, discarica$$

$$i_{Dav} = I_L(1 + \pi\sqrt{2V_r/V_p})$$

Come si vede per Vr<<Vp la correntedi conduzione e' molto piu' grande della corrente di load; questo e' dovuto al fatto che il diodo
deve recuperre le cariche pese dal condensatore in un tempo molto breve.

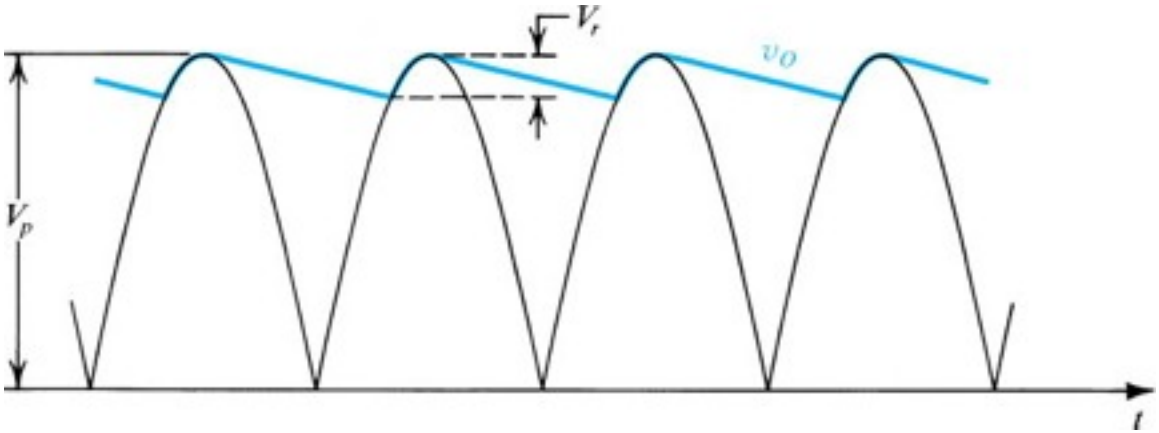


Figure 3.30 Waveforms in the full-wave peak rectifier.

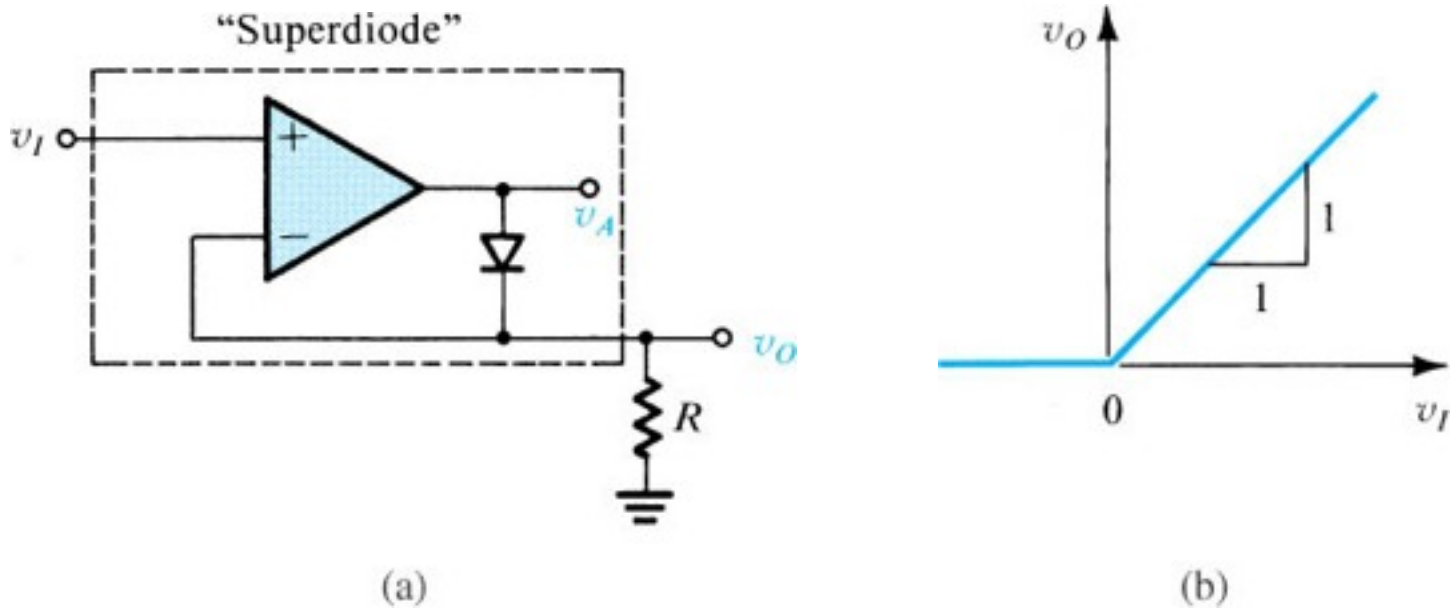


Figure 3.31 The "superdiode" precision half-wave rectifier and its almost-ideal transfer characteristic. Note that when $v_I > 0$ and the diode conducts, the op amp supplies the load current, and the source is conveniently buffered, an added advantage. Not shown are the op-amp power supplies.

Circuito limitatore

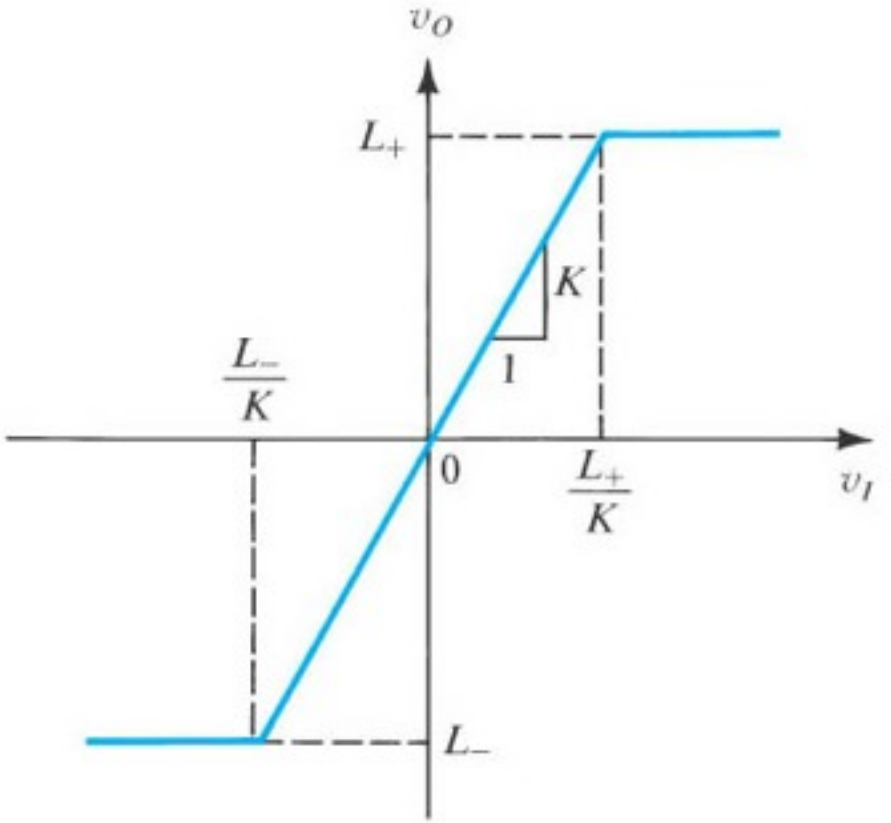


Figure 3.32 General transfer characteristic for a limiter circuit.

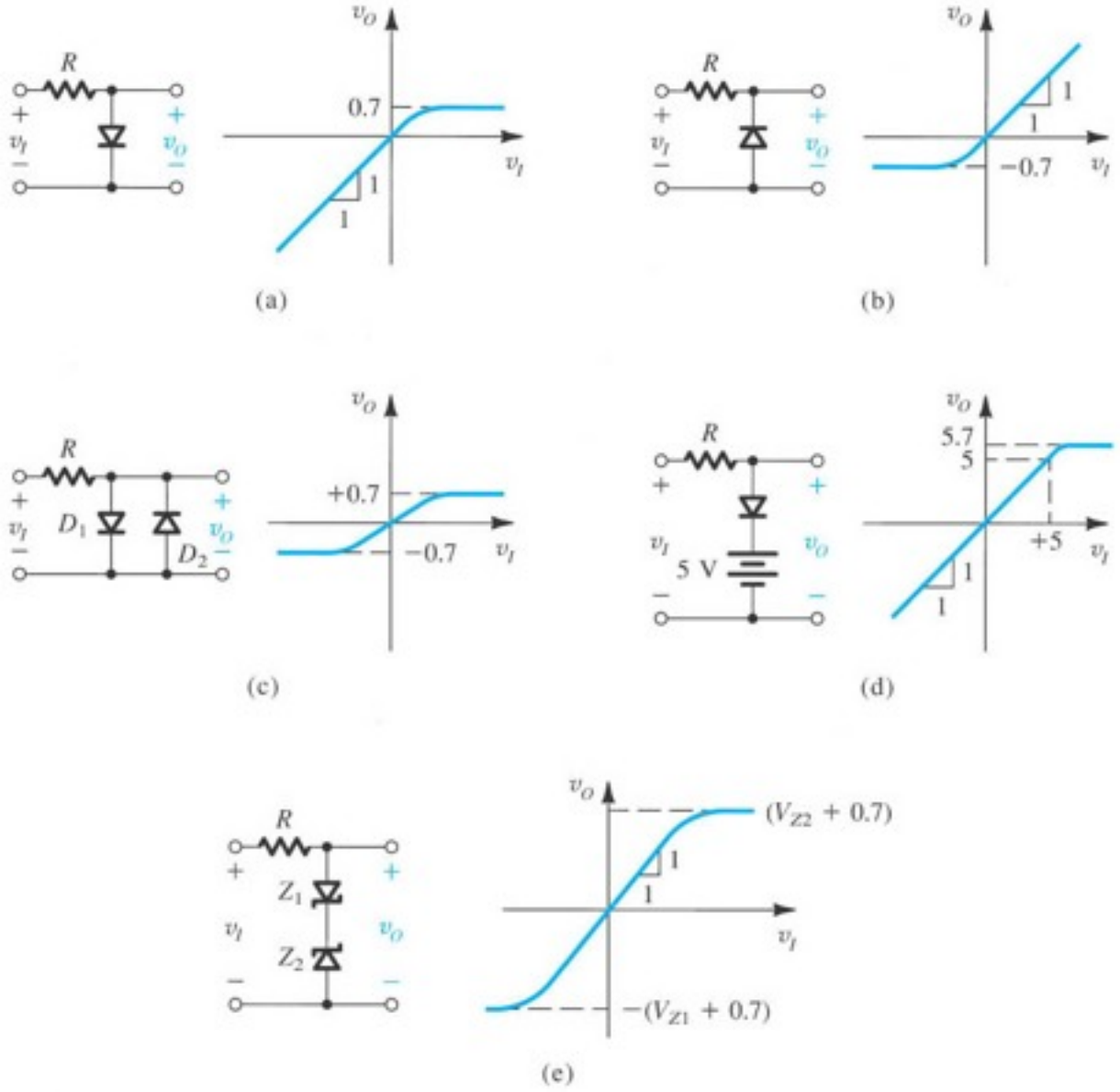


Figure 3.35 A variety of basic limiting circuits.

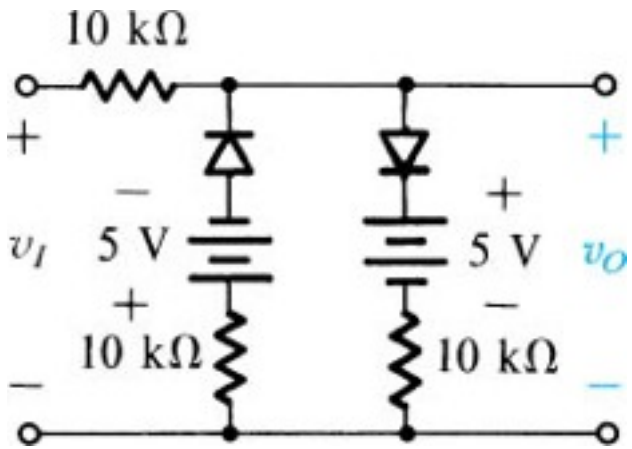


Figure E3.27

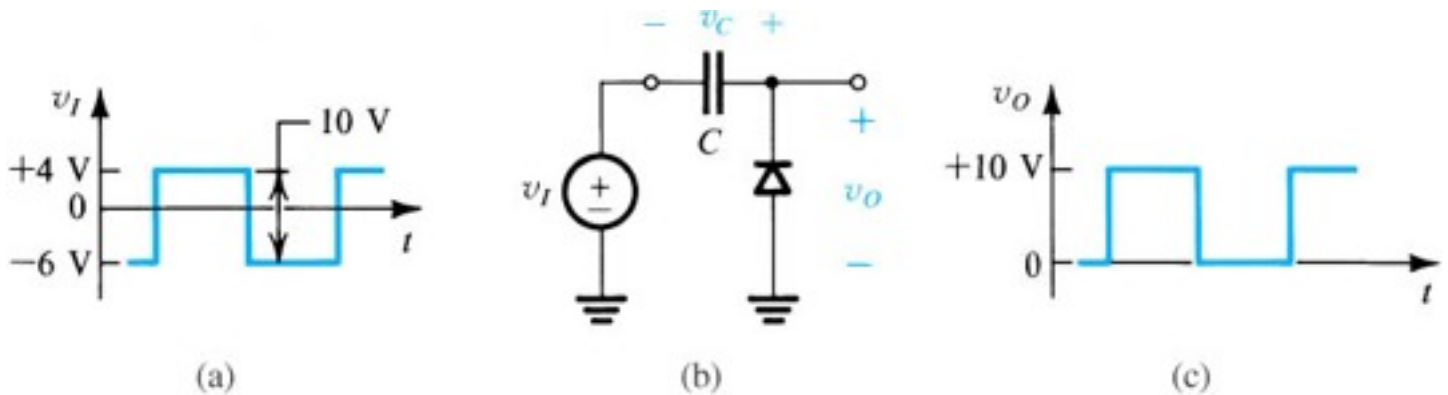


Figure 3.36 The clamped capacitor or dc restorer with a square-wave input and no load.

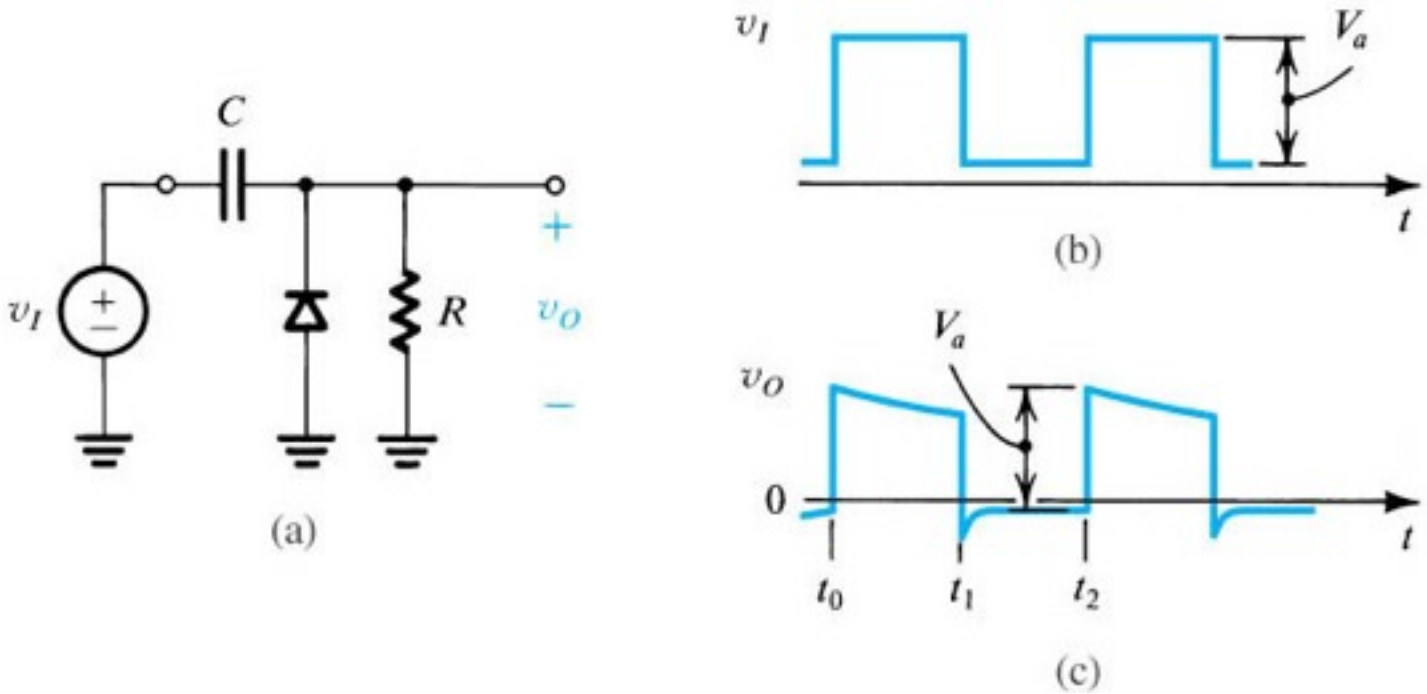


Figure 3.37 The clamped capacitor with a load resistance R.

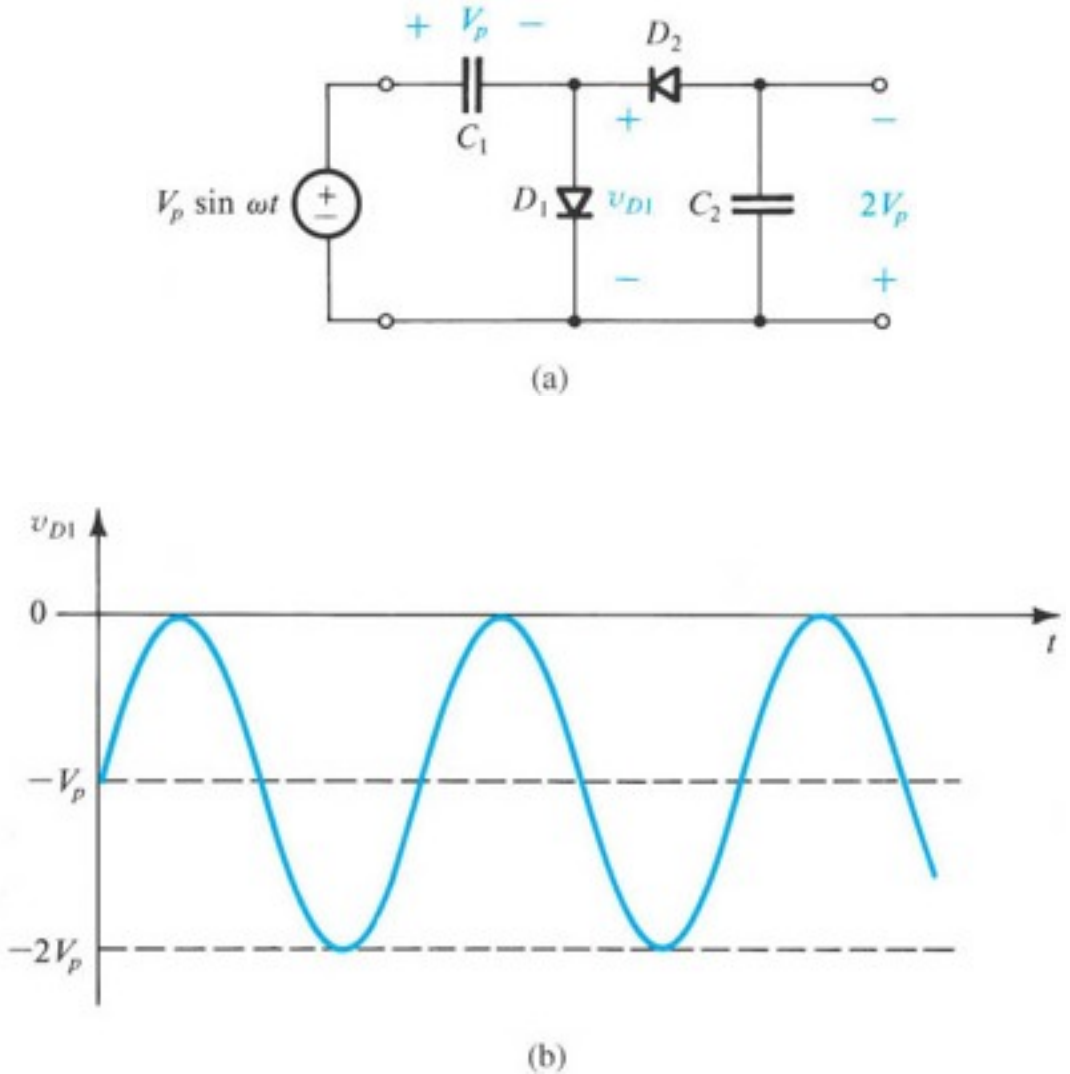


Figure 3.38 Voltage doubler: **(a)** circuit; **(b)** waveform of the voltage across D_1.

Struttura fisica del diodo

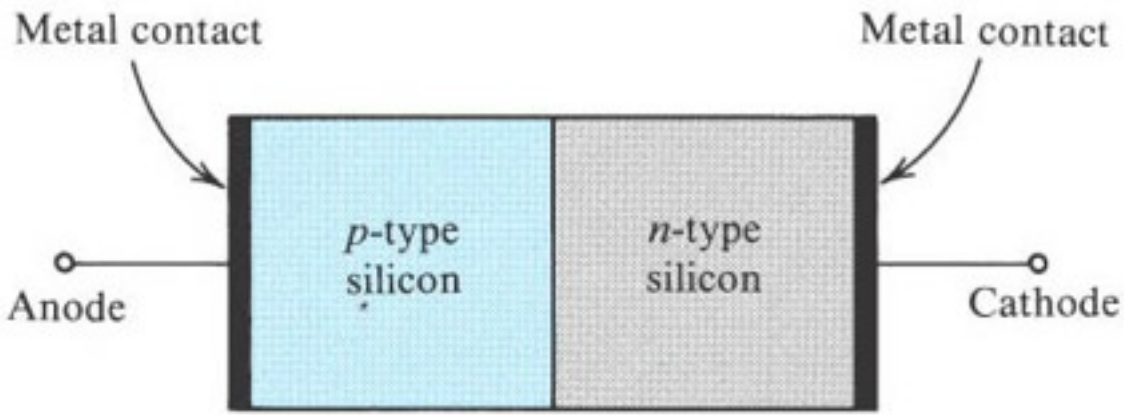


Figure 3.39 Simplified physical structure of the junction diode. (Actual geometries are given in Appendix A.)

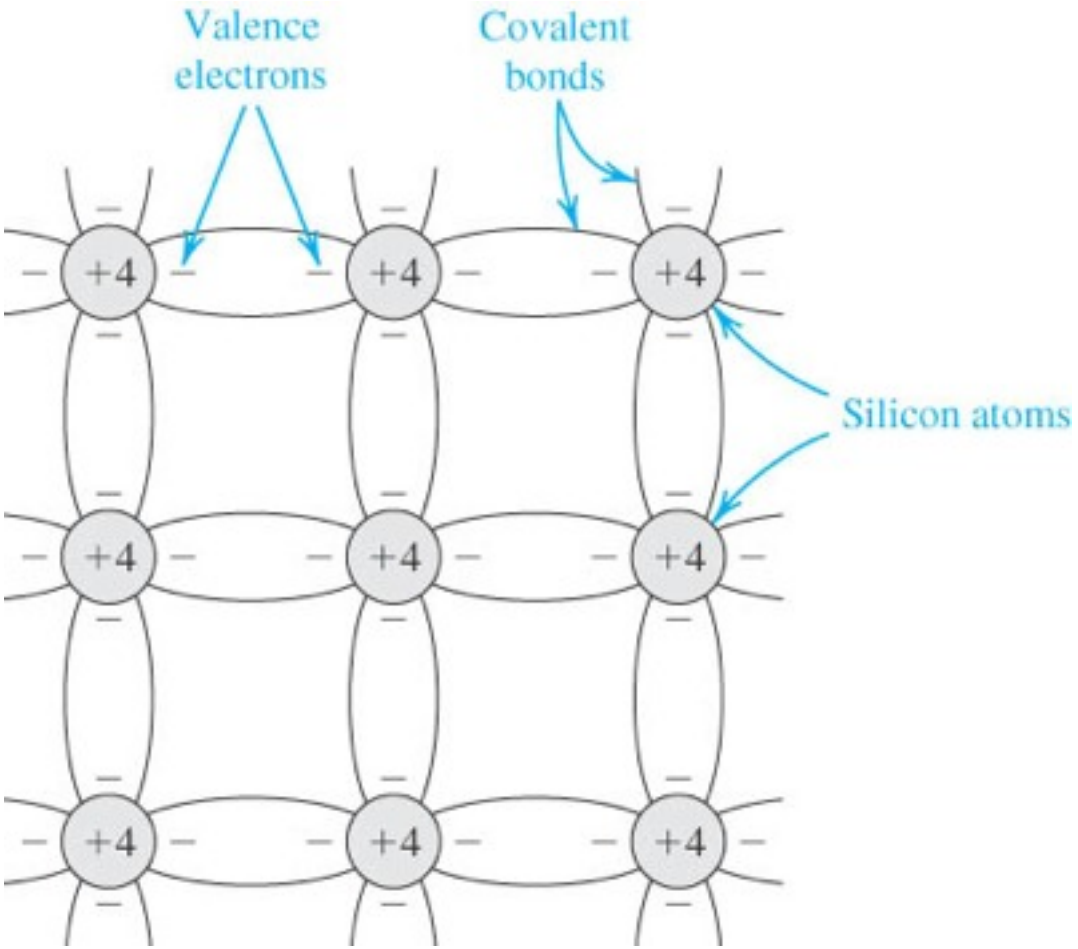


Figure 3.40 Two-dimensional representation of the silicon crystal. The circles represent the inner core of silicon atoms, with +4 indicating its positive charge of +4q, which is neutralized by the charge of the four valence electrons. Observe how the covalent bonds are formed by sharing of the valence electrons. At 0 K, all bonds are intact and no free electrons are available for current conduction.

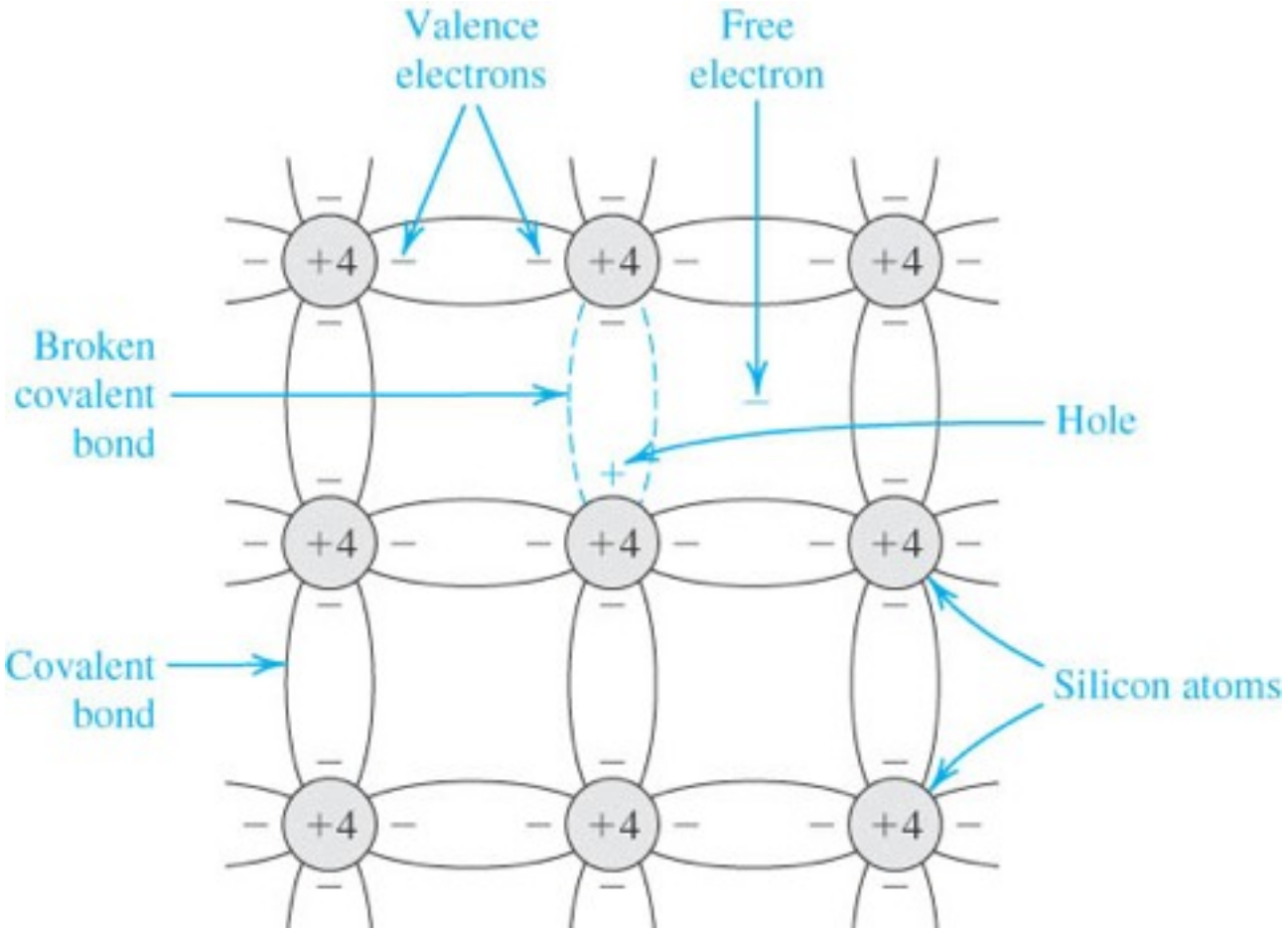


Figure 3.41 At room temperature, some of the covalent bonds are broken by thermal ionization. Each broken bond gives rise to a free electron and a hole, both of which become available for current conduction.

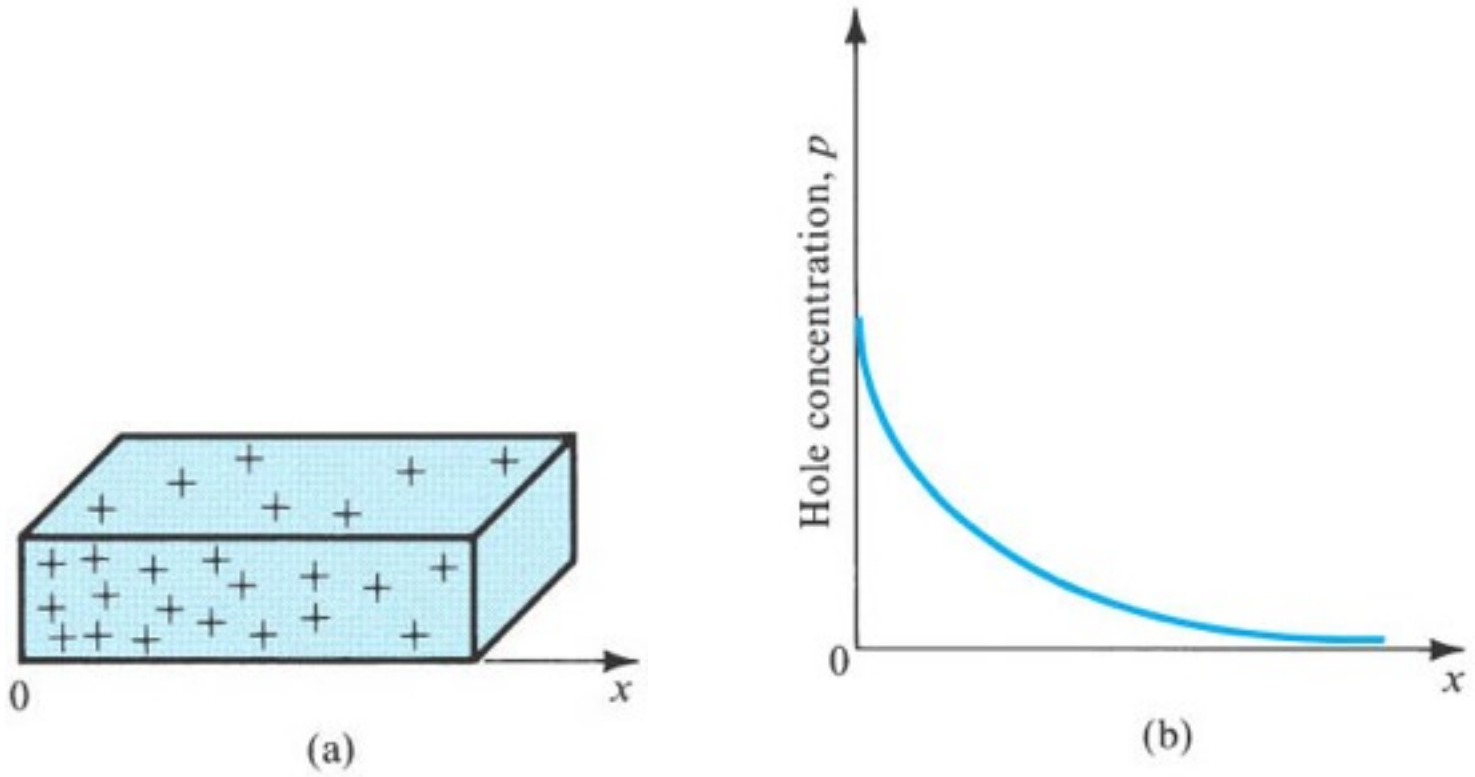


Figure 3.42 A bar of intrinsic silicon **(a)** in which the hole concentration profile shown in **(b)** has been created along the *x*-axis by some unspecified mechanism.

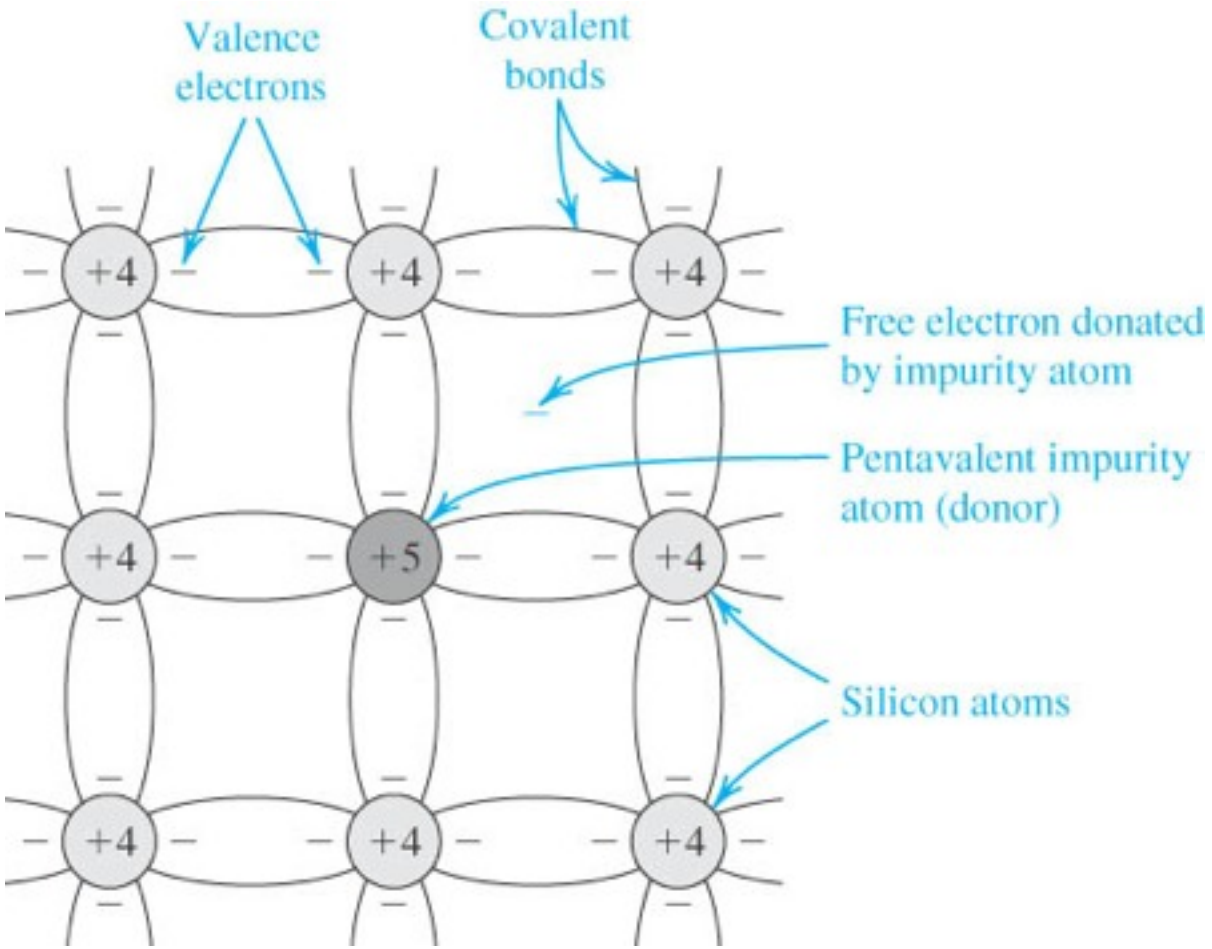


Figure 3.43 A silicon crystal doped by a pentavalent element. Each dopant atom donates a free electron and is thus called a donor. The doped semiconductor becomes *n* type.

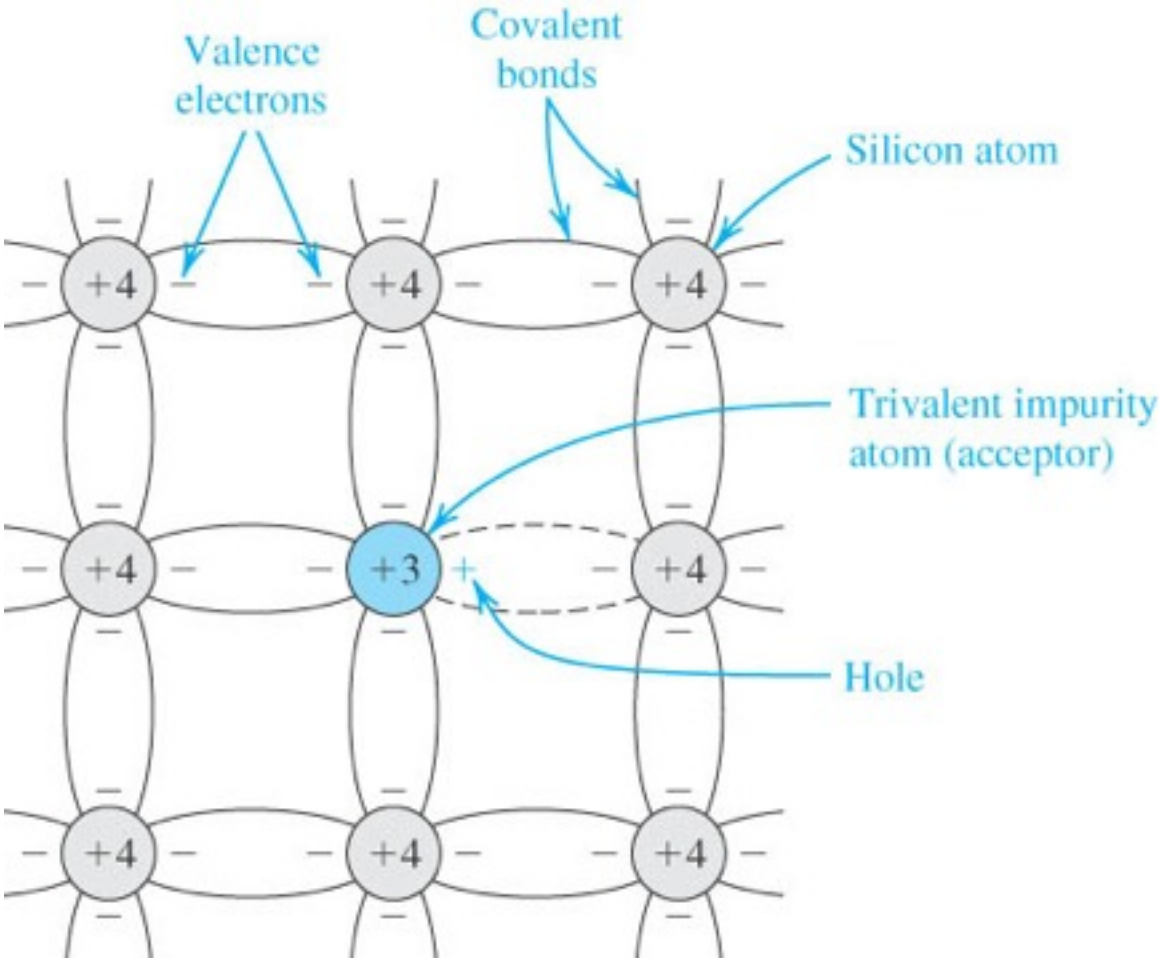


Figure 3.44 A silicon crystal doped with a trivalent impurity. Each dopant atom gives rise to a hole, and the semiconductor becomes *p* type.

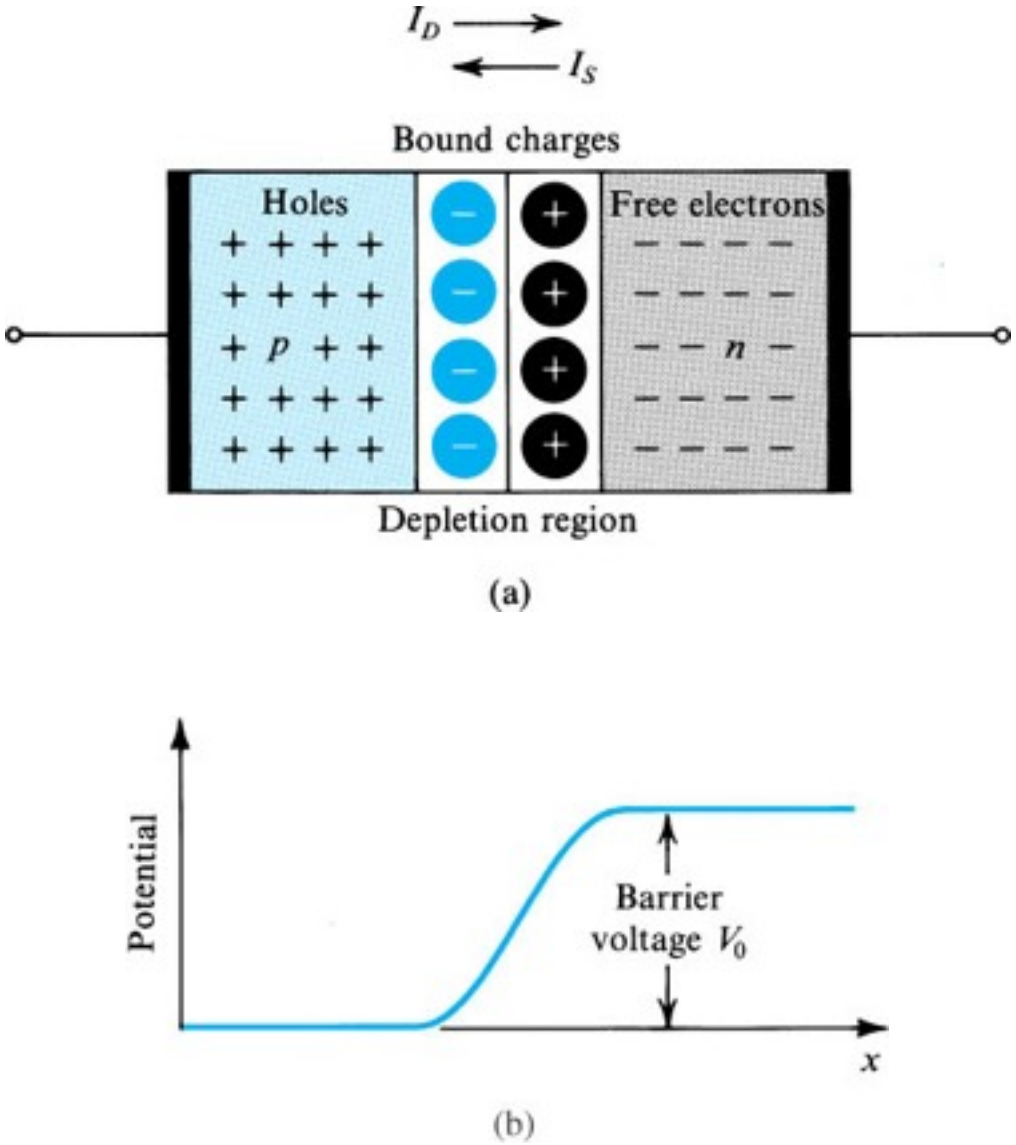


Figure 3.45 **(a)** The *pn* junction with no applied voltage (open-circuited terminals). **(b)** The potential distribution along an axis perpendicular to the junction.

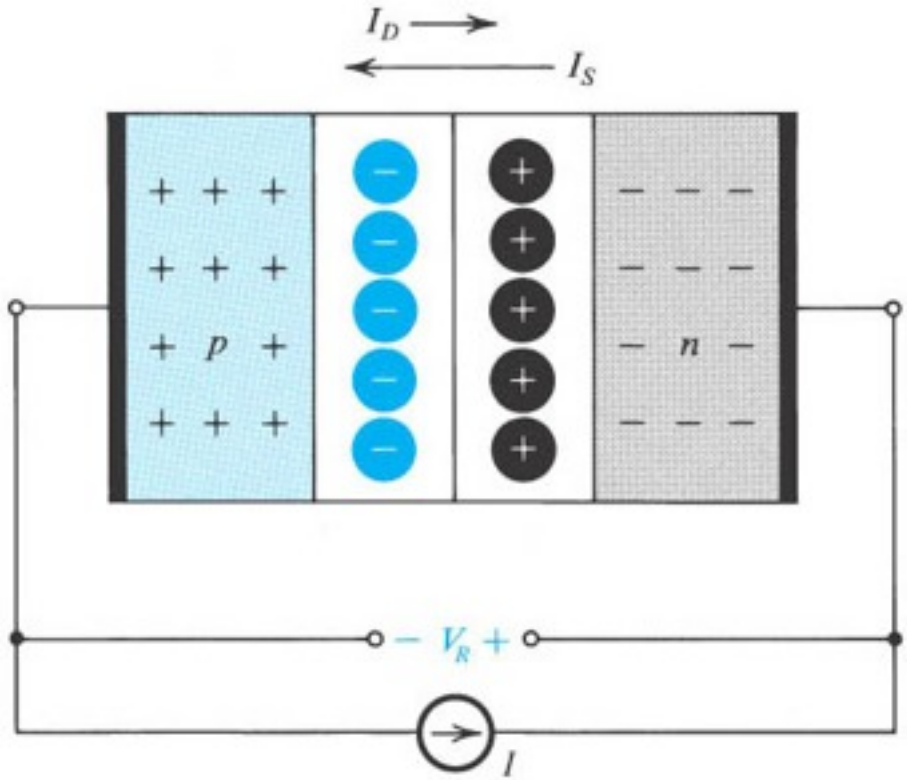


Figure 3.46 The *pn* junction excited by a constant-current source I in the reverse direction. To avoid breakdown, I is kept smaller than I_S. Note that the depletion layer widens and the barrier voltage increases by V_R volts, which appears between the terminals as a reverse voltage.

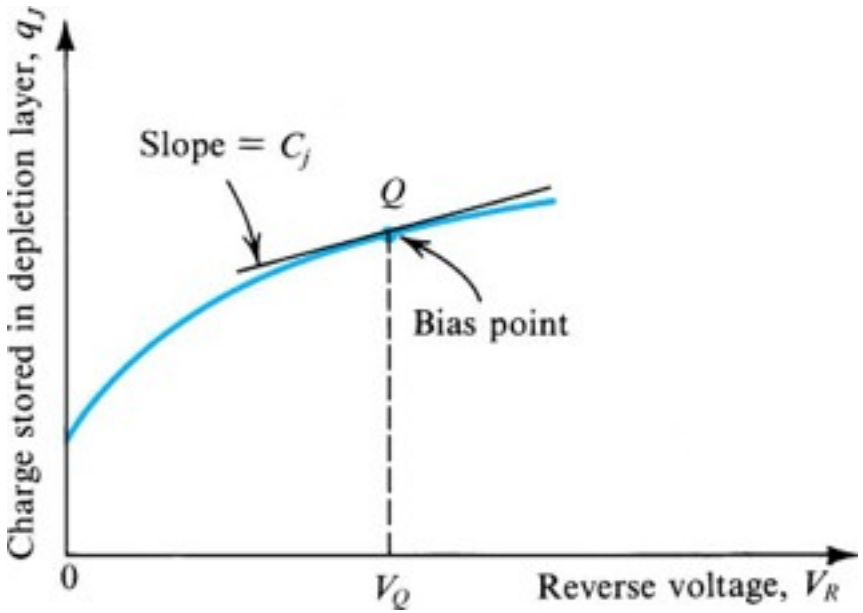


Figure 3.47 The charge stored on either side of the depletion layer as a function of the reverse voltage V_R.

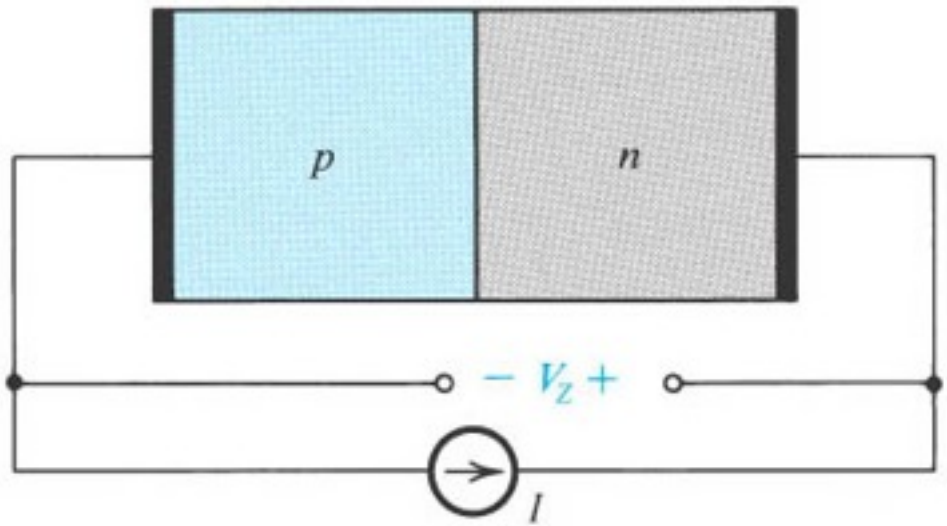


Figure 3.48 The *pn* junction excited by a reverse-current source I, where $I > I_S$. The junction breaks down, and a voltage V_Z, with the polarity indicated, develops across the junction.

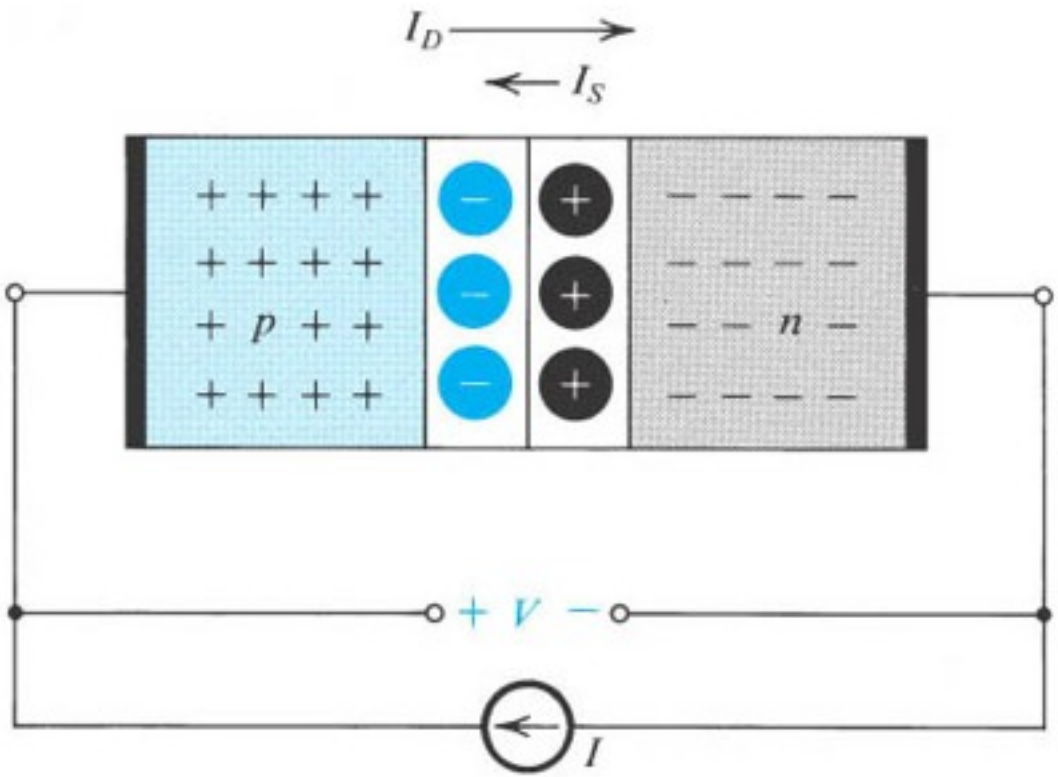


Figure 3.49 The *pn* junction excited by a constant-current source supplying a current I in the forward direction. The depletion layer narrows and the barrier voltage decreases by V volts, which appears as an external voltage in the forward direction.

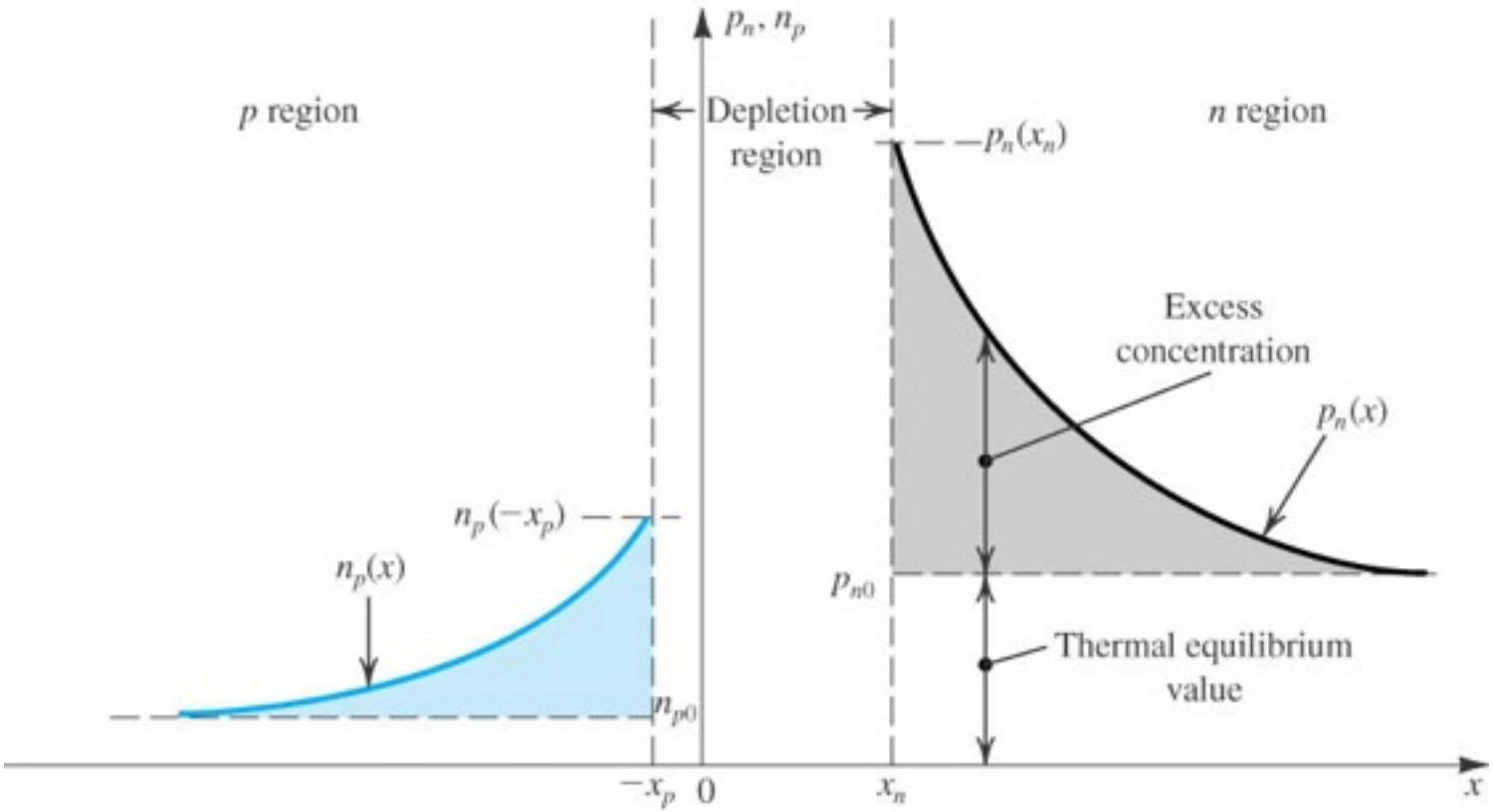
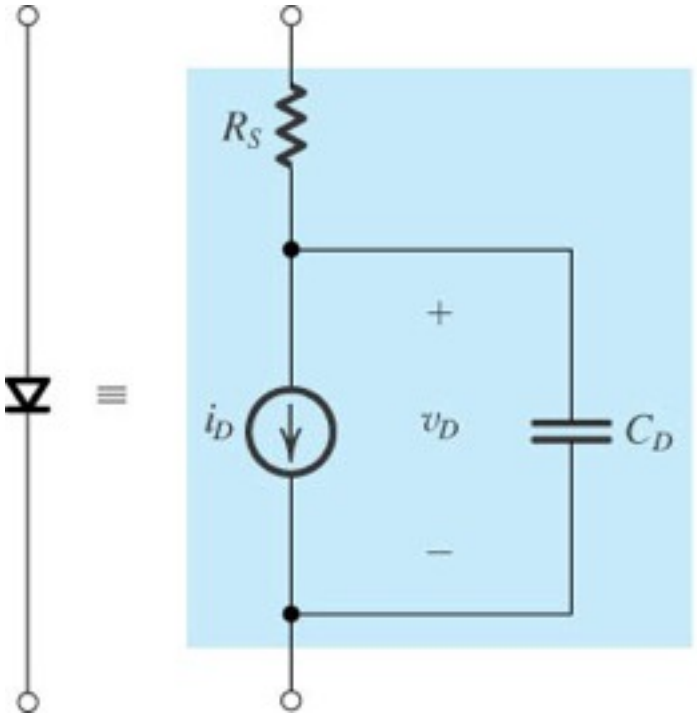


Figure 3.50 Minority-carrier distribution in a forward-biased *pn* junction. It is assumed that the *p* region is more heavily doped than the *n* region; N_A @ N_D.



$$i_D = I_S\left(e^{v_D/nV_T} - 1\right)$$

$$C_D = C_d + C_j = \frac{\tau_T}{V_T} I_S e^{v_D/nV_T} + C_{j0}\Big/\left(1 - \frac{v_D}{V_0}\right)^m$$

Figure 3.51 The SPICE diode model.

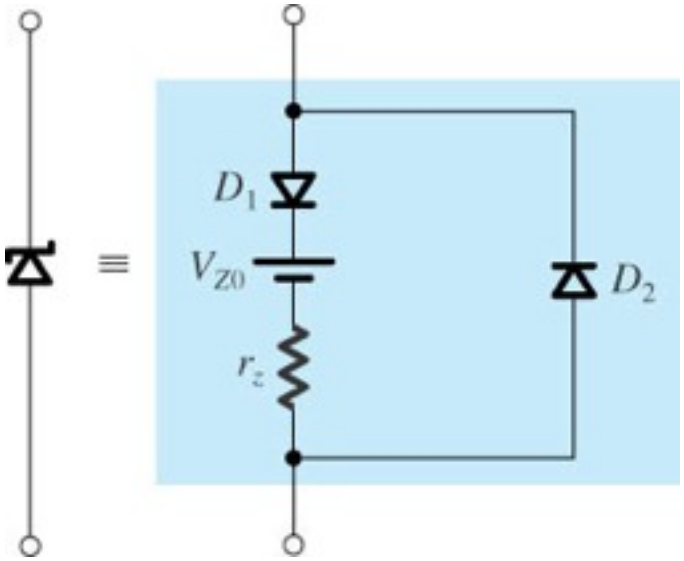


Figure 3.52 Equivalent-circuit model used to simulate the zener diode in SPICE. Diode D_1 is ideal and can be approximated in SPICE by using a very small value for n (say $n = 0.01$).

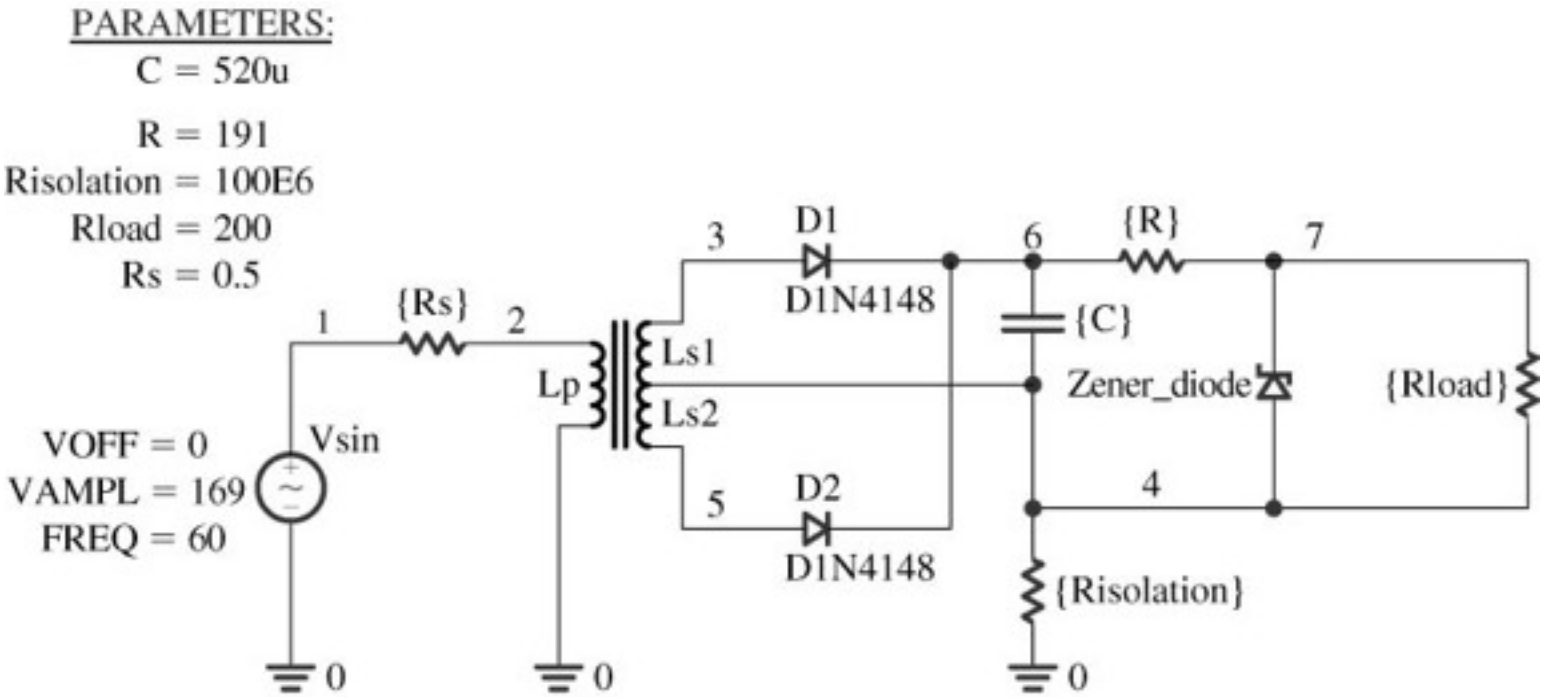


Figure 3.53 Capture schematic of the 5-V dc power supply in Example 3.10.

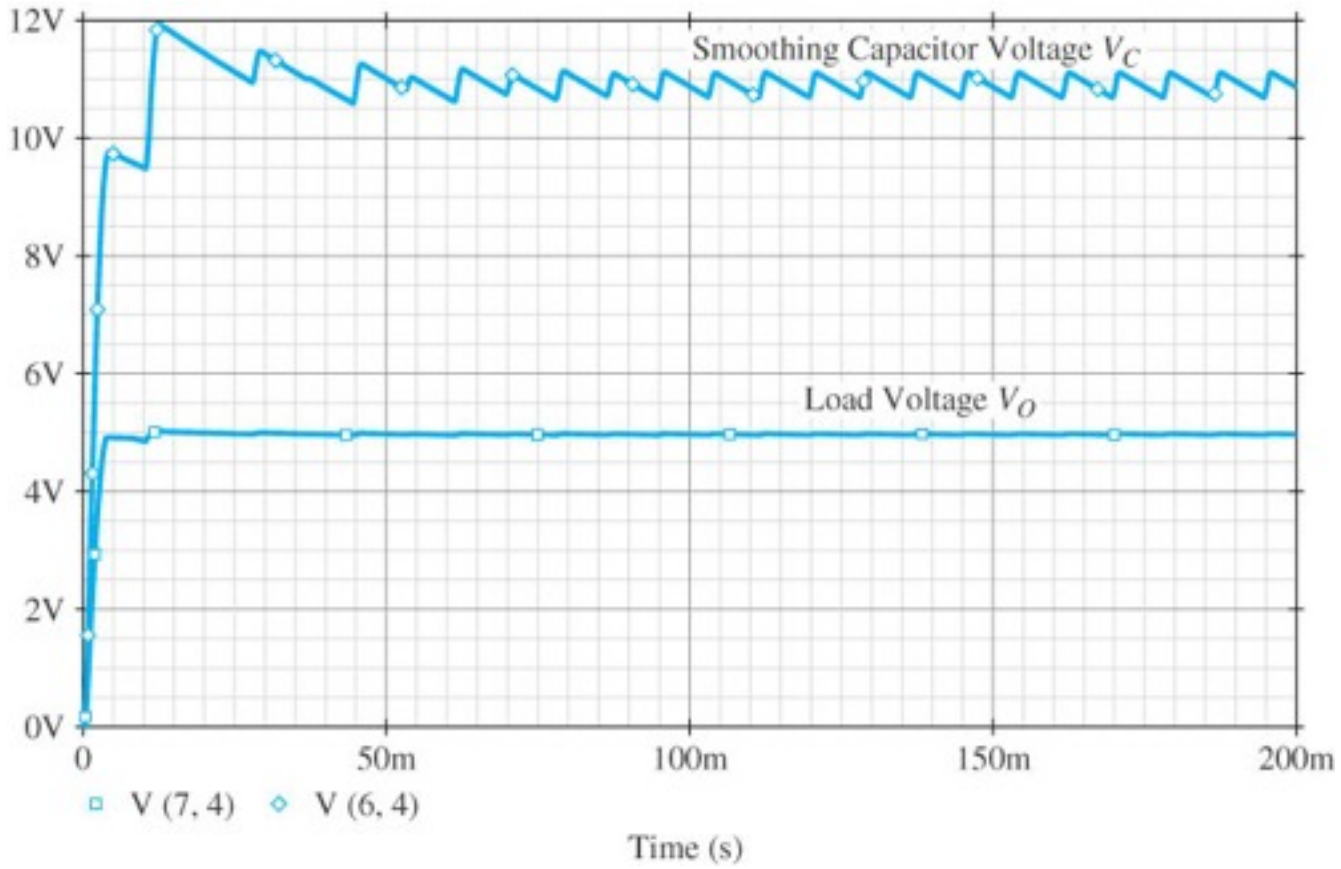


Figure 3.54 The voltage v_C across the smoothing capacitor C and the voltage v_O across the load resistor $R_{load} = 200\ \Omega$ in the 5-V power supply of Example 3.10.

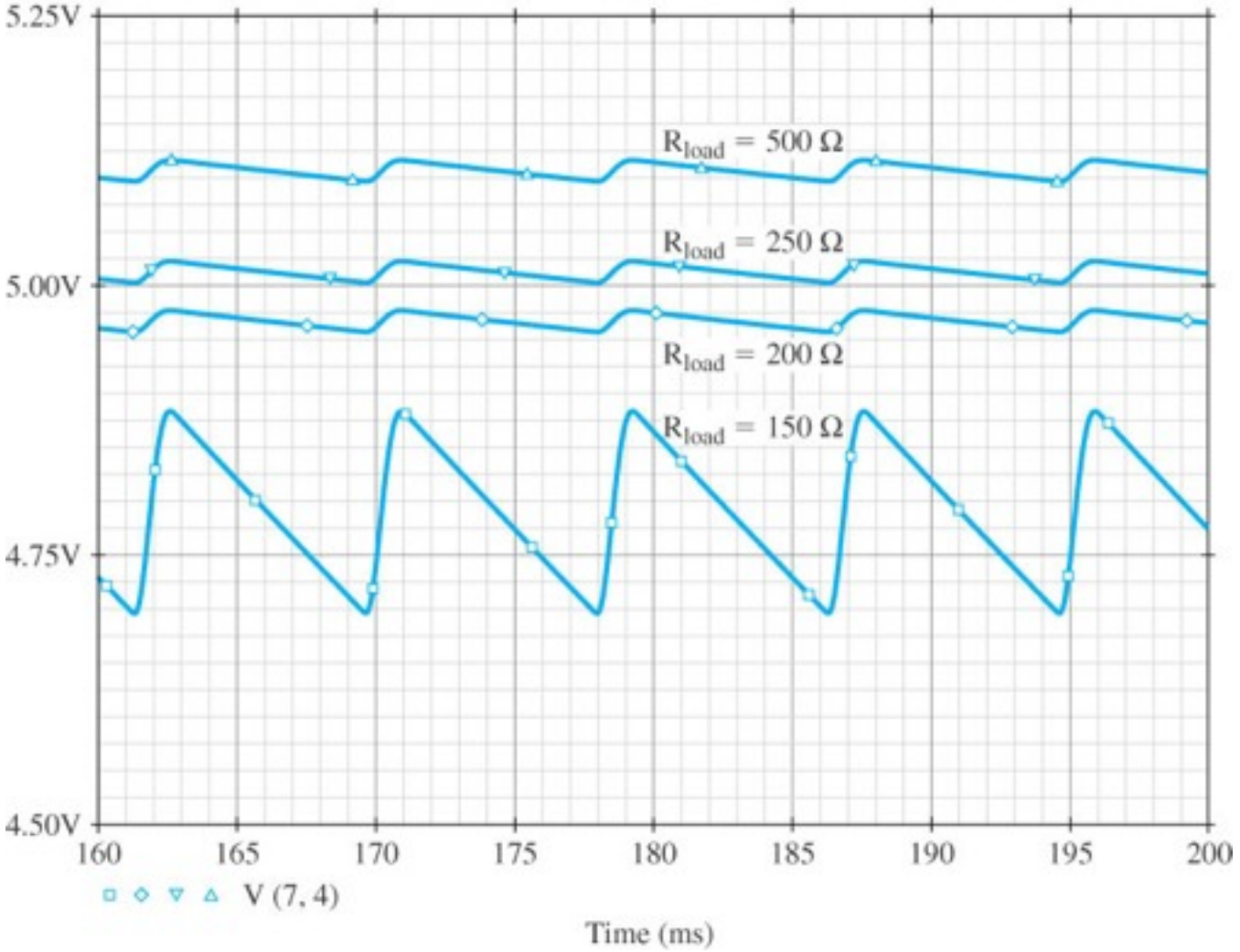


Figure 3.55 The output-voltage waveform from the 5-V power supply (in Example 3.10) for various load resistances: R_{load} = 500 Ω, 250 Ω, 200 Ω, and 150 Ω. The voltage regulation is lost at a load resistance of 150 Ω.

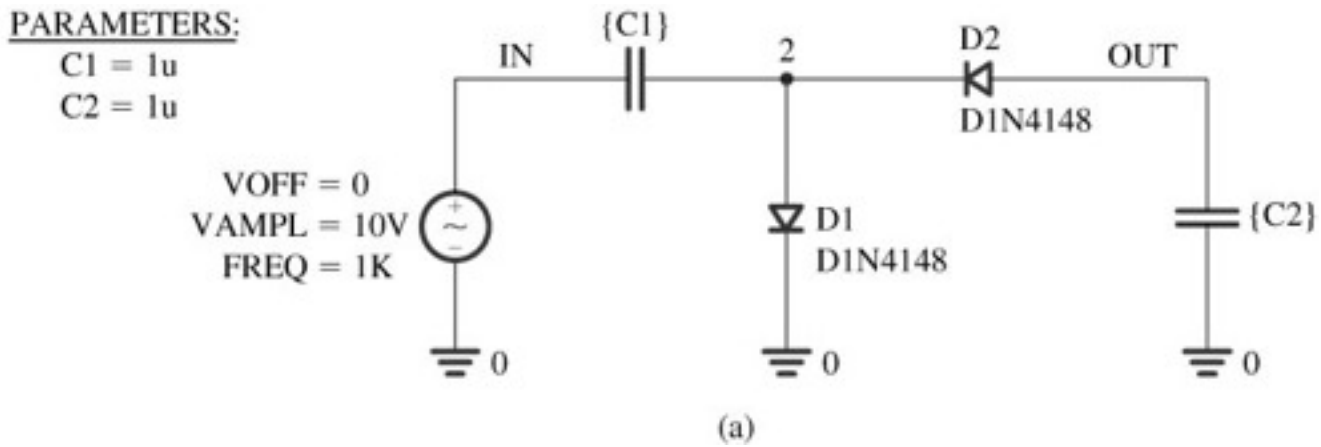


Figure E3.35 (a) Capture schematic of the voltage-doubler circuit (in Exercise 3.35).

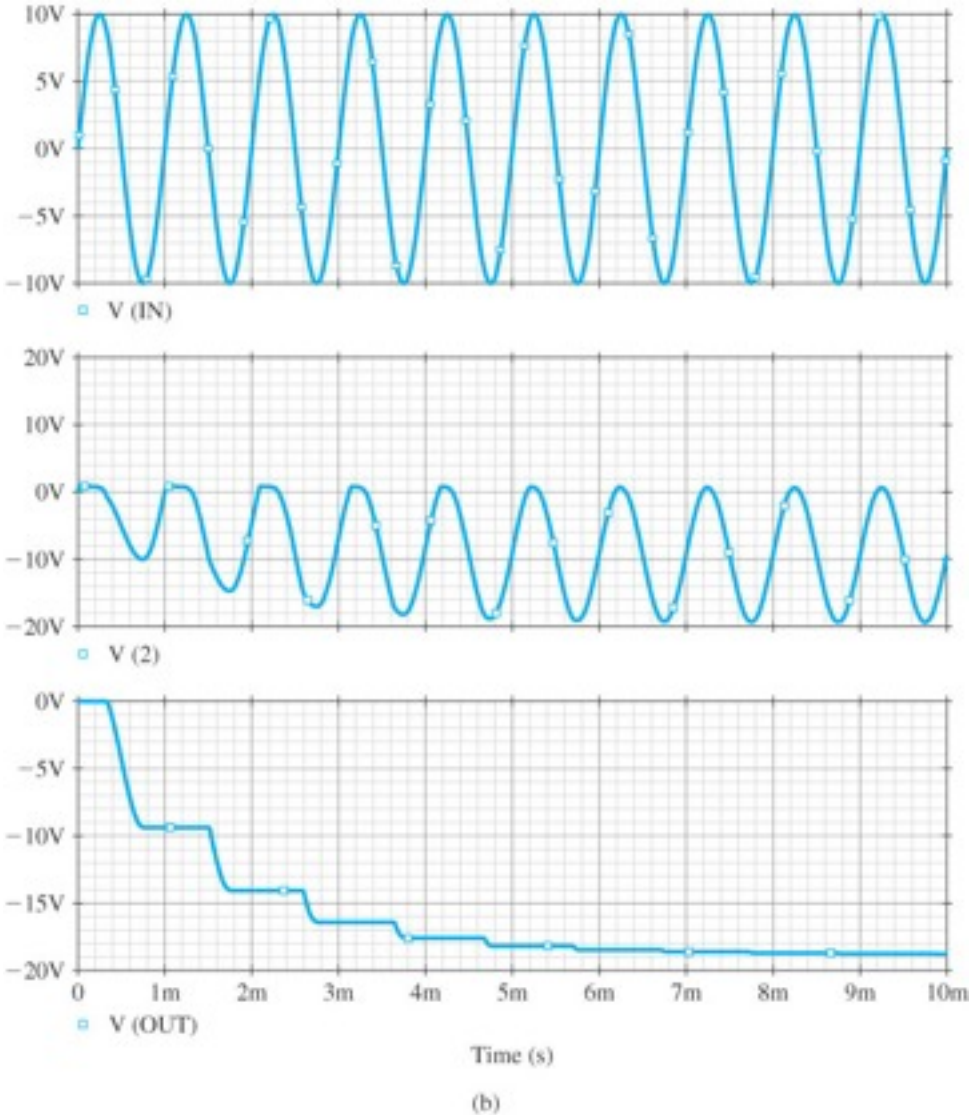


Figure E3.35 *(Continued)* **(b)** Various voltage waveforms in the voltage-doubler circuit. The top graph displays the input sine-wave voltage signal, the middle graph displays the voltage across diode D_1, and the bottom graph displays the voltage that appears at the output.

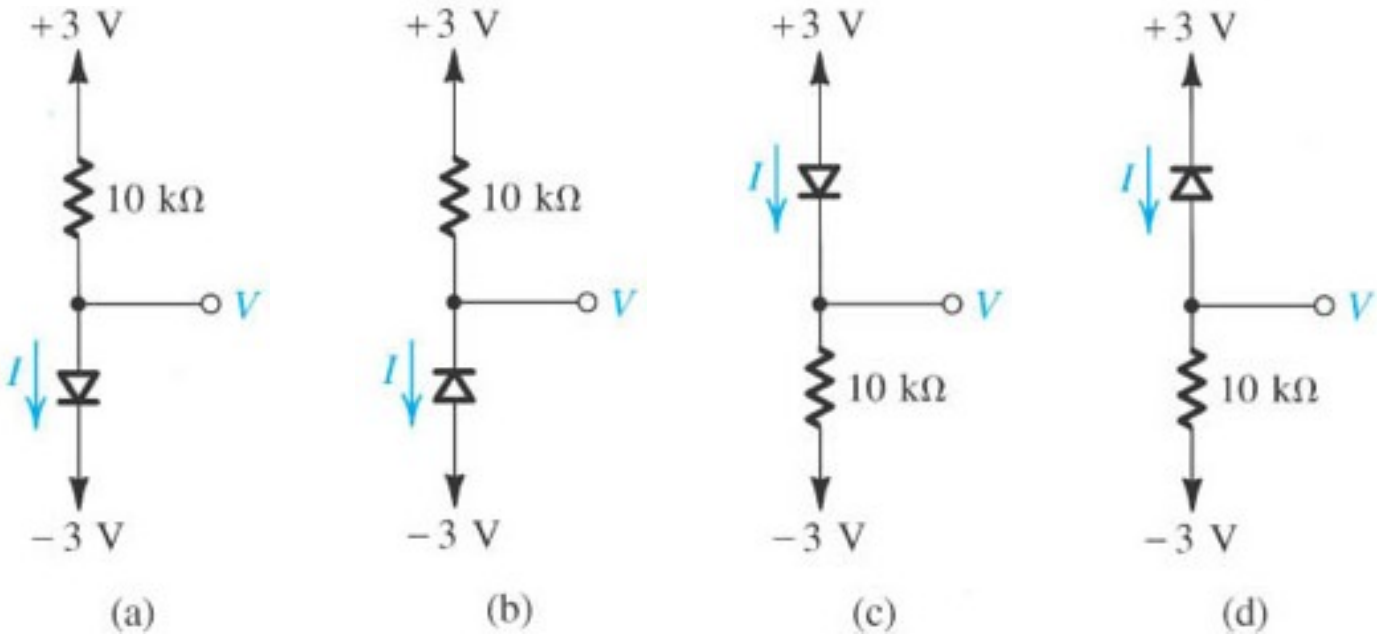


Figure P3.2

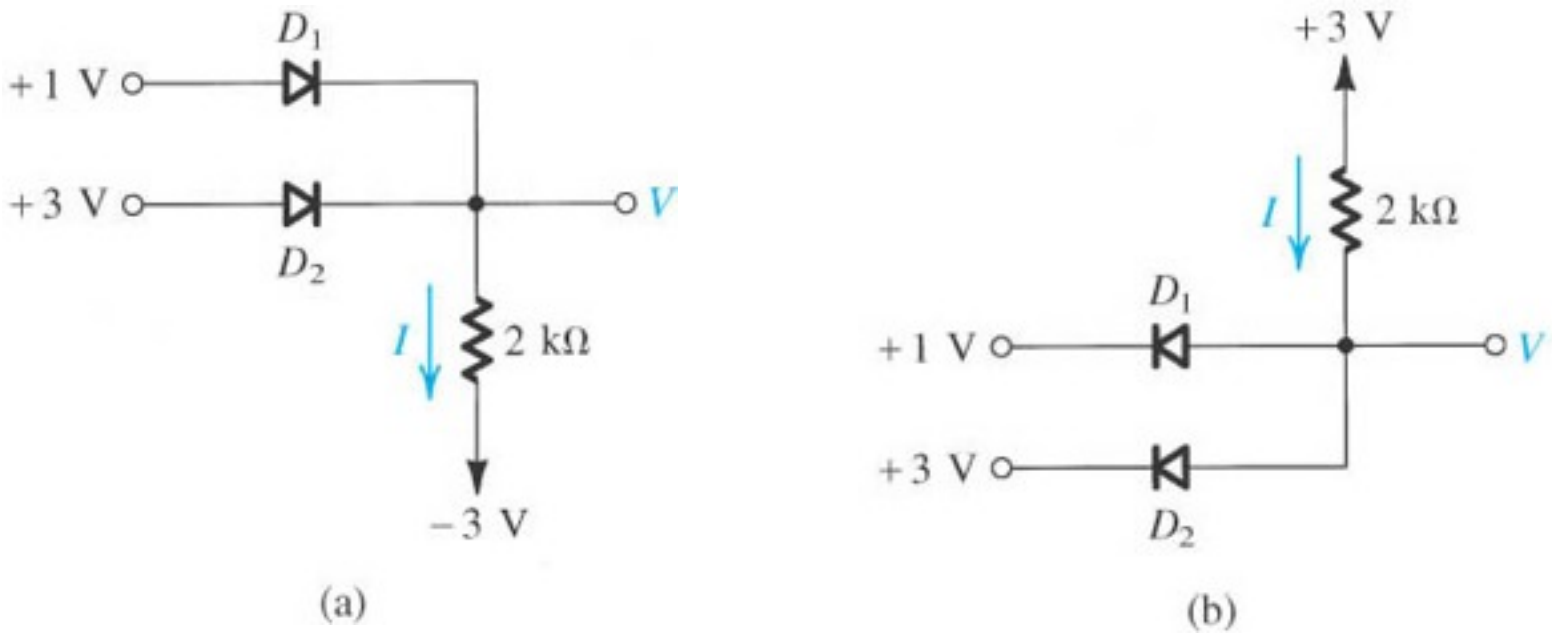


Figure P3.3

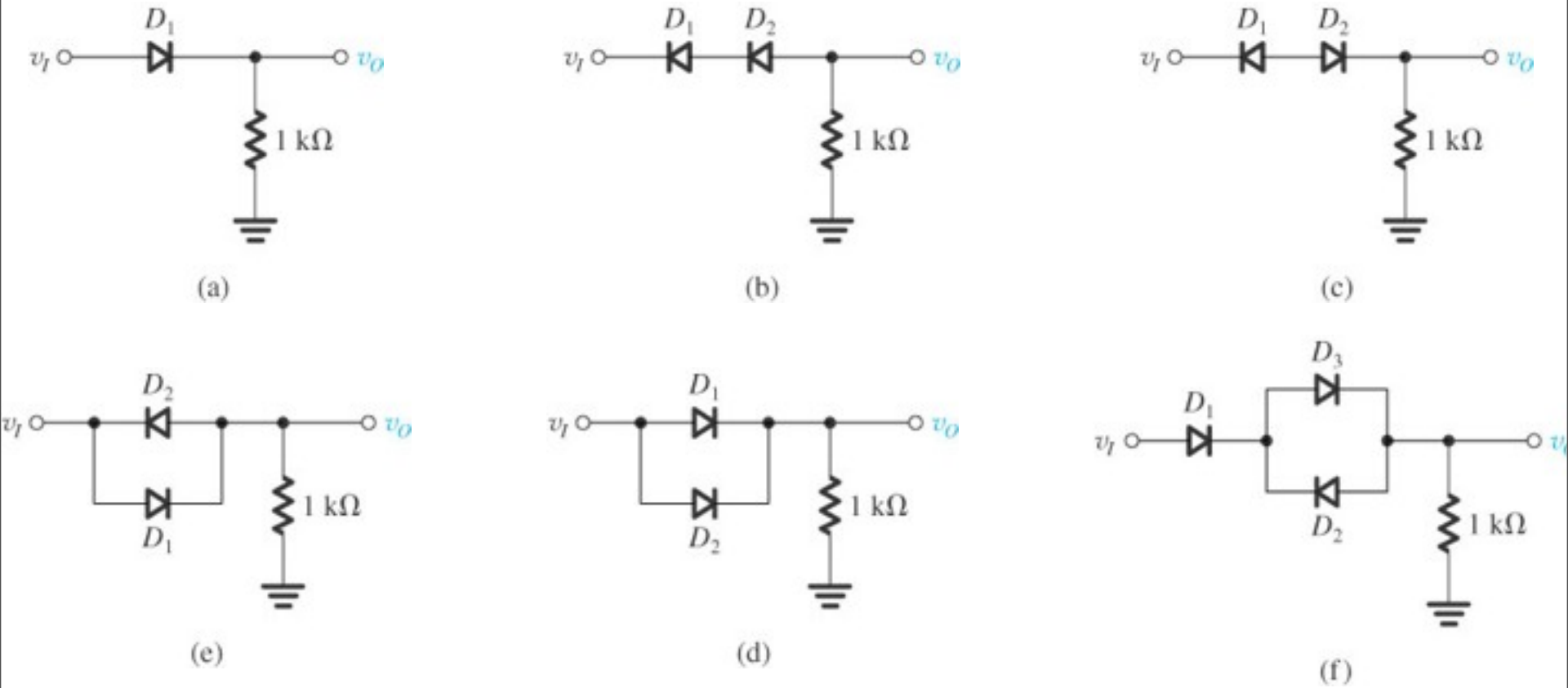
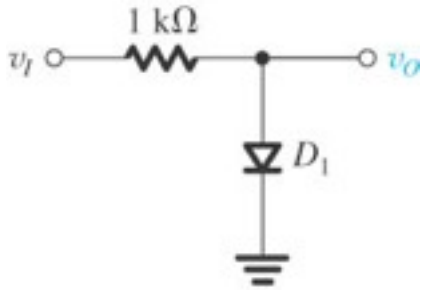


Figure P3.4 *(Continued)*



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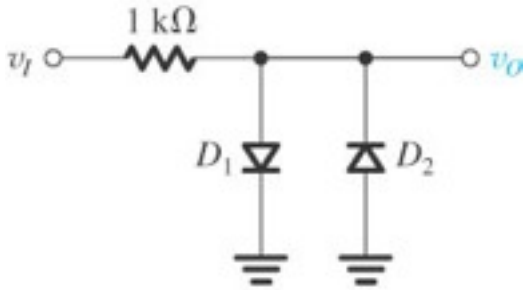

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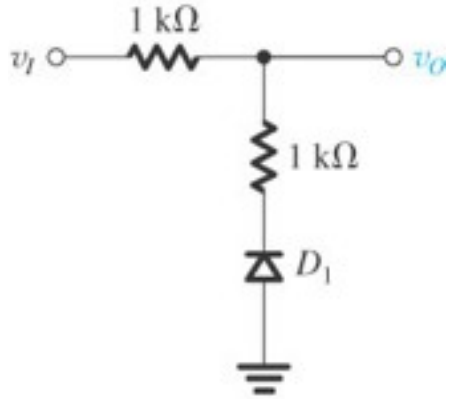

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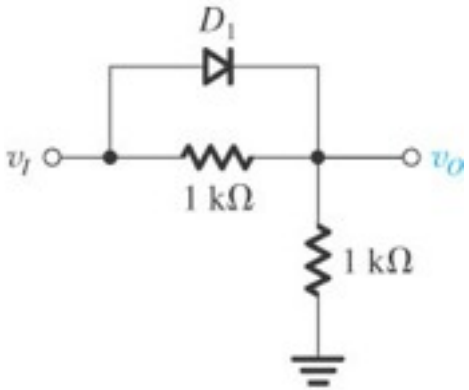

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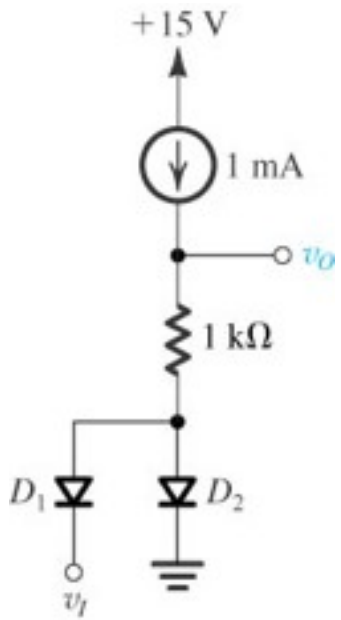

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Figure P3.4 *(Continued)*

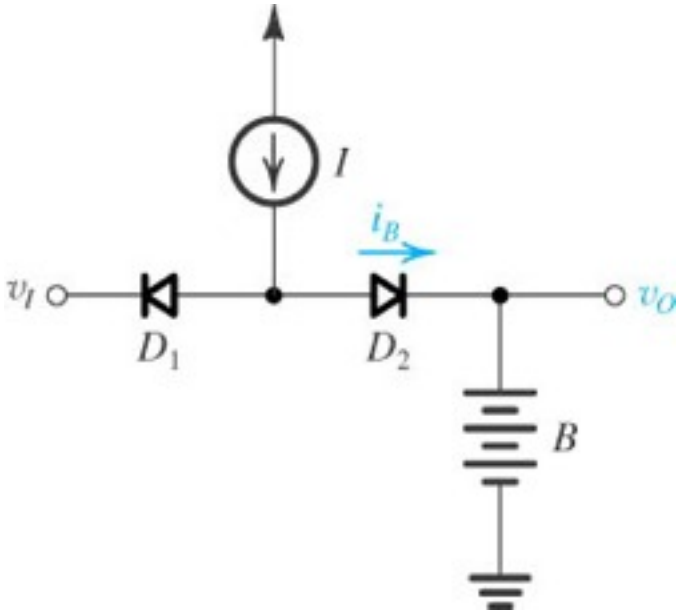
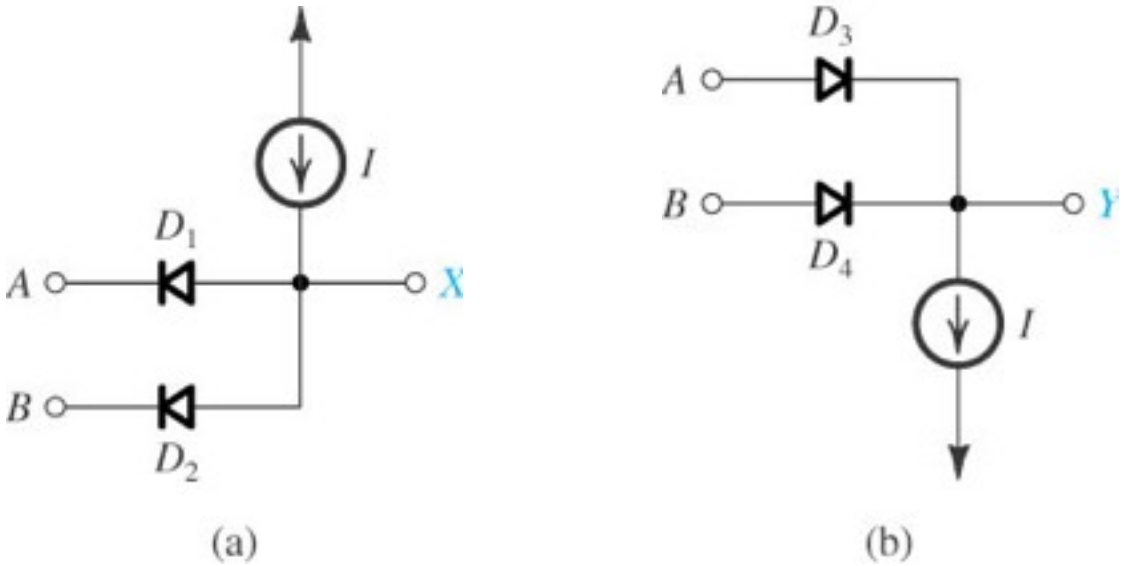


Figure P3.5



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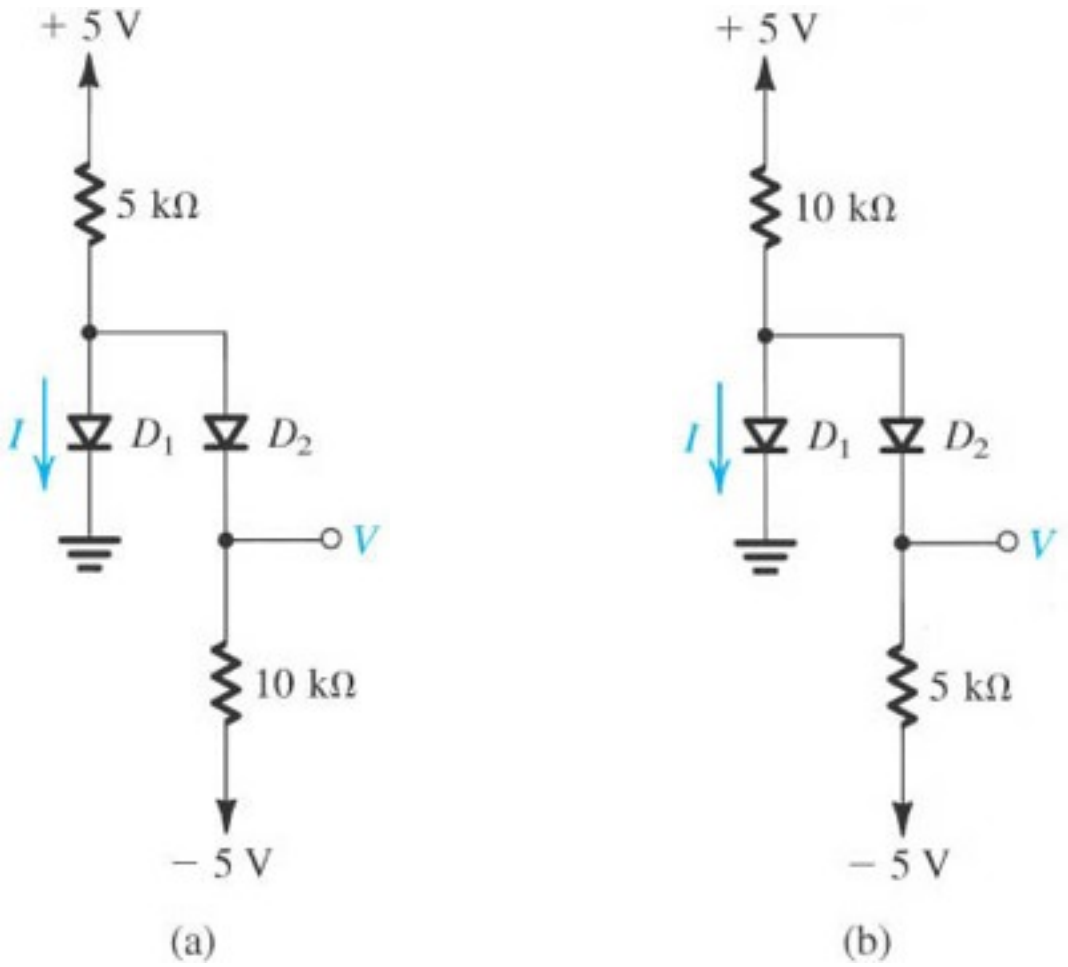
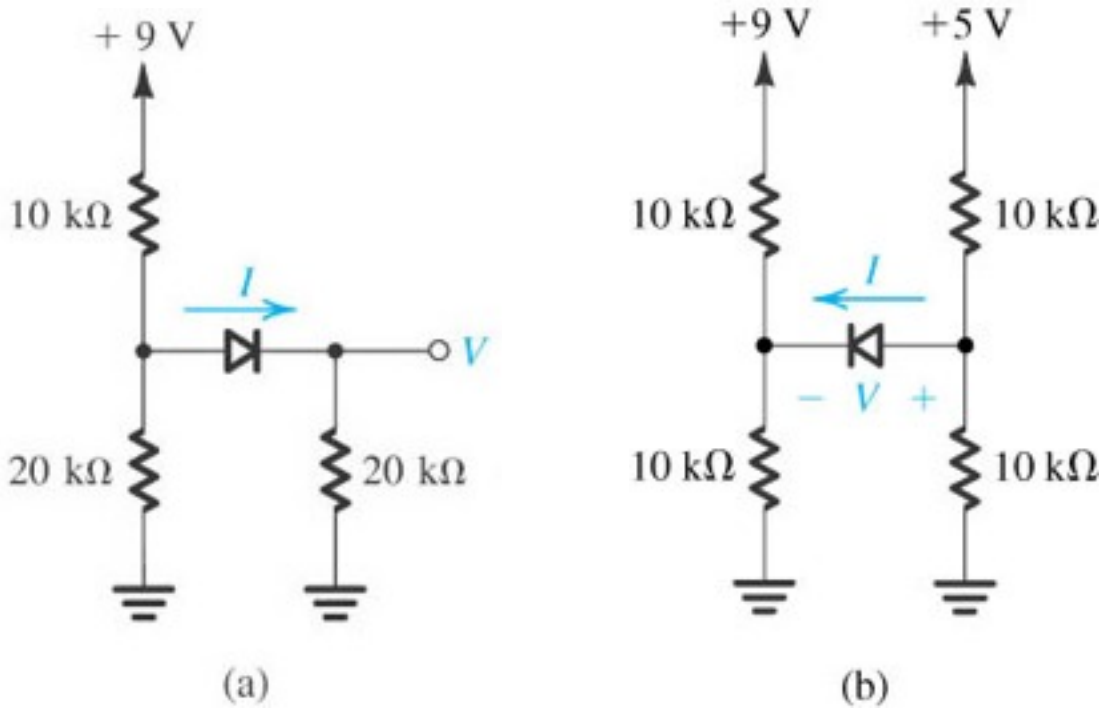


Figure P3.9



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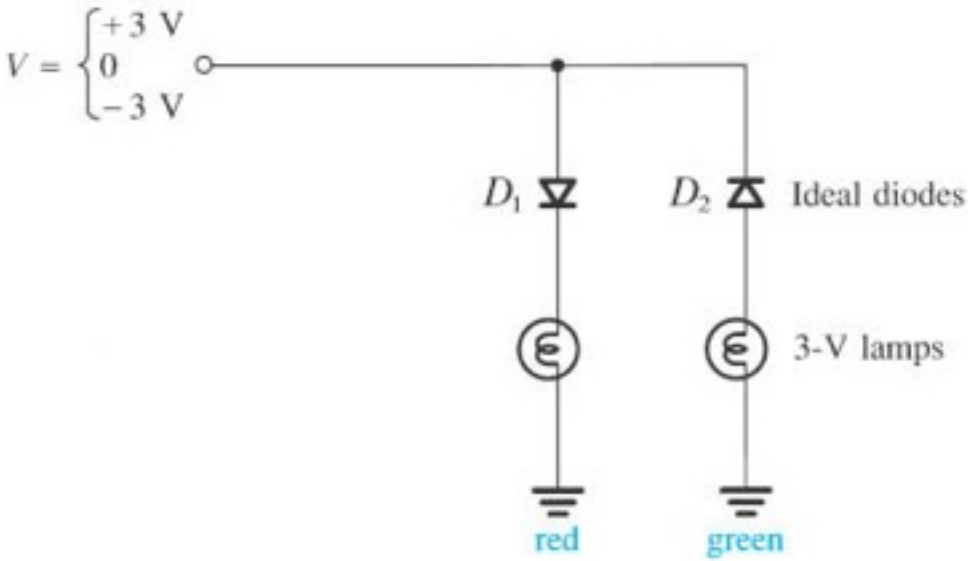
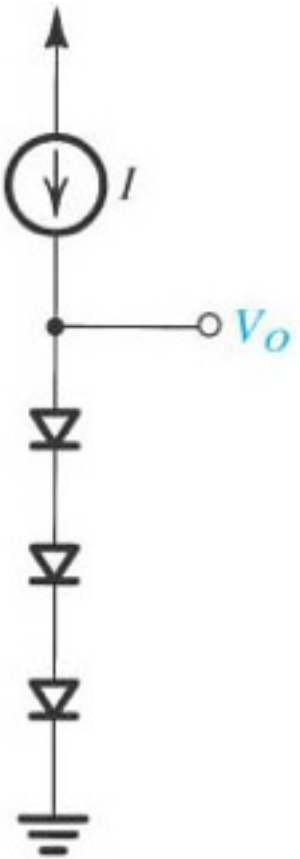


Figure P3.16



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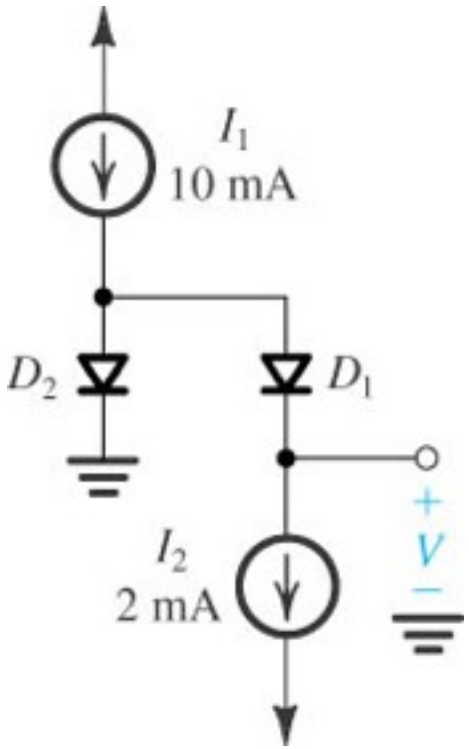

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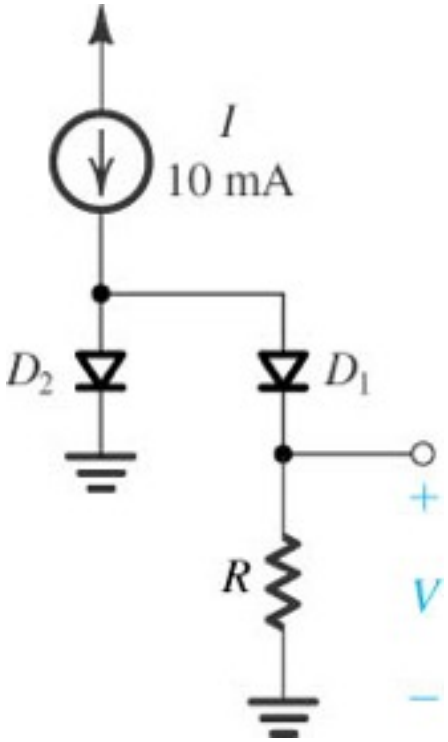

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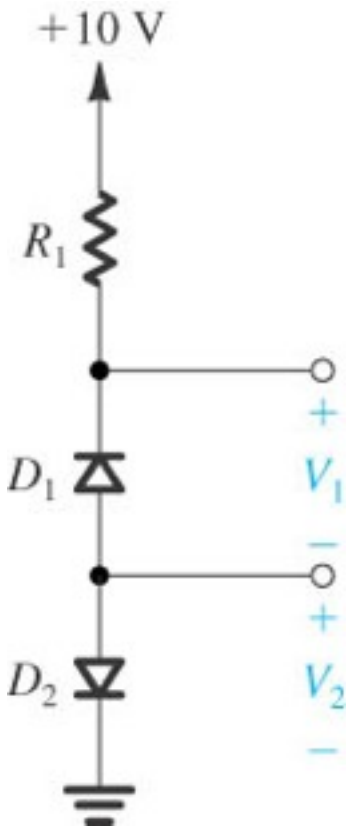

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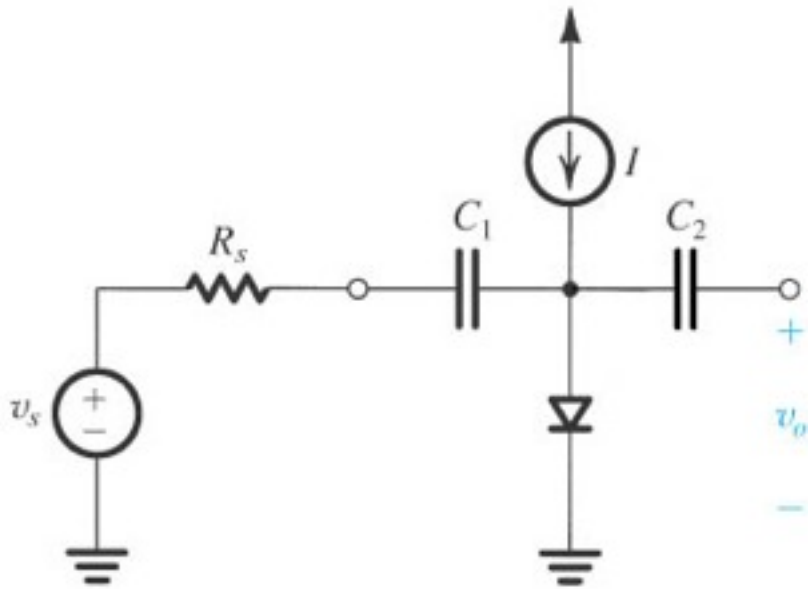

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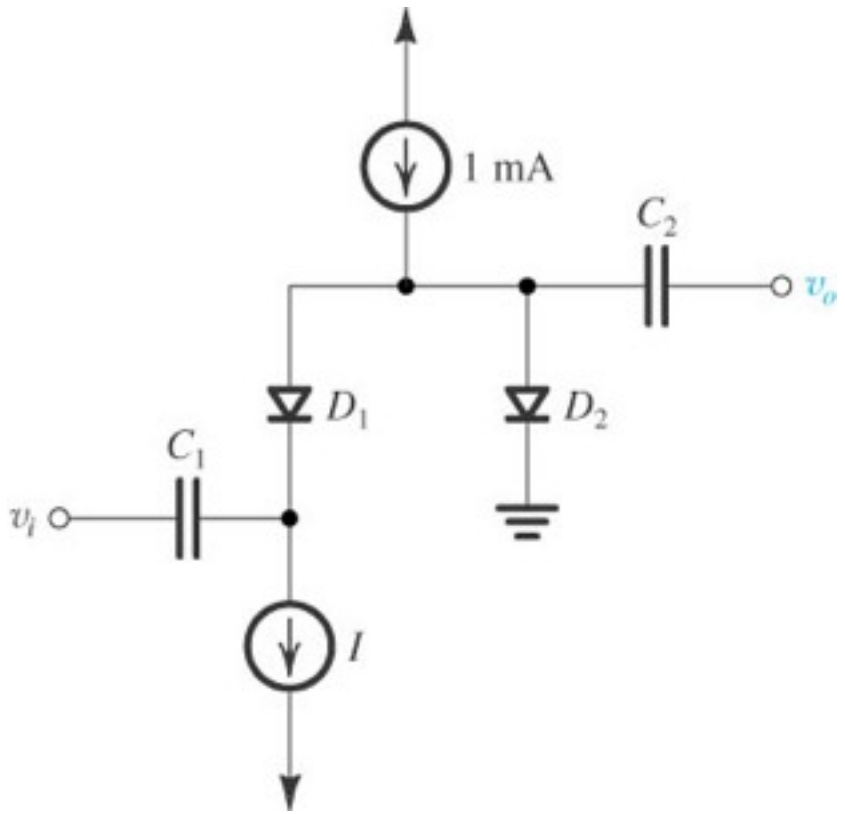

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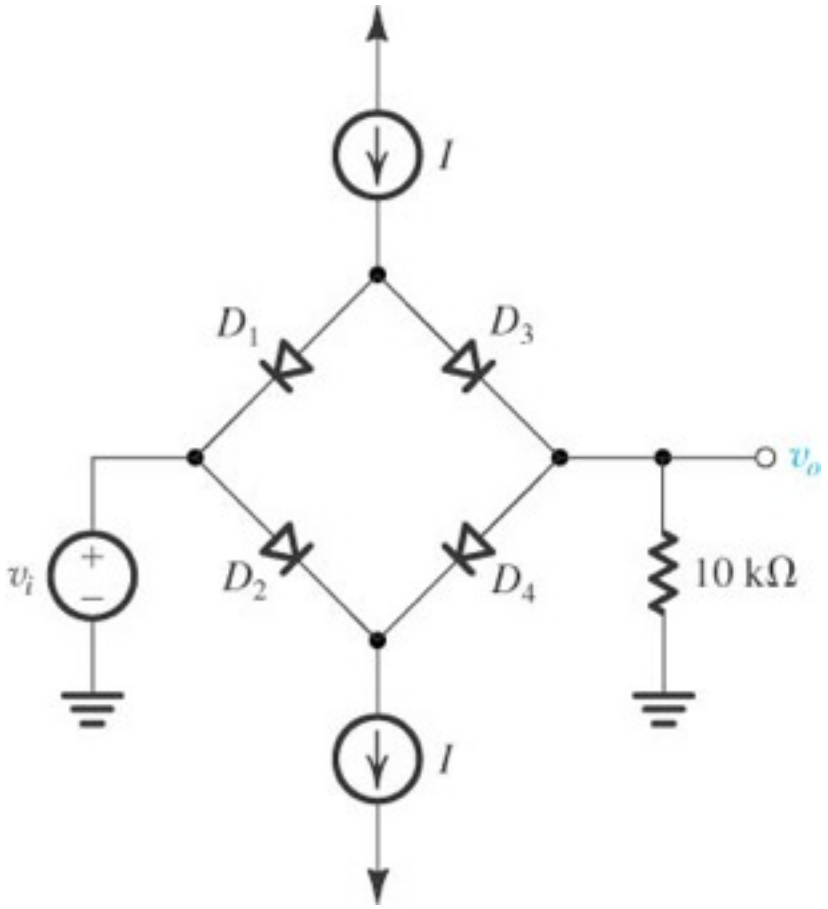

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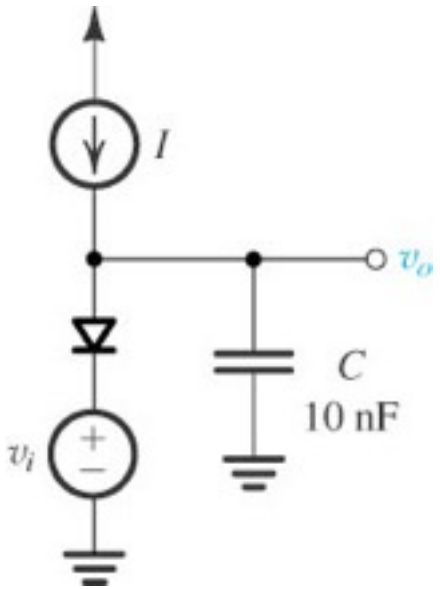

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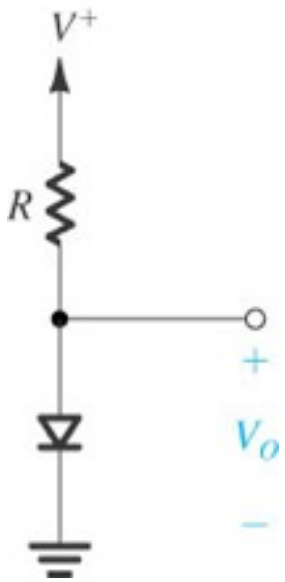

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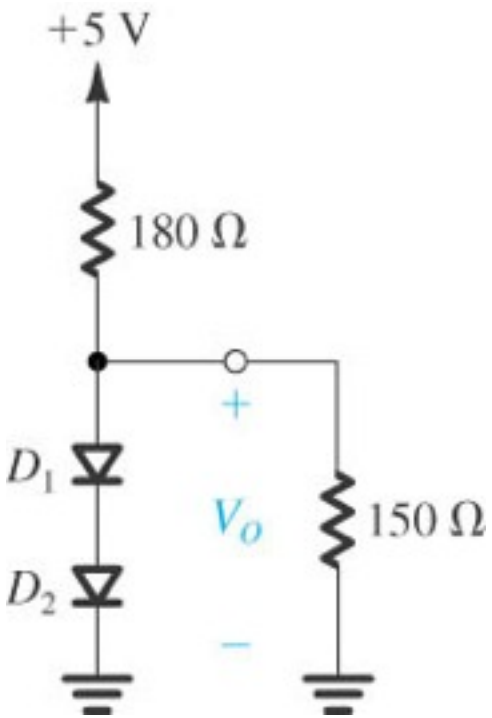

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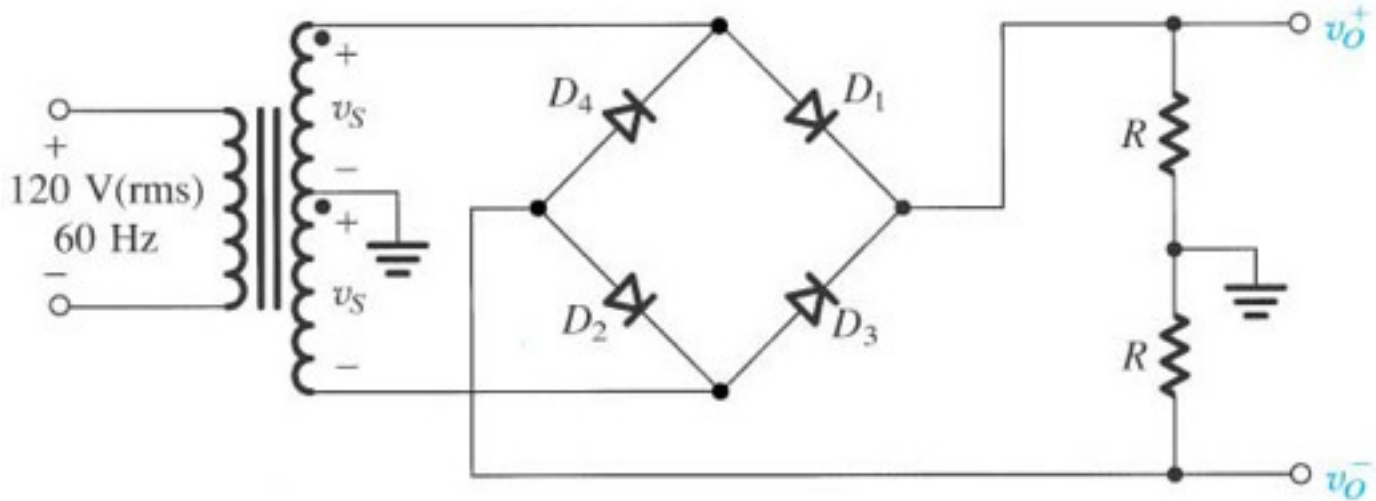

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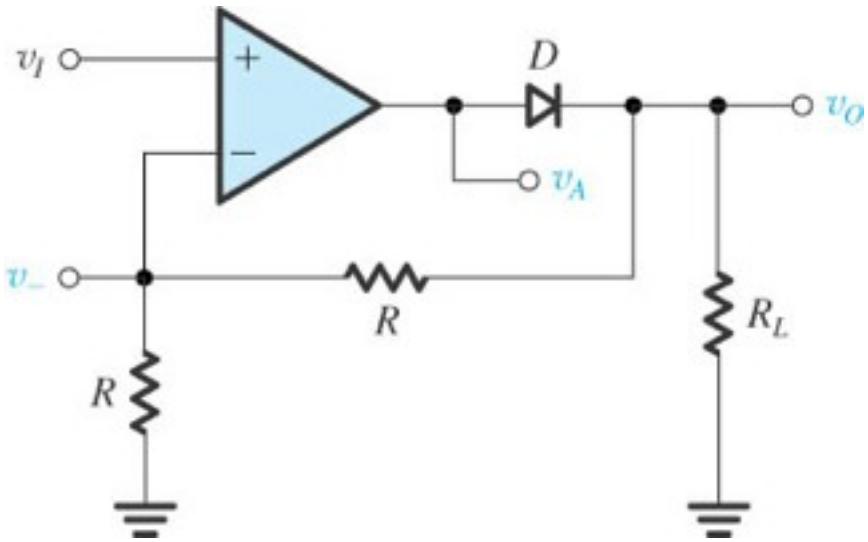

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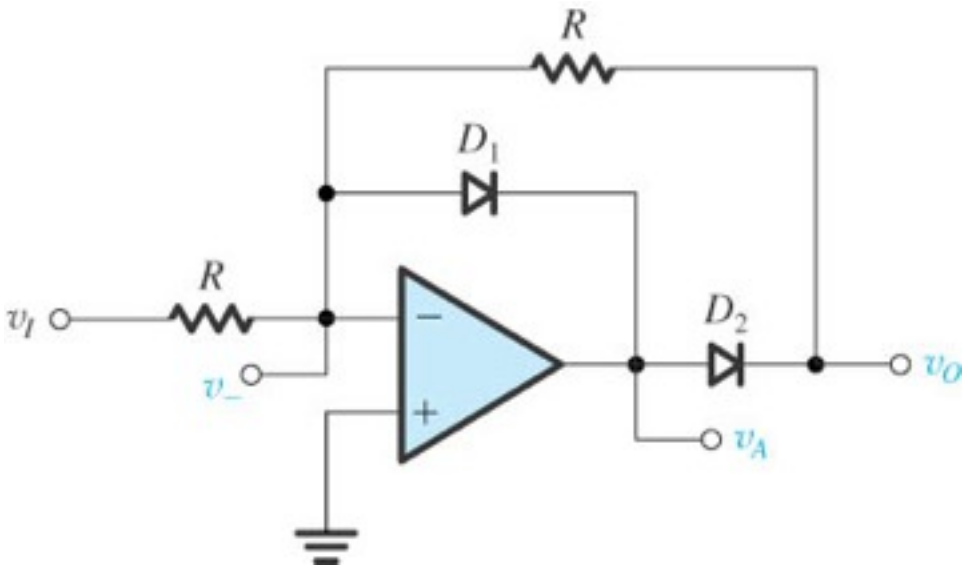

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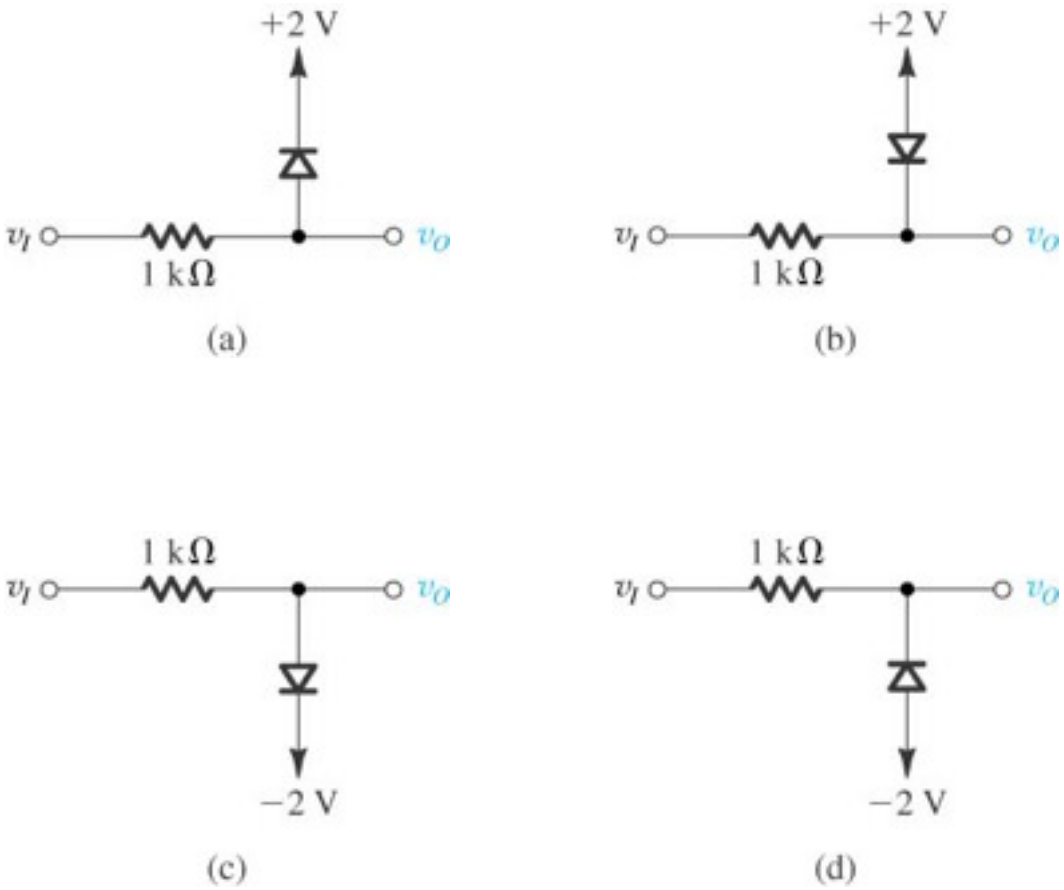

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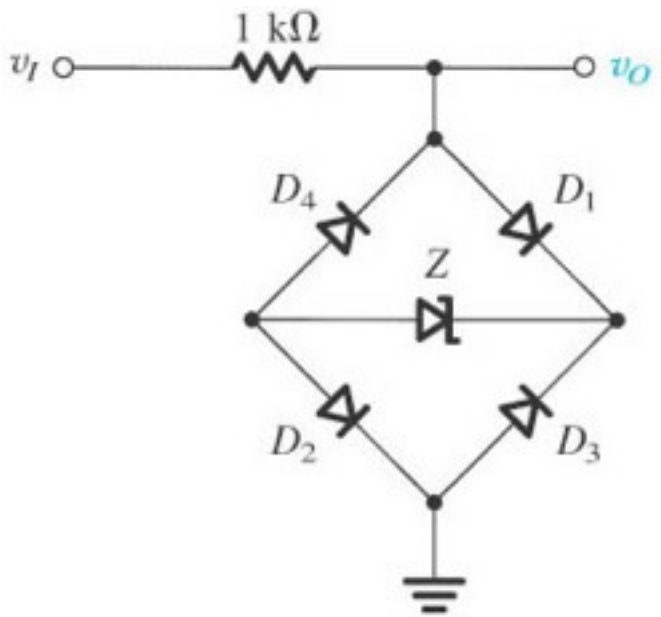

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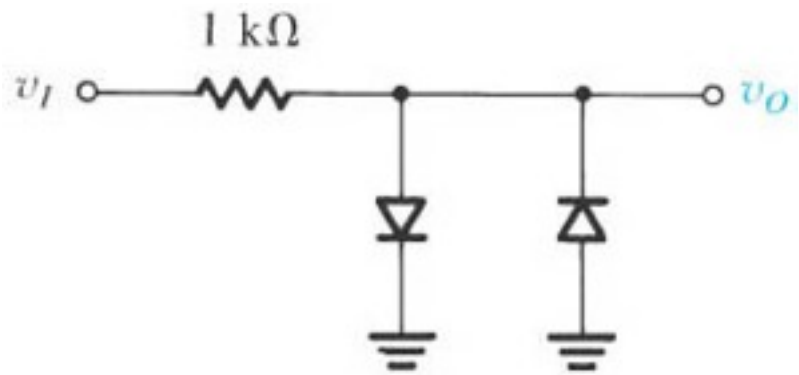

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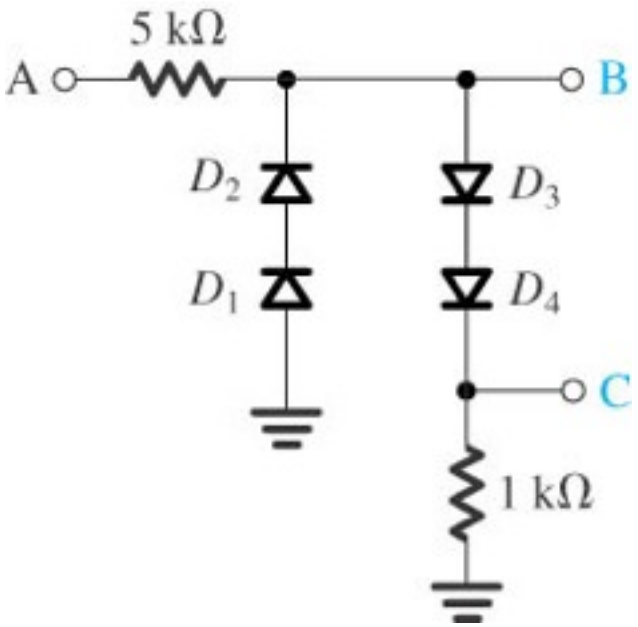

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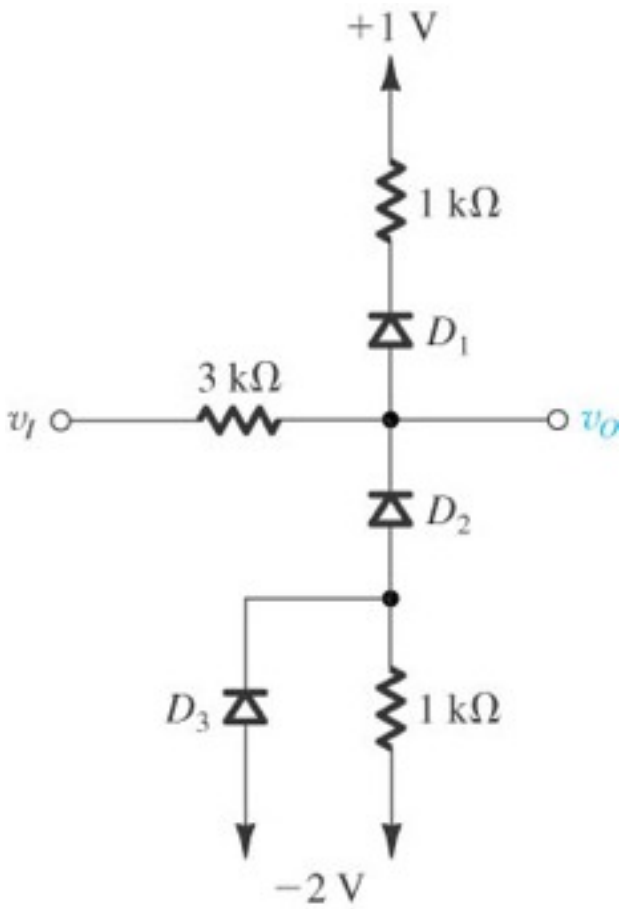

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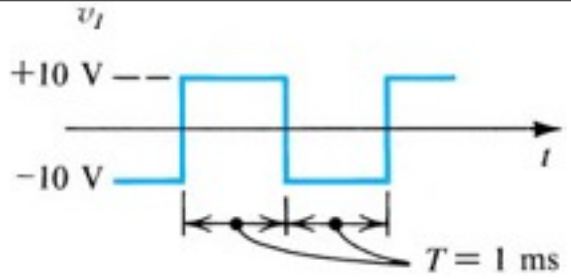

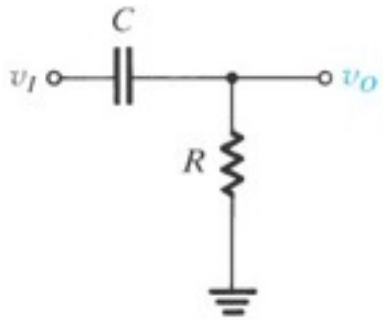

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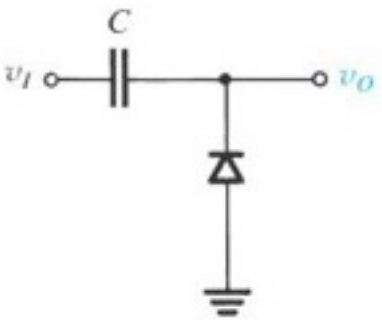

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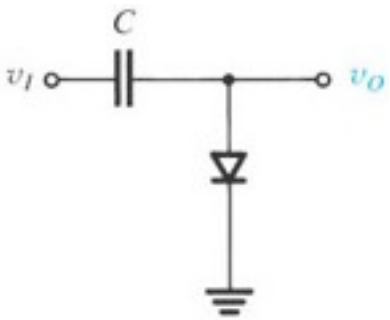

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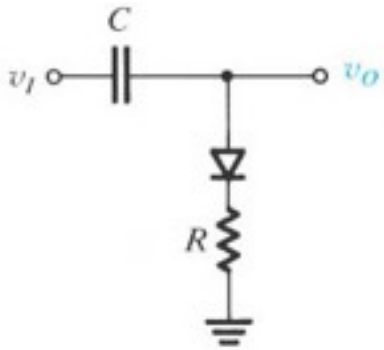

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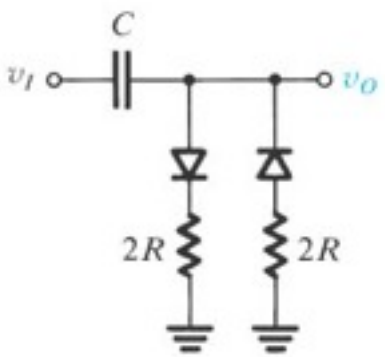

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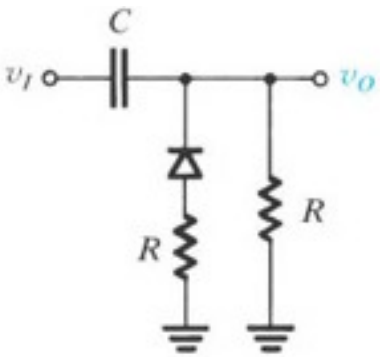

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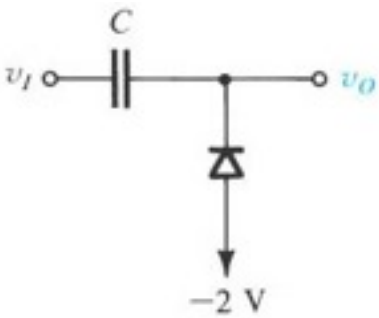

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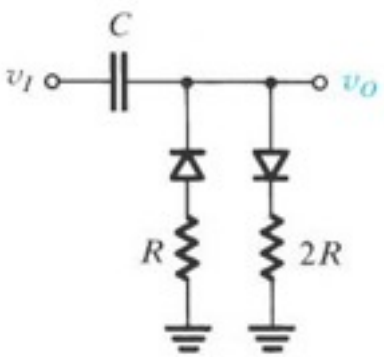

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Figure P3.105

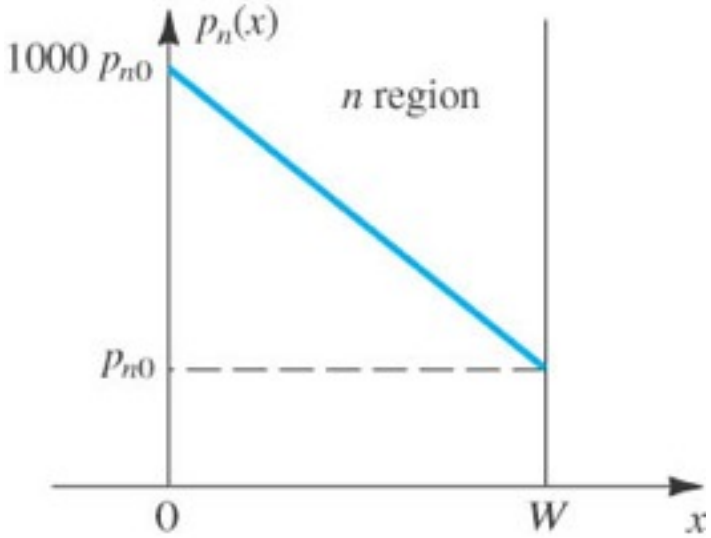

Figure P3.108