Laboratorio Avanzato di Elettronica
A.A. 2011/12

MOS Field-Effect Transistors (MOSFETs)

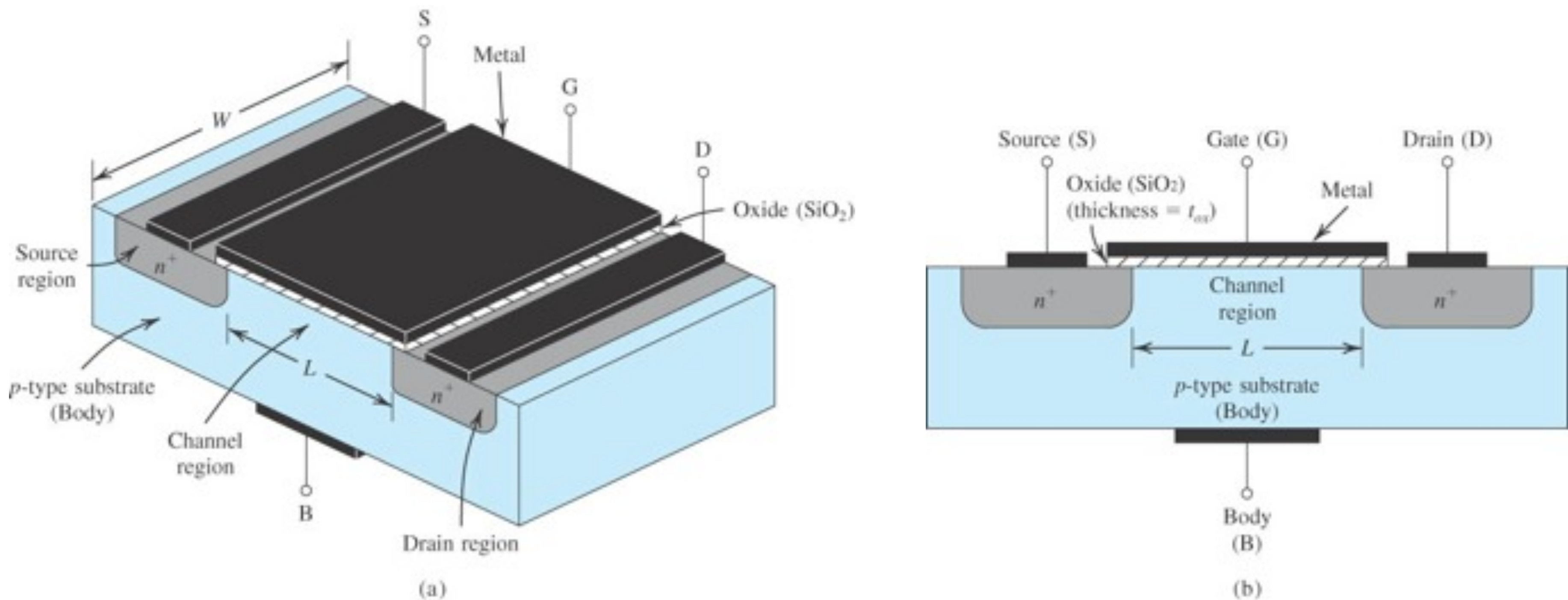

Figure 4.1 Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross-section. Typically L = 0.1 to 3 μm, W = 0.2 to 100 μm, and the thickness of the oxide layer (t_{ox}) is in the range of 2 to 50 nm.

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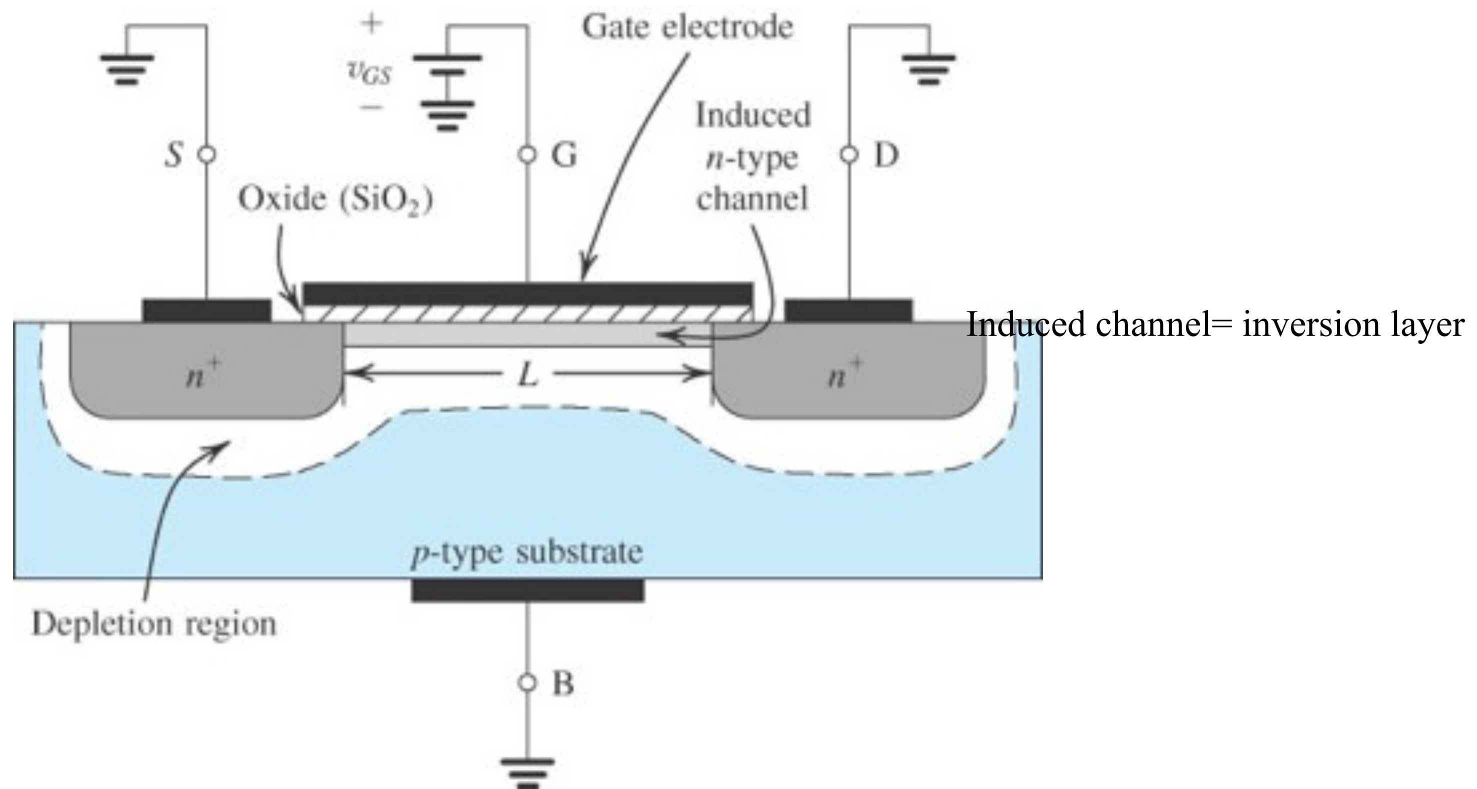
La v_{GS} che forma il canale di conduzione e' chiamata tensione di soglia v_t, compresa tra 0.5 ed 1 V



Il gate ed il canale formano un condensatore, con l'ossido come dielettrico. Applicando una piccola tensione positiva sul gate si accumulano cariche positivee nel canale cariche negative, rendendo la regione conduttiva.

Figure 4.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

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Come funziona il MOS con piccola V_{DS}

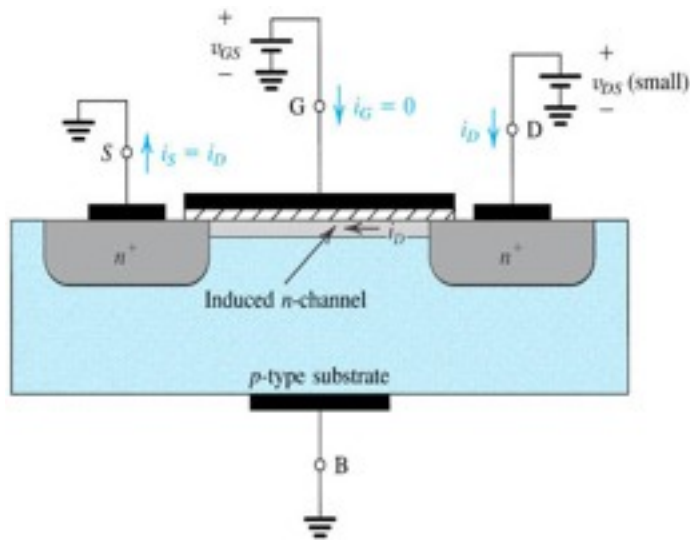

Figure 4.3 An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and thus i_D is proportional to $(v_{GS} - V_t)\, v_{DS}$. Note that the depletion region is not shown (for simplicity).

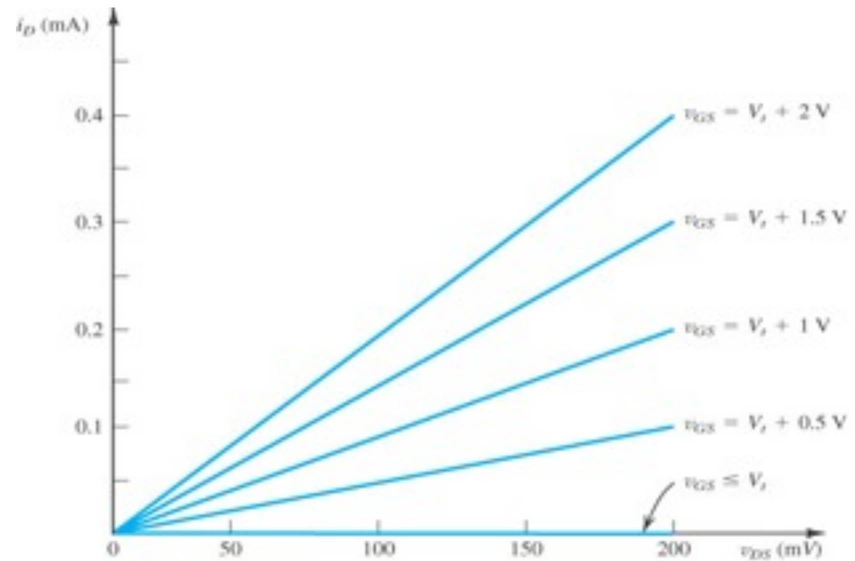

Figure 4.4 The i_D–v_{DS} characteristics of the MOSFET in Fig. 4.3 when the voltage applied between drain and source, v_{DS}, is kept small. The device operates as a linear resistor whose value is controlled by v_{GS}.

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Al crescere di V_{DS}

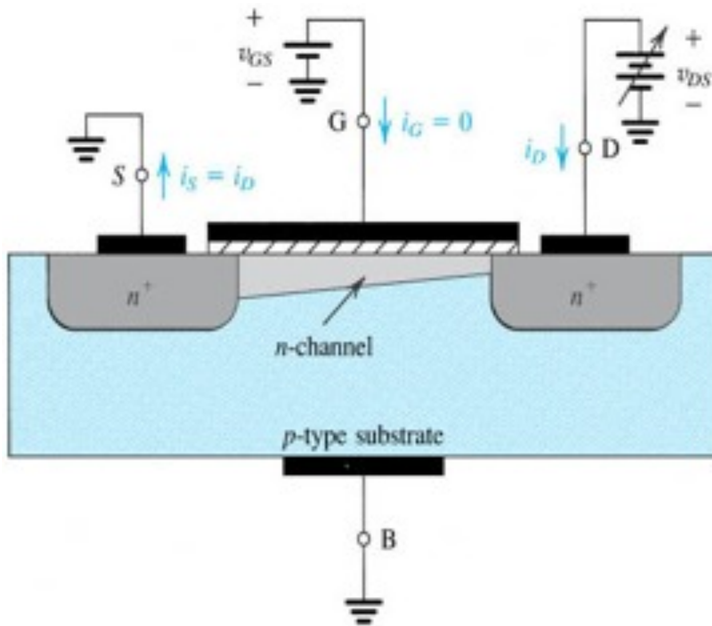

Figure 4.5 Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value $> V_t$.

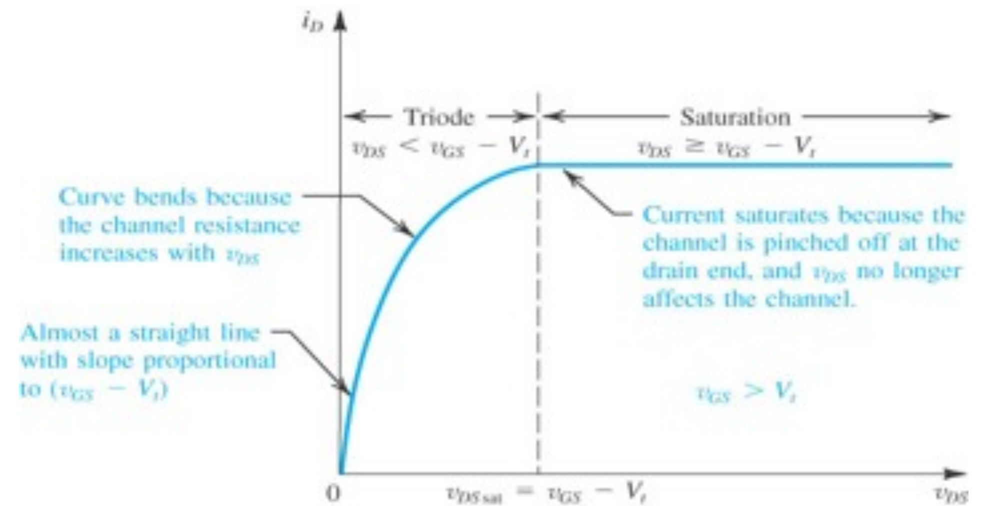

Figure 4.6 The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} > V_t$.

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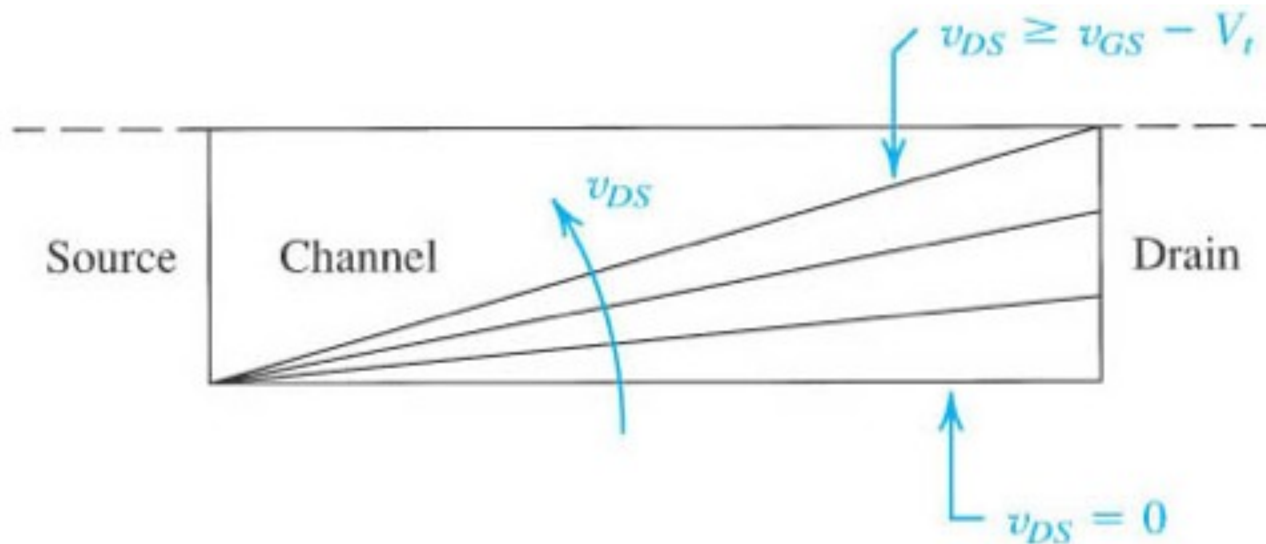

Figure 4.7 Increasing v_{DS} causes the channel to acquire a tapered shape. Eventually, as v_{DS} reaches $v_{GS} - V_t$, the channel is pinched off at the drain end. Increasing v_{DS} above $v_{GS} - V_t$ has little effect (theoretically, no effect) on the channel's shape.

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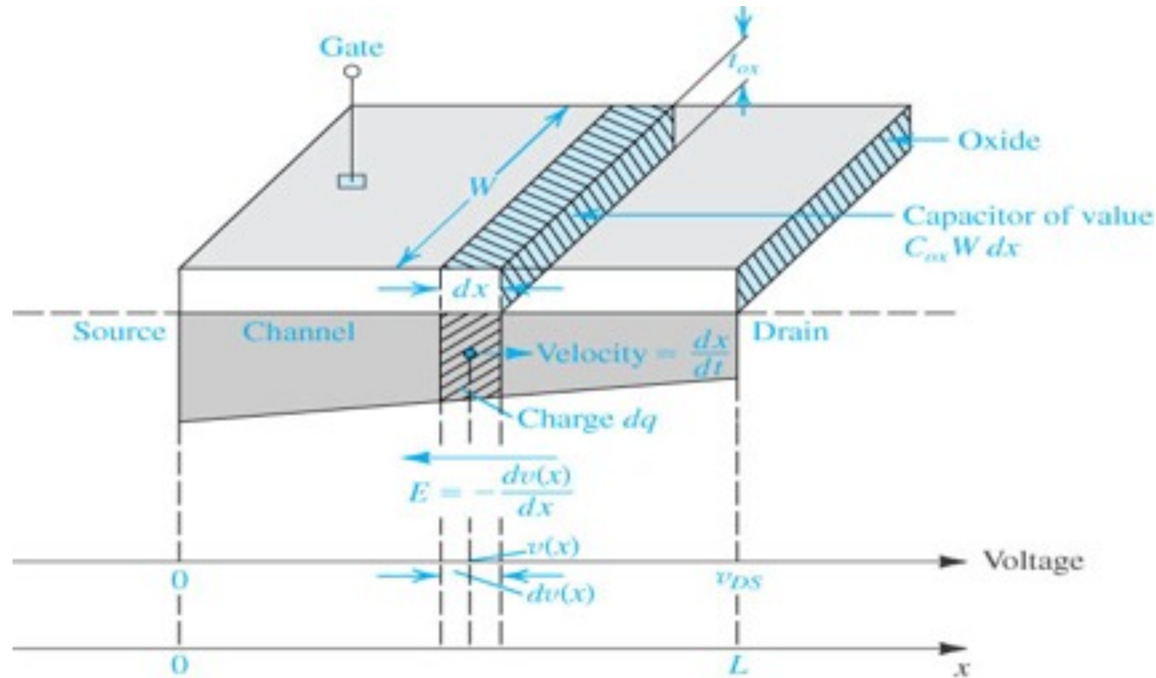
Relazione tra I_D e V_{DS}



$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}, \quad \text{con } \varepsilon_{ox} = 3.9\varepsilon_0 = 3.45 \times 10^{-11}\,\text{F/m}$$

carica elettronica in dx

$$dq = -C_{ox}(Wdx)[V_{GS} - v(x) - V_T]$$

Figure 4.8 Derivation of the i_D–v_{DS} characteristic of the NMOS transistor.

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La tensione v_{DS} produce un campo elettrico lungo il canale nella direzione negativa

$$E(x) = -\frac{dv(x)}{dx}$$

la carica dq drifta con velocita'

$$\frac{dx}{dt} = -\mu_n E(x) = \mu_n \frac{dv(x)}{dx}$$

corrente di drift

$$i = \frac{dq}{dt} = \frac{dq}{dx}\frac{dx}{dt}, \qquad i = -\mu_n C_{ox} W [v_{GS} - v(x) - V_t] \frac{dv(x)}{dx}$$

corrente di canale

$$i_D = -i = \mu_n C_{ox} W [v_{GS} - v(x) - V_t] \frac{dv(x)}{dx}$$

$$i_D dx = \mu_n C_{ox} W [v_{GS} - v(x) - V_t] dv(x)$$

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l'integrazione della relazione tra i limiti x=0 e x=L e conseguentemente per $v(0)=0$ e $v(L)= v_{DS}$ porta alla relazione base

Espressione per la i_D-v_{DS} nella **regione *triodo***

$$i_d = (\mu_n C_{ox})\left(\frac{W}{L}\right)[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2]$$

all'inizio della **regione *saturazione*** si ha $v_{DS} = v_{GS} - V_t$ e l'espressione diventa , a meno di un fattore 1/2

$$i_d = (\mu_n C_{ox})\left(\frac{W}{L}\right)[(v_{GS} - V_t)^2]$$

dove si vede che $\mathbf{i_d}$ rimane costante per un dato $\mathbf{v_{GS}}$

questo significa che per ogni valore di v_{GS} ci sara'una curva caratteristica ed un valore di corrente di saturazione

$k_n^{'} = (\mu_n C_{ox})$ e' un parametro che dipende dalla tecnologia usata per fabbricare il *n*-channel, e' chiamato *process transconductance parameter* **e si misura in A/V^2**

i valori in gioco sono approssimativamente per un MOSFET

per Cox circa decina di fF/um^2

per u_n circa centinaia di uA/V2

con W/L circa 10 per un canale di 0.8 um

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Complementary MOS o CMOS

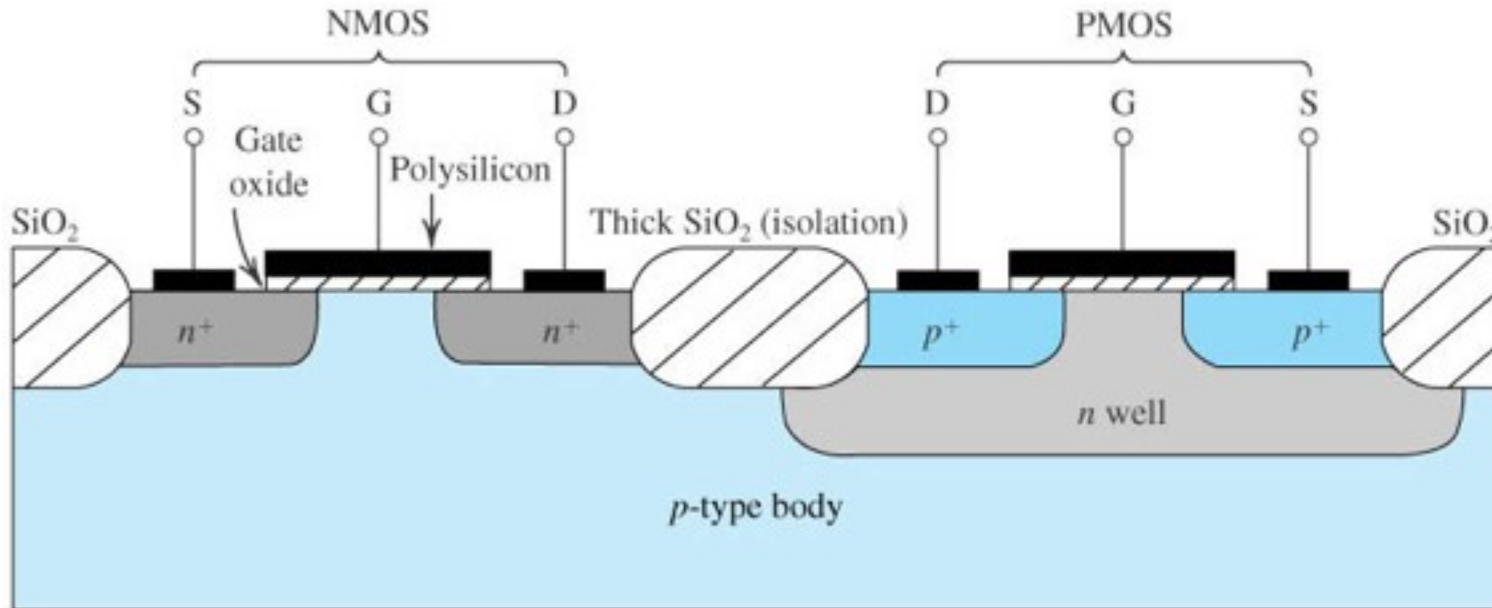

Figure 4.9 Cross-section of a CMOS integrated circuit. Note that the PMOS transistor is formed in a separate *n*-type region, known as an *n* well. Another arrangement is also possible in which an *n*-type body is used and the *n* device is formed in a *p* well. Not shown are the connections made to the *p*-type body and to the *n* well; the latter functions as the body terminal for the *p*-channel device.

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Caratteristica i_D-v_{DS} per un n-channel MOS

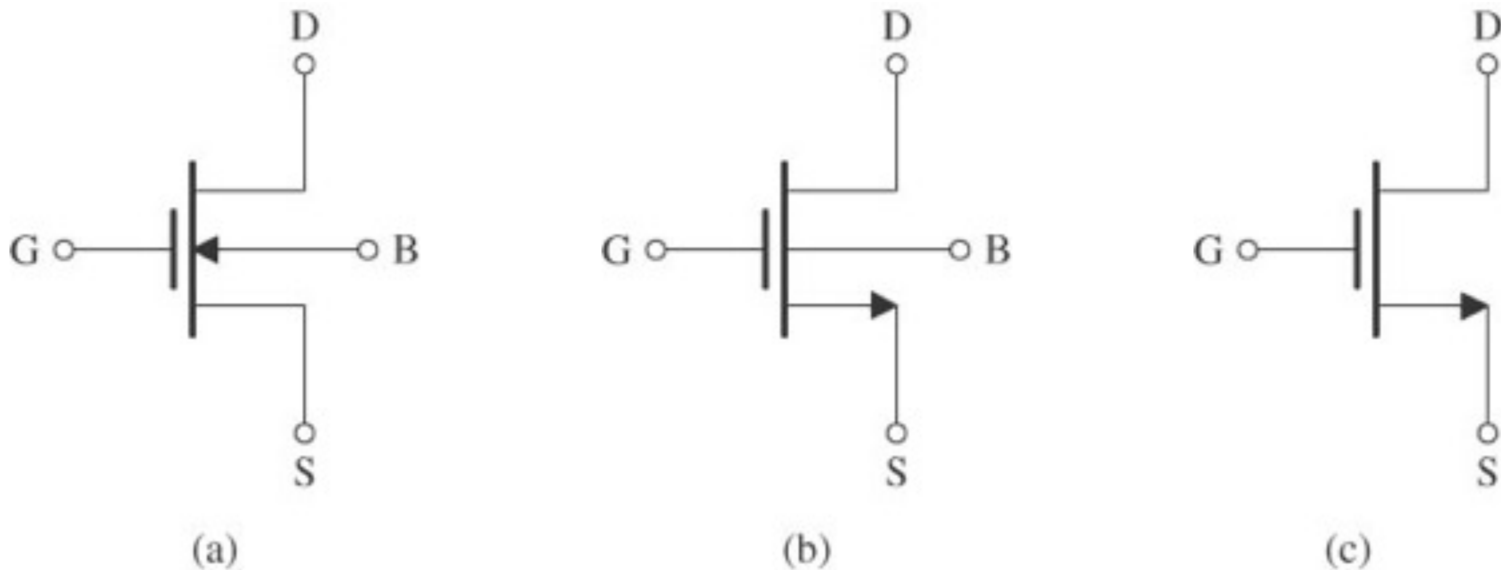

Figure 4.10 **(a)** Circuit symbol for the *n*-channel enhancement-type MOSFET. **(b)** Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., *n* channel). **(c)** Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

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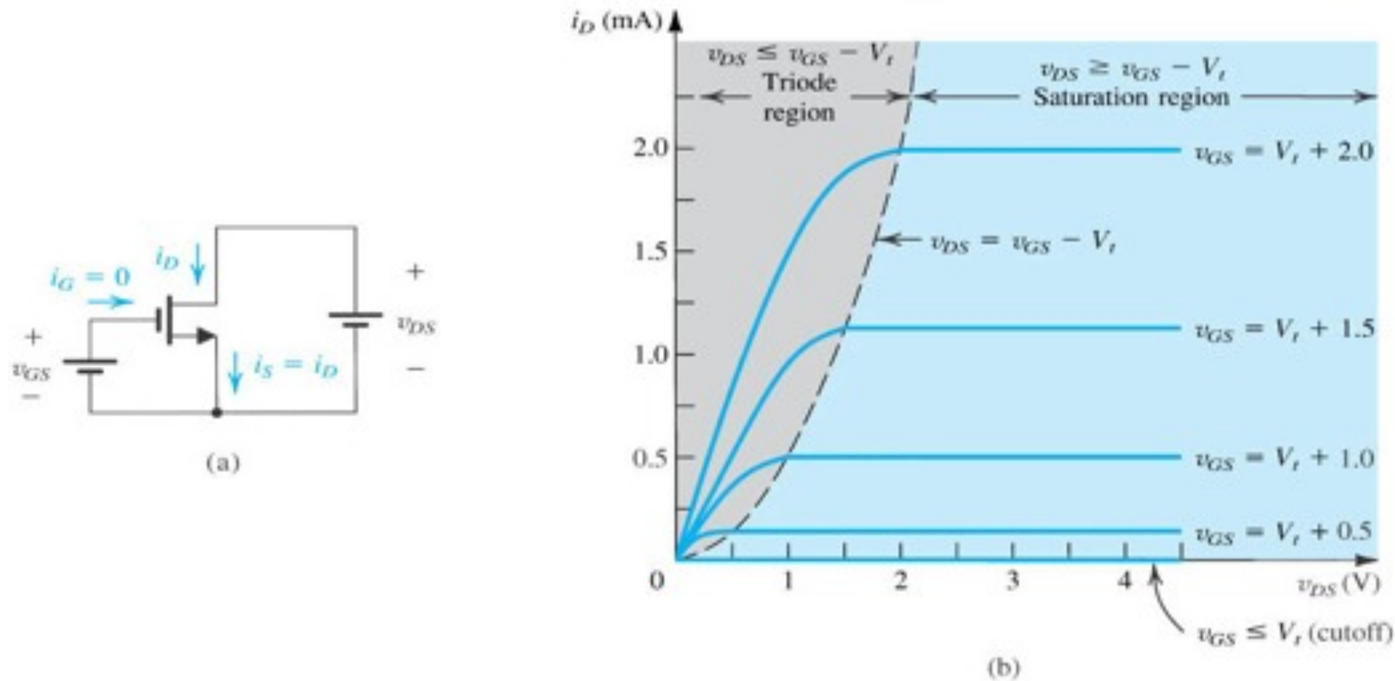

Figure 4.11 **(a)** An *n*-channel enhancement-type MOSFET with v_{GS} and v_{DS} applied and with the normal directions of current flow indicated. **(b)** The i_D–v_{DS} characteristics for a device with $k'_n(W/L) = 1.0$ mA/V².

per v_{DS} piccola si trascura il contributo di v^2_{DS} e la relazione per la zona triodo diventa

$$i_D \cong k' \frac{W}{L}(v_{GS} - V_t)v_{DS}$$

Per v_{GS} fissato la relazione i_D-v_{DS} e' lineare: il MOS si comporta come una resistenza controllata da v_{GS}

e la resistenza r_{DS}

$$r_{DS} \equiv \frac{v_{DS}}{i_D}\Big|_{\substack{v_{DS}\,piccolo \\ v_{GS} = V_{GS}}} = [k' \frac{W}{L}(v_{GS} - V_t)]^{-1}$$

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Per lavorare nella regione di saturazione il MOS deve indurre un canale V_{GS} >=Vt (canale indotto) e chiudere (pinch off) il canale sul DRAIN alzando V_{DS} tale che v_{GD}<=Vt (pinched off channel).

In sostanza si deve avere $$v_{DS} \geq v_{GS} - V_t$$

la regione tra triodo e saturazione e' caratterizzata da $$v_{DS} = v_{GS} - V_t$$

per cui sostituendo si ricava la relazione per la corrente di saturazione

$$i_D = \frac{1}{2} k' \frac{W}{L} (v_{GS} - V_t)^2$$

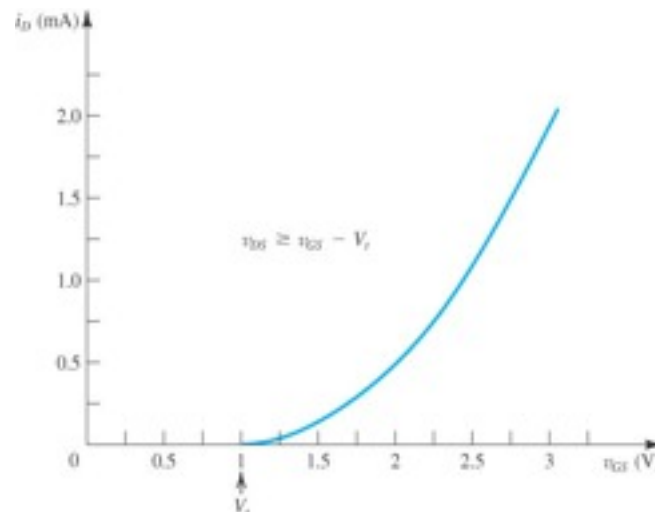

Figure 4.12 The i_D–v_{GS} characteristic for an enhancement-type NMOS transistor in saturation (V_t = 1 V, $k'_n W/L$ = 1.0 mA/V^2).

IL MOS si comporta come una sorgente ideale di corrente controllata da una V_{GS} , secondo una relazione quadratica.

Il comportamento e' quindi quello di un modello di circuito equivalente per **large signal**

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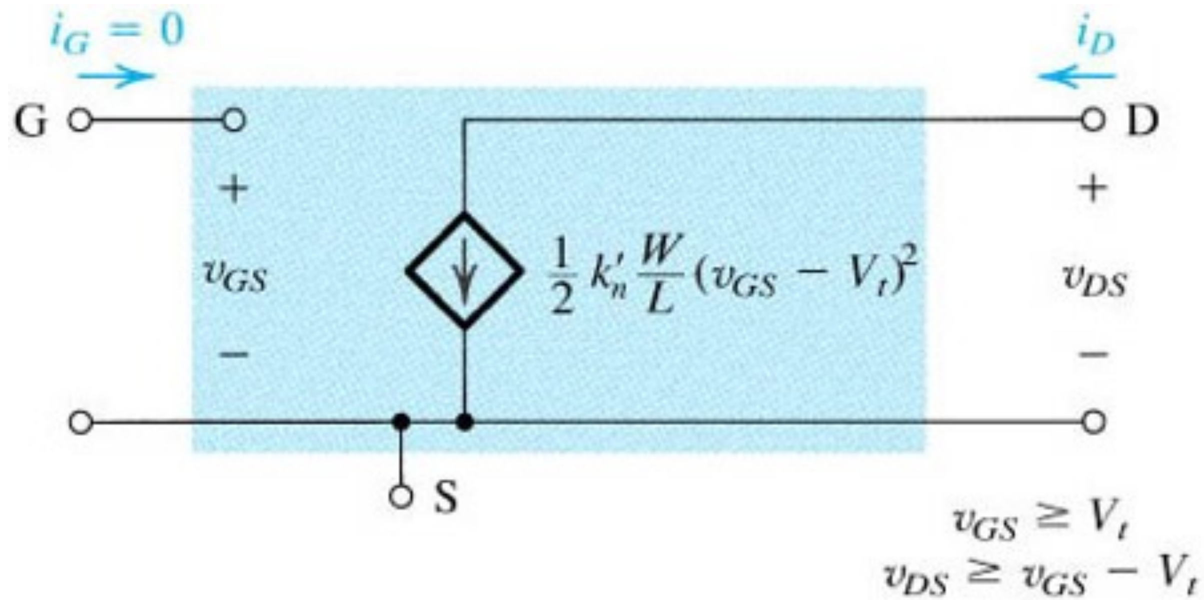

Figure 4.13 Large-signal equivalent-circuit model of an *n*-channel MOSFET operating in the saturation region.

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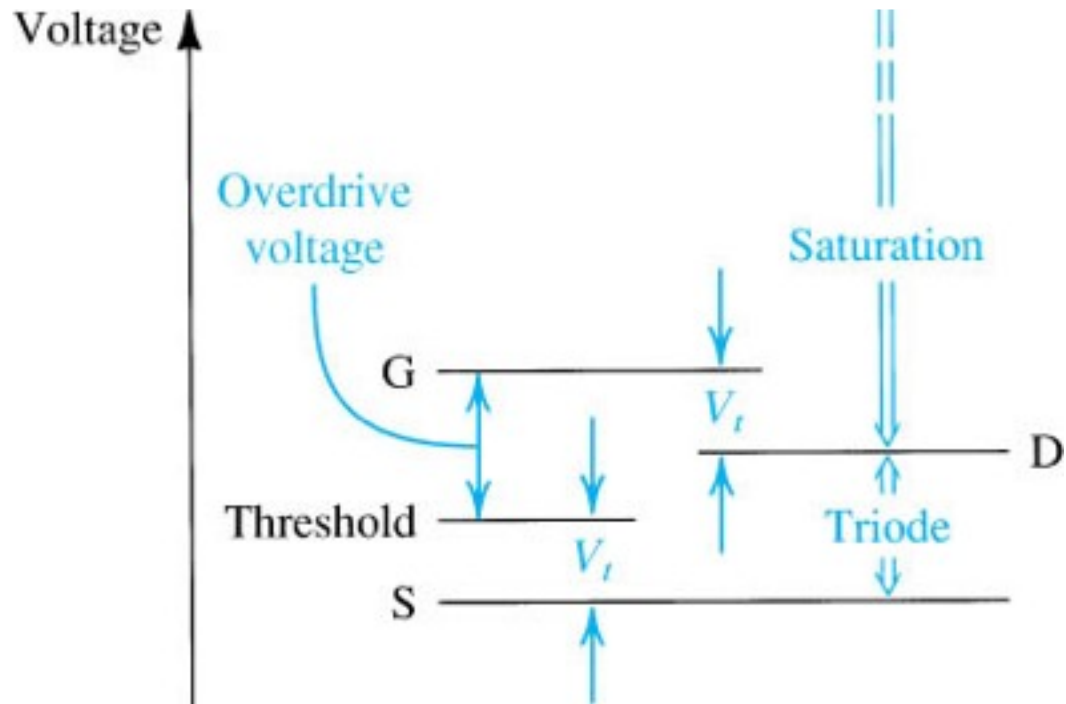

Figure 4.14 The relative levels of the terminal voltages of the enhancement NMOS transistor for operation in the triode region and in the saturation region.

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Resistenza finita di output in saturazione

In saturazione i_D e' indipendenta da v_{DS}, cosi' un cambiamento Δv_{DS} NON causa una variazione in i_D, che implica che la **resistenza incrementale**, vista al drain, di un MOS saturato e' infinita.

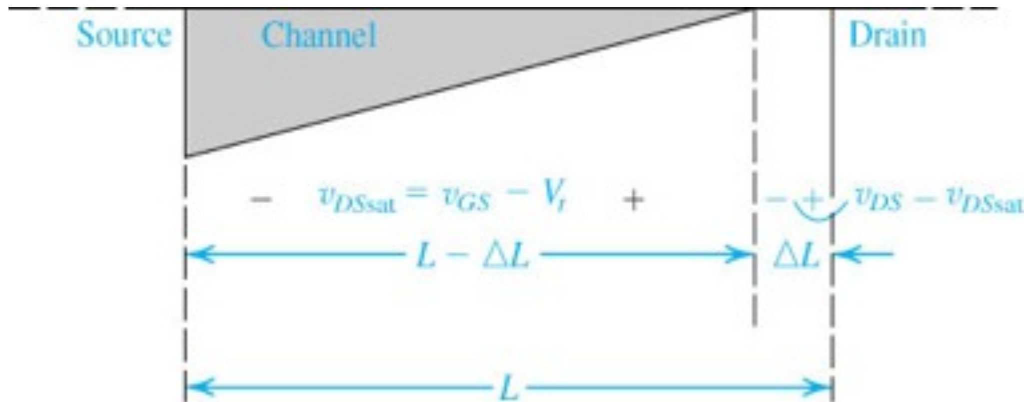

Figure 4.15 Increasing v_{DS} beyond v_{DSsat} causes the channel pinch-off point to move slightly away from the drain, thus reducing the effective channel length (by ΔL).

MA aumentando $v_{DS} > v_{DSsat} = v_{GS} - V_t$ si restringe il canale e si ha un effetto di Channel modulation e poiche' la i_D dipende dalla lunghezza del canale, cio' fa si' che i_D cresca al crescere con v_{DS}.

$$i_D = \frac{1}{2} k_n' \frac{W}{L - \Delta l}(v_{GS} - V_t)^2 \cong \frac{1}{2} k_n' \frac{W}{L}\left(1 + \frac{\Delta L}{L}\right)(v_{GS} - V_t)^2 \quad \text{assumendo } \Delta L / L << 1$$

con $\Delta L = \lambda' v_{DS}$

$$i_D = \frac{1}{2} k_n' \frac{W}{L}\left(1 + \frac{\lambda'}{L} v_{DS}\right)(v_{GS} - V_t)^2$$

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Tenendo conto della variazione della lunghezza L del canale la relazione di i_D diventa

$$i_D = \frac{1}{2} k' \frac{W}{L} (v_{GS} - V_t)^2 (1 + \lambda v_{DS})$$

$$\lambda = \frac{\lambda'}{L}$$

parametro dipendente dalla tecnologia

$$V_A = \frac{1}{\lambda}$$

ha dimensioni di V

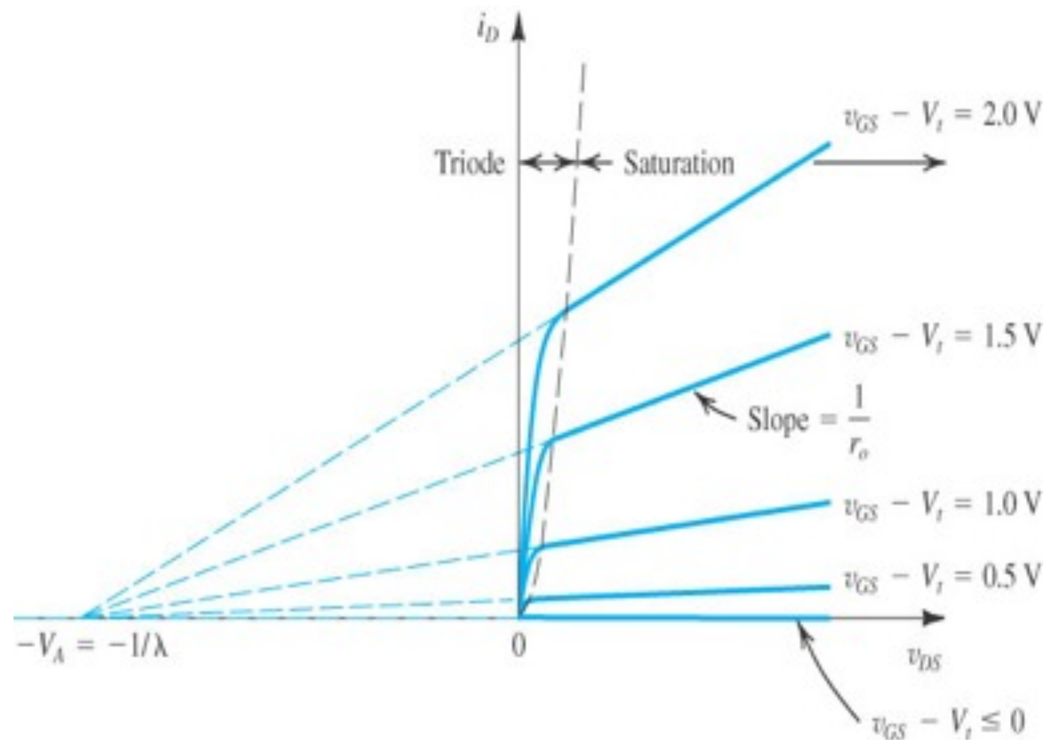

Figure 4.16 Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length L.

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ne segue che la resistenza di output della sorgente di corrente i_D
non e' piu' infinita.

$$r_0 \equiv \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1}_{v_{GS}} \qquad r_0 = \frac{V_A}{I_D} \qquad \text{con} \qquad I_D = \frac{1}{2}k_n' \frac{W}{L}(V_{GS} - V_t)^2$$

Output Resistance
inversamente proporzionale \corrente di drain

Corrente di drain senza modulazione

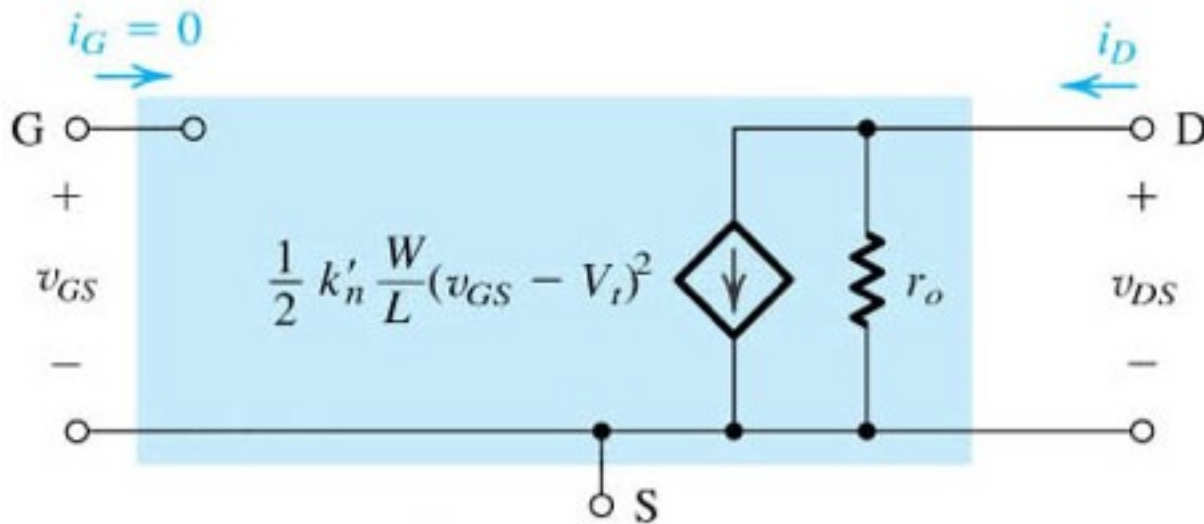

Figure 4.17 Large-signal equivalent circuit model of the *n*-channel MOSFET in saturation, incorporating the output resistance r_o. The output resistance models the linear dependence of i_D on v_{DS} and is given by Eq. (4.22).

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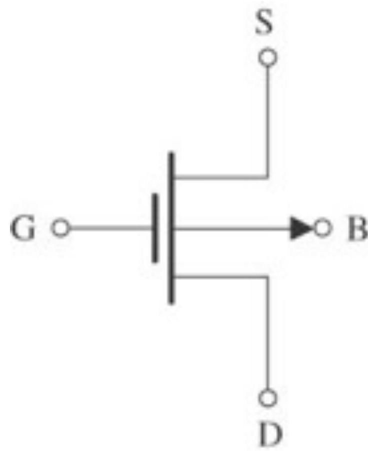
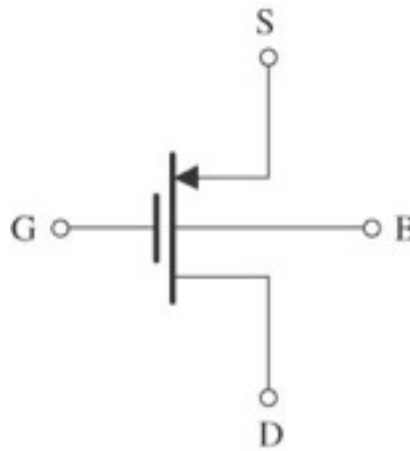
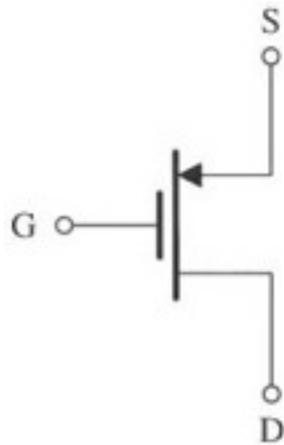
p-channel MOSFET





Valgono le stesse relazioni del n-channel MOS solo che , v_{GS}, V_t, e V_{DS} sono tutte negative



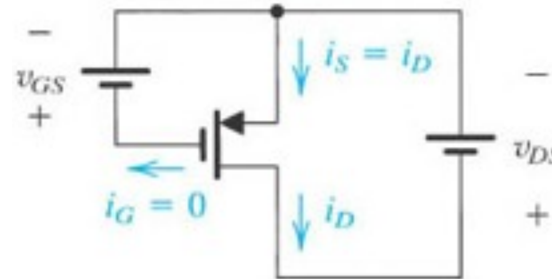


Figure 4.18 **(a)** Circuit symbol for the *p*-channel enhancement-type MOSFET. **(b)** Modified symbol with an arrowhead on the source lead. **(c)** Simplified circuit symbol for the case where the source is connected to the body. **(d)** The MOSFET with voltages applied and the directions of current flow indicated. Note that v_{GS} and v_{DS} are negative and i_D flows out of the drain terminal.

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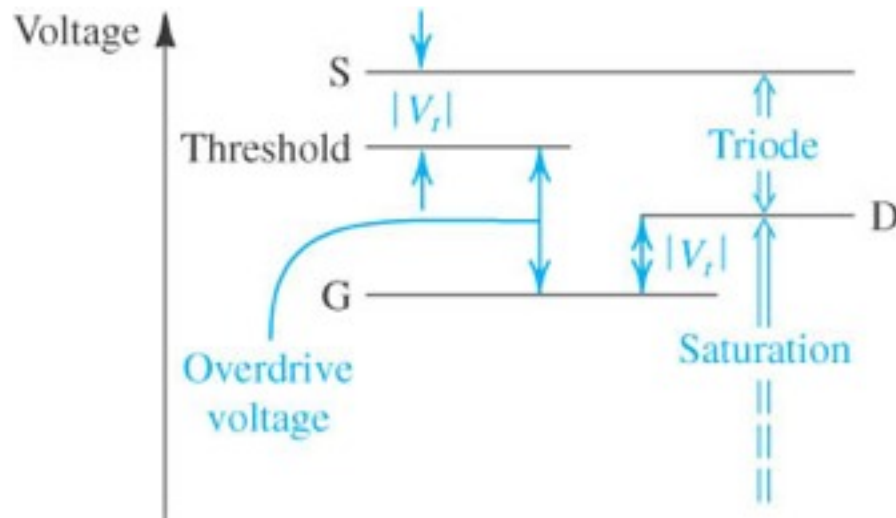

Figure 4.19 The relative levels of the terminal voltages of the enhancement-type PMOS transistor for operation in the triode region and in the saturation region.

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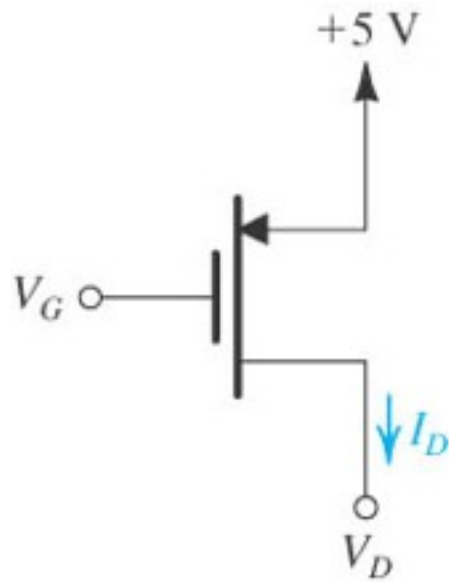

Figure E4.8

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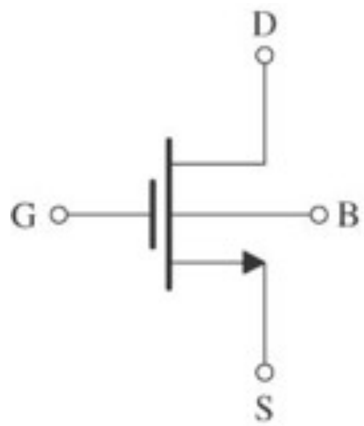

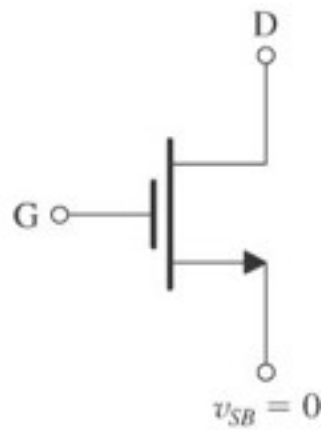

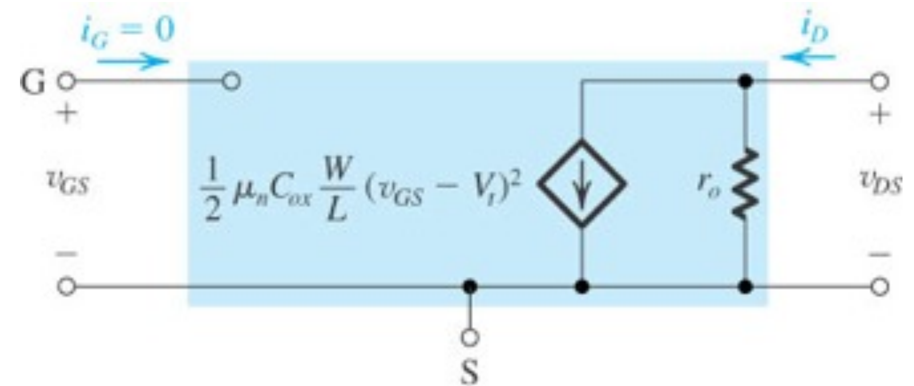

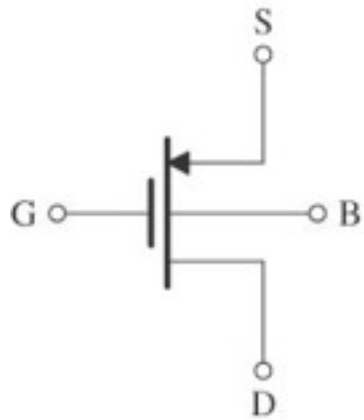

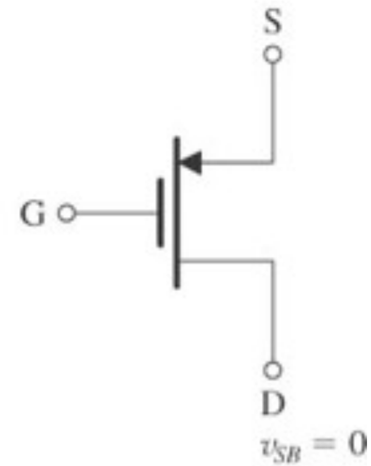

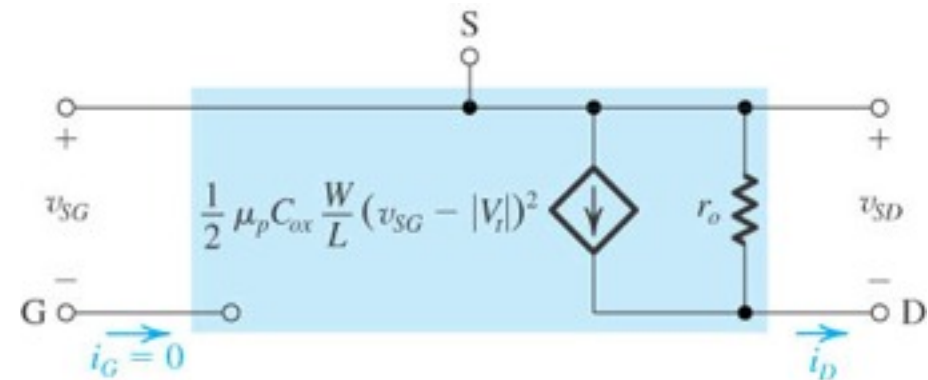

Table 4.1

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IL MOSFET come amplificatore e switch

$$v_o = v_{DS} = V_{DD} - R_D i_D$$

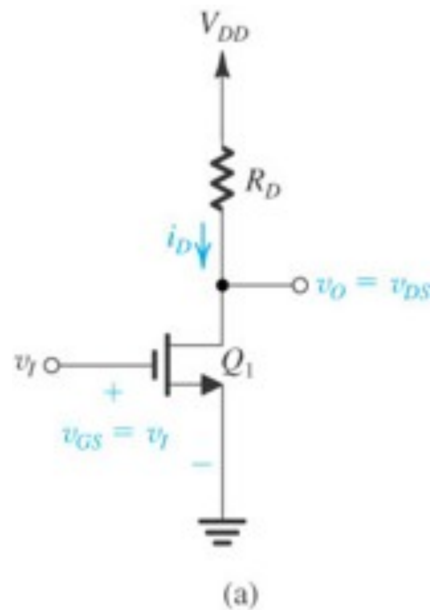

Figure 4.26 **(a)** Basic structure of the common-source amplifier. **(b)** Graphical construction to determine the transfer characteristic of the amplifier in (a).

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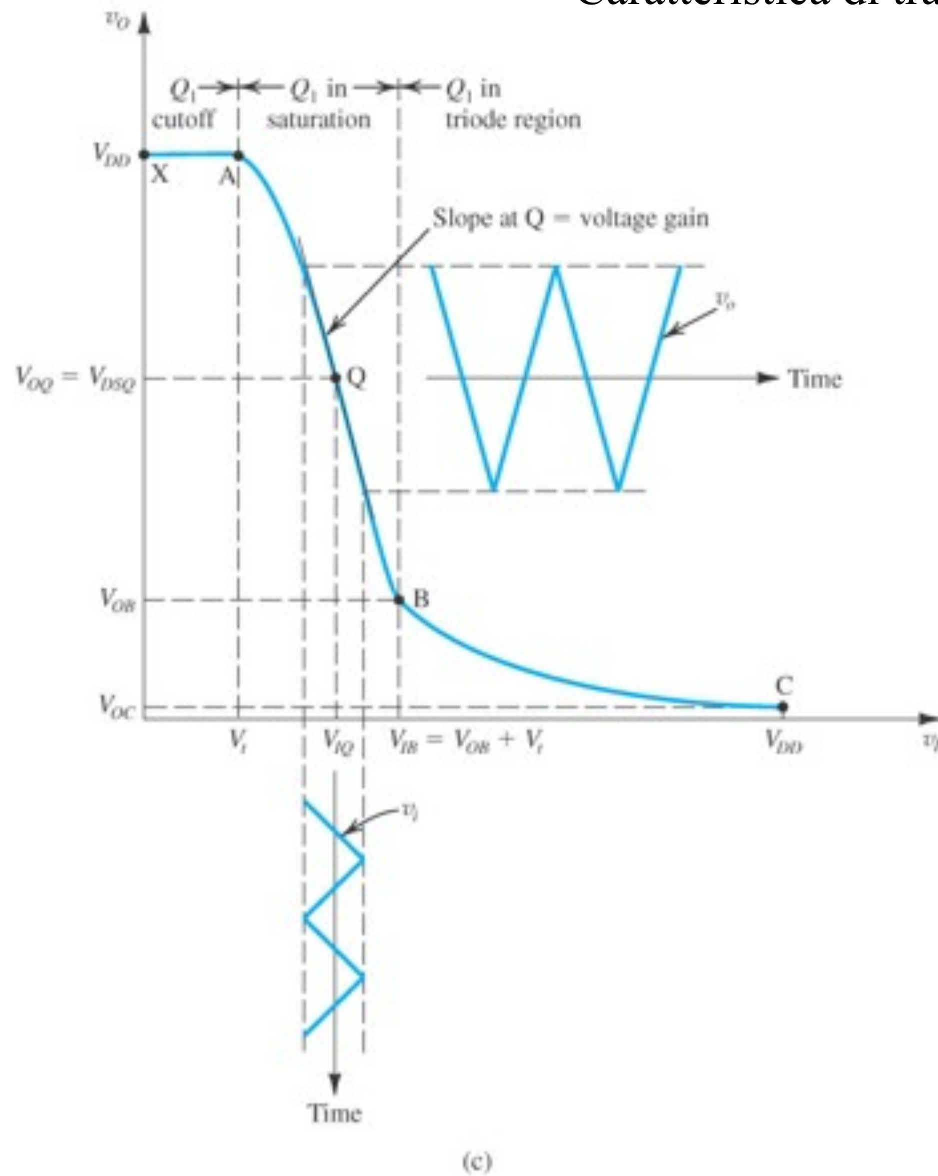

Figure 4.26 *(Continued)* **(c)** Transfer characteristic showing operation as an amplifier biased at point Q.

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Operazione come amplificatore lineare

Il punto di lavoro Q , o quiescent point, e' scelto a meta' del segmento saturazione nella curva di transfer. Questo per avere uno swing del segnale massimo.

Lavorando nella zona lineare della funzione di transfer, con un segnale vi sufficientemente piccolo si avra' un segnale vo proporzionale a vi, con un guadagno Av

$$A_v = \frac{dv_o}{dv_i}\Big|_{v_i = v_{iq}}$$

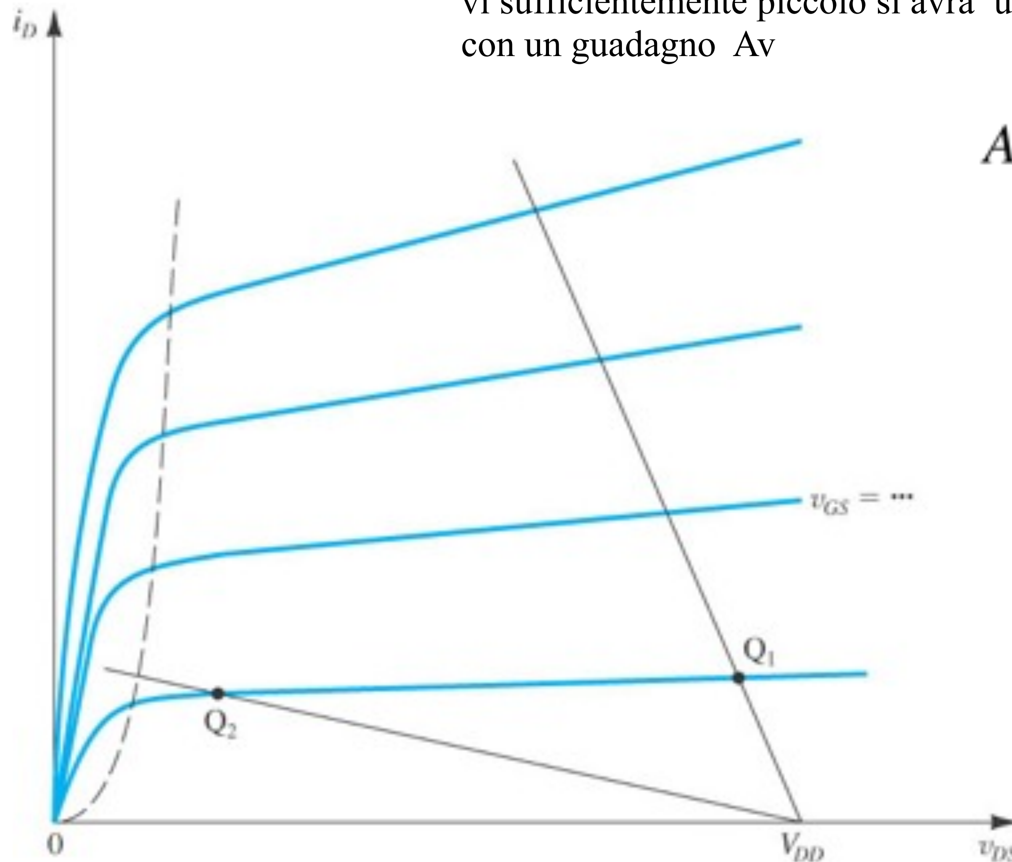

Figure 4.27 Two load lines and corresponding bias points. Bias point Q_1 does not leave sufficient room for positive signal swing at the drain (too close to V_{DD}). Bias point Q_2 is too close to the boundary of the triode region and might not allow for sufficient negative signal swing.

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Espressione analitica per la caratteristica di transfer

1) Regione di cut off $v_i \le V_D$ e $v_o = V_{DD}$

2) Regione di di saturazione $v_i \ge V_D$ e $v_o \ge v_i - V_D$

$$i_D = \frac{1}{2}(\mu_n C_{ox})(\frac{W}{L})(v_I - V_t)^2$$

$$v_o = V_{DD} - R_D i_D$$

$$v_o = V_{DD} - \frac{1}{2}(\mu_n C_{ox})(\frac{W}{L})(v_I - V_t)^2$$

Il guadagno sara' $A_v = -R_D(\mu_n C_{ox})(\frac{W}{L})(v_{IQ} - V_t)$

o in un'altra espressione $A_v = -\frac{2(V_{DD} - V_{OQ})}{V_{OV}} = -\frac{2V_{RD}}{V_{OV}}$ con V_{RD} = tensione DC ai capi di R_D

l'end-point della regione saturazione e' caratterizzato $V_{OB} = V_{IB} - V_t$

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3) regione triodo $v_i \geq V_t$, e $v_o \leq v_i - V_t$

$$i_D = \mu_n C_{ox} \frac{W}{L}[(v_i - V_t)v_o - \frac{1}{2}v_o^2] \quad , \quad \text{essendo} \quad v_o = V_{DD} - R_D i_D$$

$$v_o = V_{DD} - R_D \mu_n C_{ox} \frac{W}{L}[(v_i - V_t)v_o - \frac{1}{2}v_o^2]$$

se v_o e' piccolo

$$v_o \cong V_{DD} - R_D \mu_n C_{ox} \frac{W}{L}(v_i - V_t)v_o \quad , \quad \text{che si riscrive come} \quad v_o = V_{DD} / [1 + R_D \mu_n C_{ox} \frac{W}{L}(v_i - V_t)]$$

$$r_{DS} = 1 / [\mu_n C_{ox} \frac{W}{L}(v_i - V_t)]$$

da cui si ricava $v_o = V_{DD} \frac{r_{DS}}{r_{DS} + R_D}$ e poiche' usualmente $r_{DS} << R_D$

si ottiene la relazione usabile $v_o \cong V_{DD} \frac{r_{DS}}{R_D}$

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Biasing nei circuiti MOS

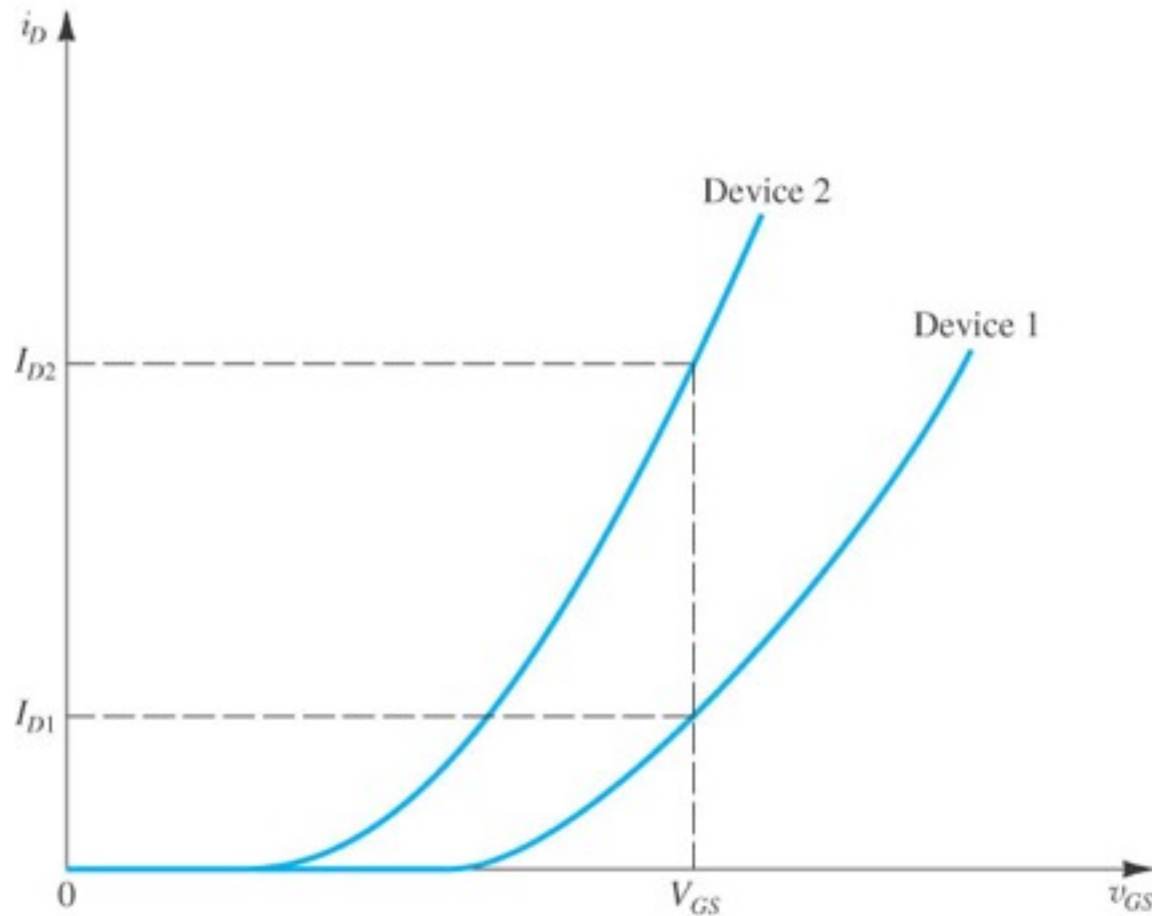

Figure 4.29 The use of fixed bias (constant V_{GS}) can result in a large variability in the value of I_D. Devices 1 and 2 represent extremes among units of the same type.

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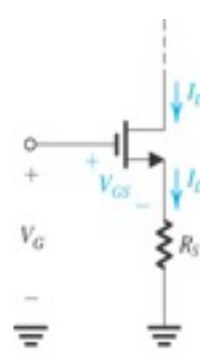
Biasing nei circuiti amplificatori MOS

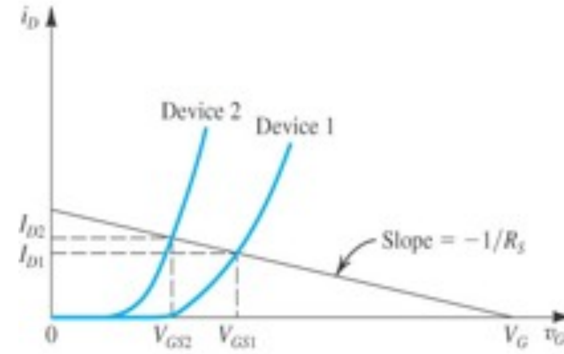
Biasing fissando V_{GS}, soluzione non favorita,
perche' transistori non tutti uguali anche tra stesso tipo

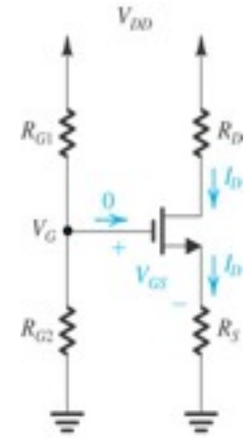
Biasing fissando V_G, soluzione favorita, si aggiusta
il valore caso per caso

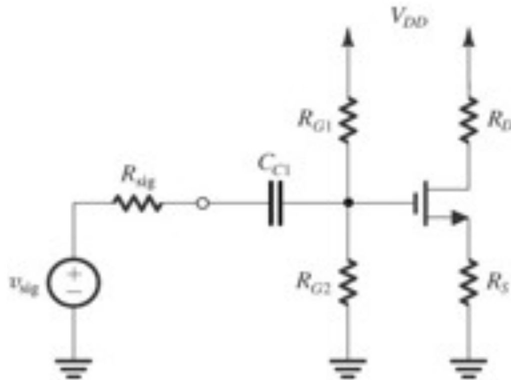
$$V_G = V_{GS} + R_S I_D$$

Agisce come feedback negativo









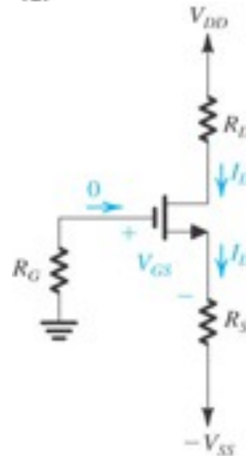


Figure 4.30 Biasing using a fixed voltage at the gate, V_G, and a resistance in the source lead, R_S: **(a)** basic arrangement; **(b)** reduced variability in I_D; **(c)** practical implementation using a single supply; **(d)** coupling of a signal source to the gate using a capacitor C_{C1}; **(e)** practical implementation using two supplies.

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Biasing con una resistenza di feedback tra Drain e Gate

$$V_{GS} = V_{DS} = V_{DD} - R_D I_D \quad \text{che diventa} \quad V_{DD} = V_{GS} + R_D I_D$$

R_D agisce come resistenza di feedback negativo

Il segnale al Gate non disturba la VGS e puo' essere usato come un CS amplifier.

Ha una limitazione nel fatto che lo swing del segnale in output non puo' essere molto esteso

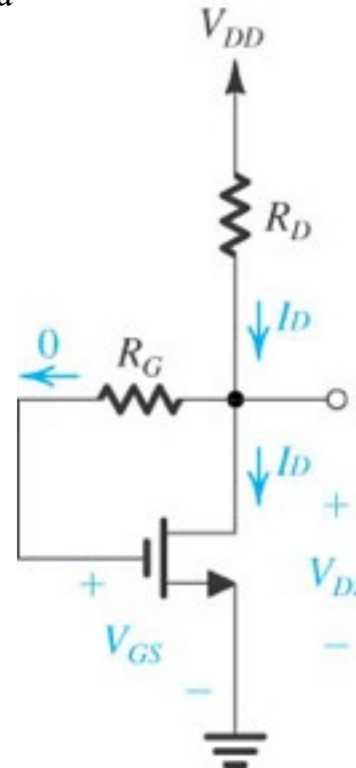

Figure 4.32 Biasing the MOSFET using a large drain-to-gate feedback resistance, R_G.

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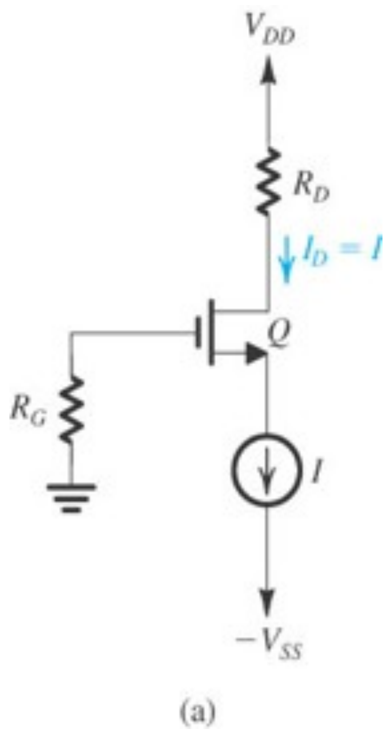
Biasing con CONSTANT CURRENT SOURCE

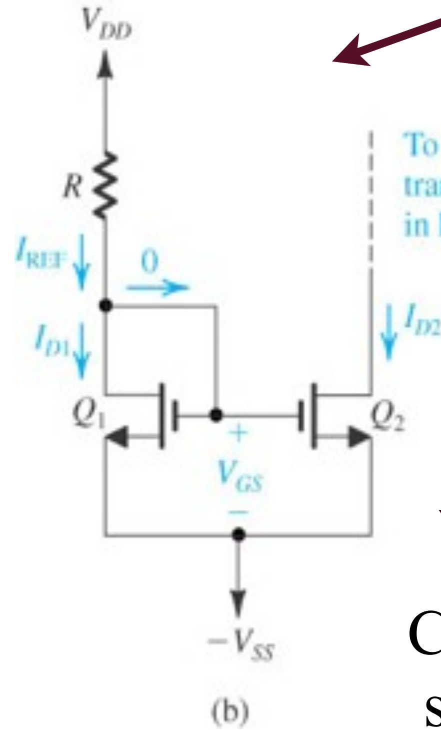
Modo piu' efficace

. R_G , ~ M Ohm, assicura un dc ground ed una alta resistenza in input

. R_D fissa un valore a V_D assicurando un largo swing al segnale in uscita ed assicurando che il MOS sia in saturazione

Circuito per implementare un CCS





$$I = I_{D2} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_2 (V_{GS} - V_t)^2$$

$$I = I_{ref} \left(\frac{(W/L)_2}{(W/L)_1}\right)$$

Circuito MIRROR CURRENT specchio di corrente

Figure 4.33 **(a)** Biasing the MOSFET using a constant-current source *I*. **(b)** Implementation of the constant-current source *I* using a current mirror.

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Small signal amplifier models

Il segnale v_{gs} e' sovrapposto al DC bias V_{GS}, assunto fisso.

Il punto di bias DC sara' scelto in modo da permettere lo swing del segnale

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2$$

$$V_D = V_{DD} - R_D I_D$$

Per avere saturazione $V_D > V_{GS} - V_t$ ma deve essere abbastanza grande da assicurare lo swing del segnale

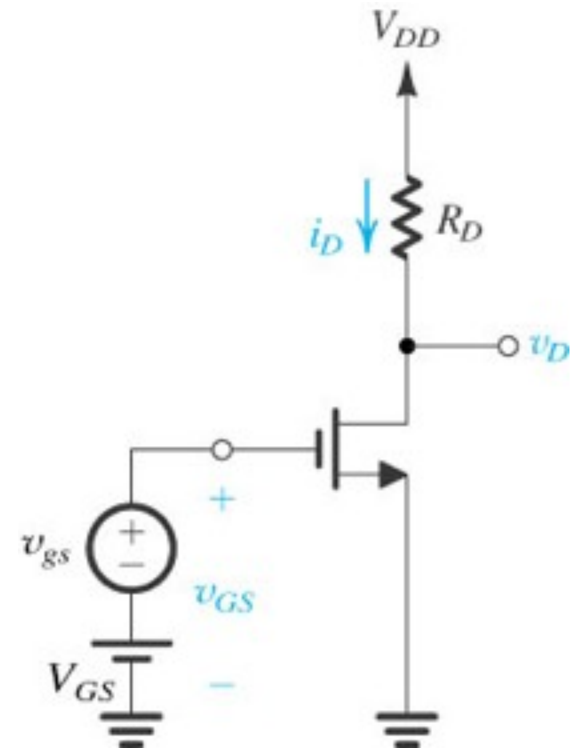

Figure 4.34 Conceptual circuit utilized to study the operation of the MOSFET as a small-signal amplifier.

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Il segnale di corrente sul terminale Drain

Applicando un segnale v_{gs}
la corrente di Drain istantanea sara'

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(V_{GS} + v_{gs} - V_t)^2$$

sviluppando compare un termine v_{gs}**2
non lineare

Per ridurre l'effetto deve essere

$$v_{gs} << 2(V_{GS} - V_t)$$

cosi'

$$i_D \approx I_D + i_d \quad \text{con} \quad i_d = k_n' \frac{W}{L}(V_{GS} - V_t)v_{gs}$$

il parametro che lega i_d a v_{gs} e' la transconduttanza g_m

$$g_m = \frac{i_d}{v_{gs}} = k_n'\left(\frac{W}{L}\right)(V_{GS} - V_t) = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{v_{GS} = V_{GS}}$$

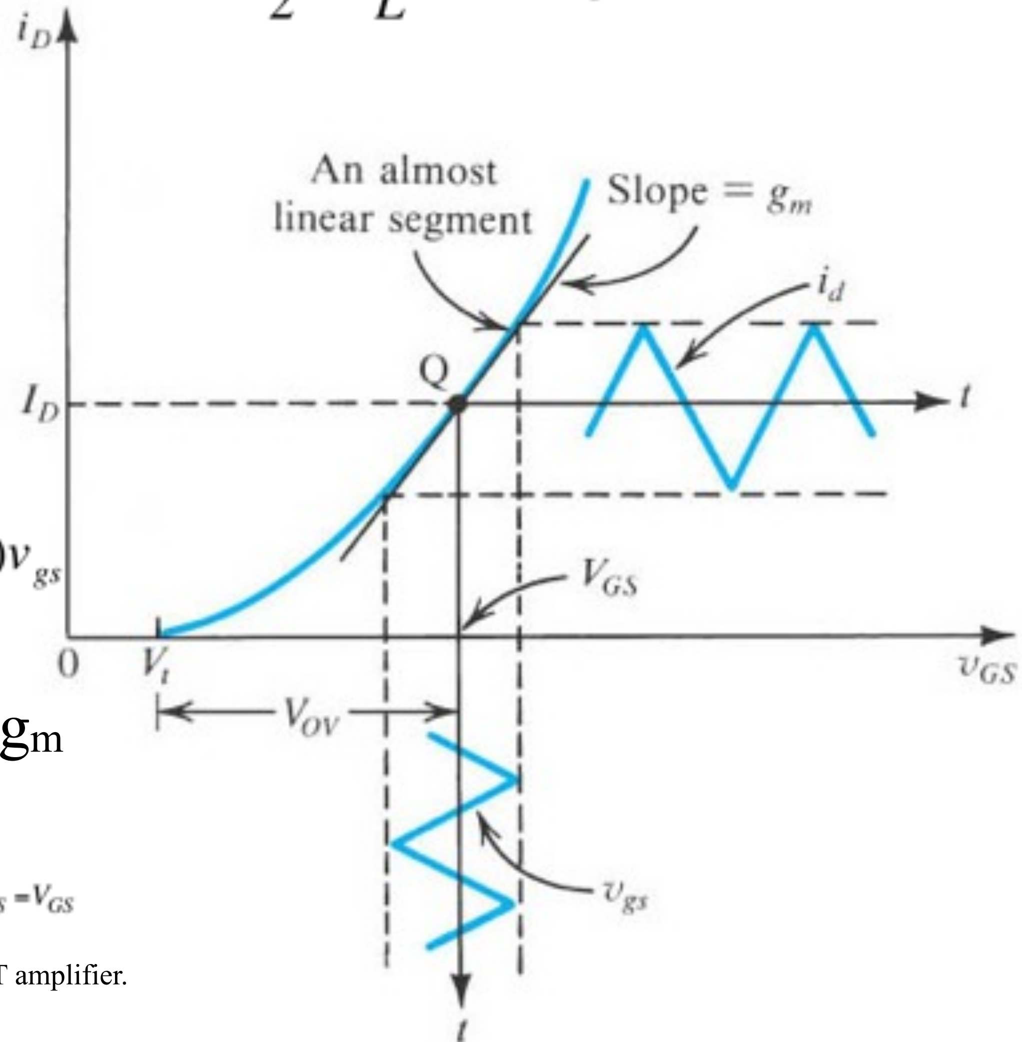


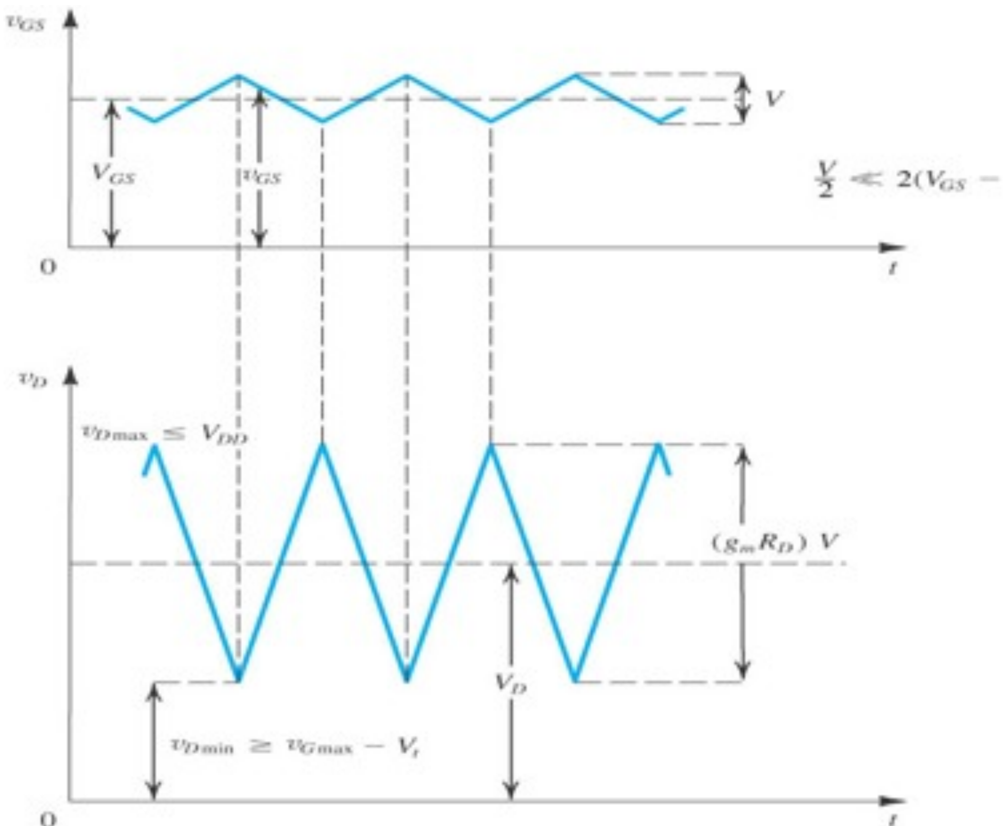
Figure 4.35 Small-signal operation of the enhancement MOSFET amplifier.

Guadagno in tensione

$$v_D = V_{DD} - R_D i_D$$

per piccoli segnali $v_D = V_{DD} - R_D(I_D - i_D)$ che diventa $v_D = V_D - R_D i_d$

in termini di g_m $v_d = -i_d R_D = -g_m v_{gs} R_D$



e il guadagno in tensione

$$A_v \equiv \frac{v_d}{v_{gs}} = -g_m R_D$$

il segno - indica un output con la fase invertita

Figure 4.36 Total instantaneous voltages v_{GS} and v_D for the circuit in Fig. 4.34.

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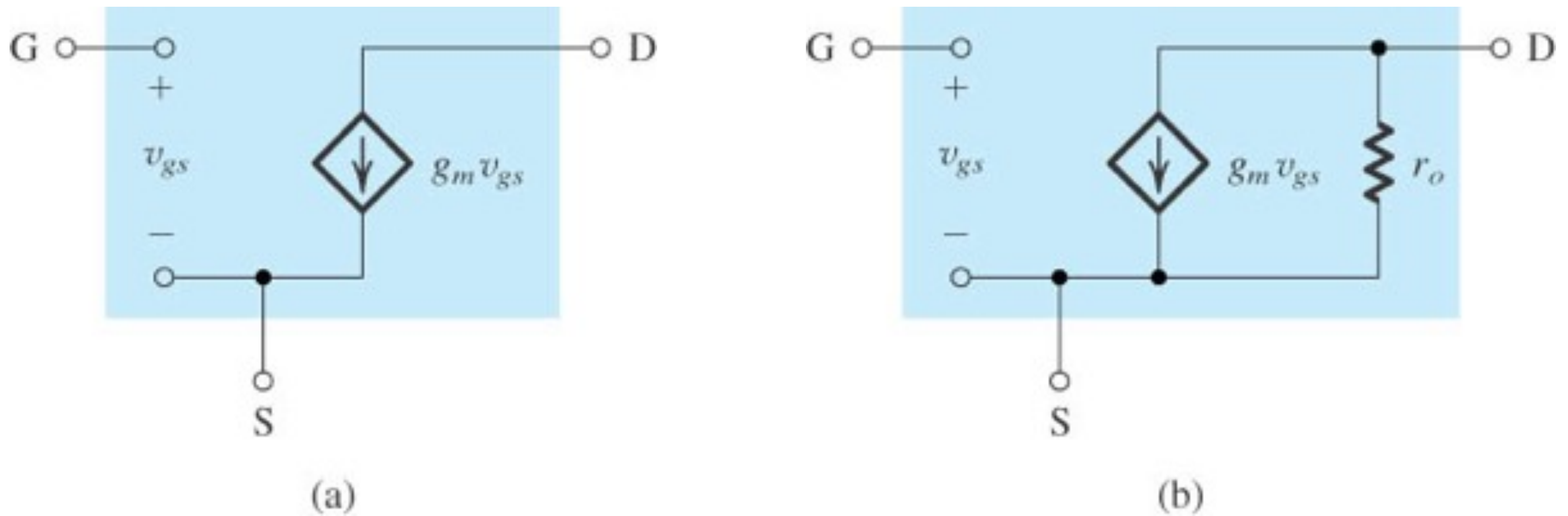

Figure 4.37 Small-signal models for the MOSFET: **(a)** neglecting the dependence of i_D on v_{DS} in saturation (the channel-length modulation effect); and **(b)** including the effect of channel-length modulation, modeled by output resistance $r_o = |V_A| / I_D$.

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Single stage MOS amplifier

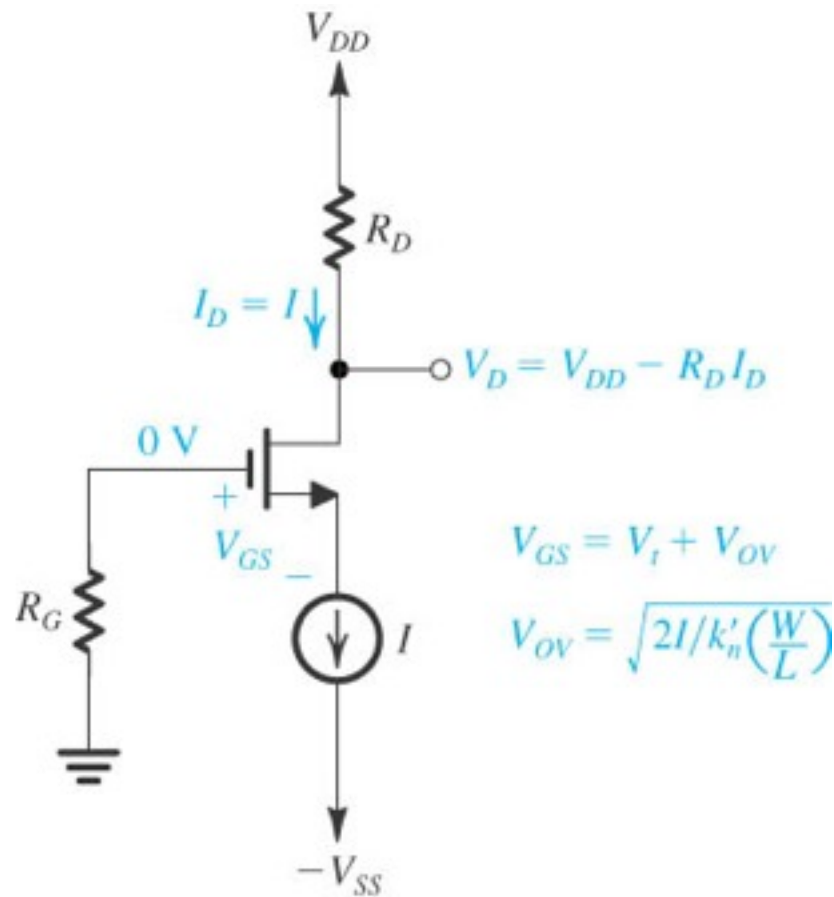

Figure 4.42 Basic structure of the circuit used to realize single-stage discrete-circuit MOS amplifier configurations.

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Common Source amplifier

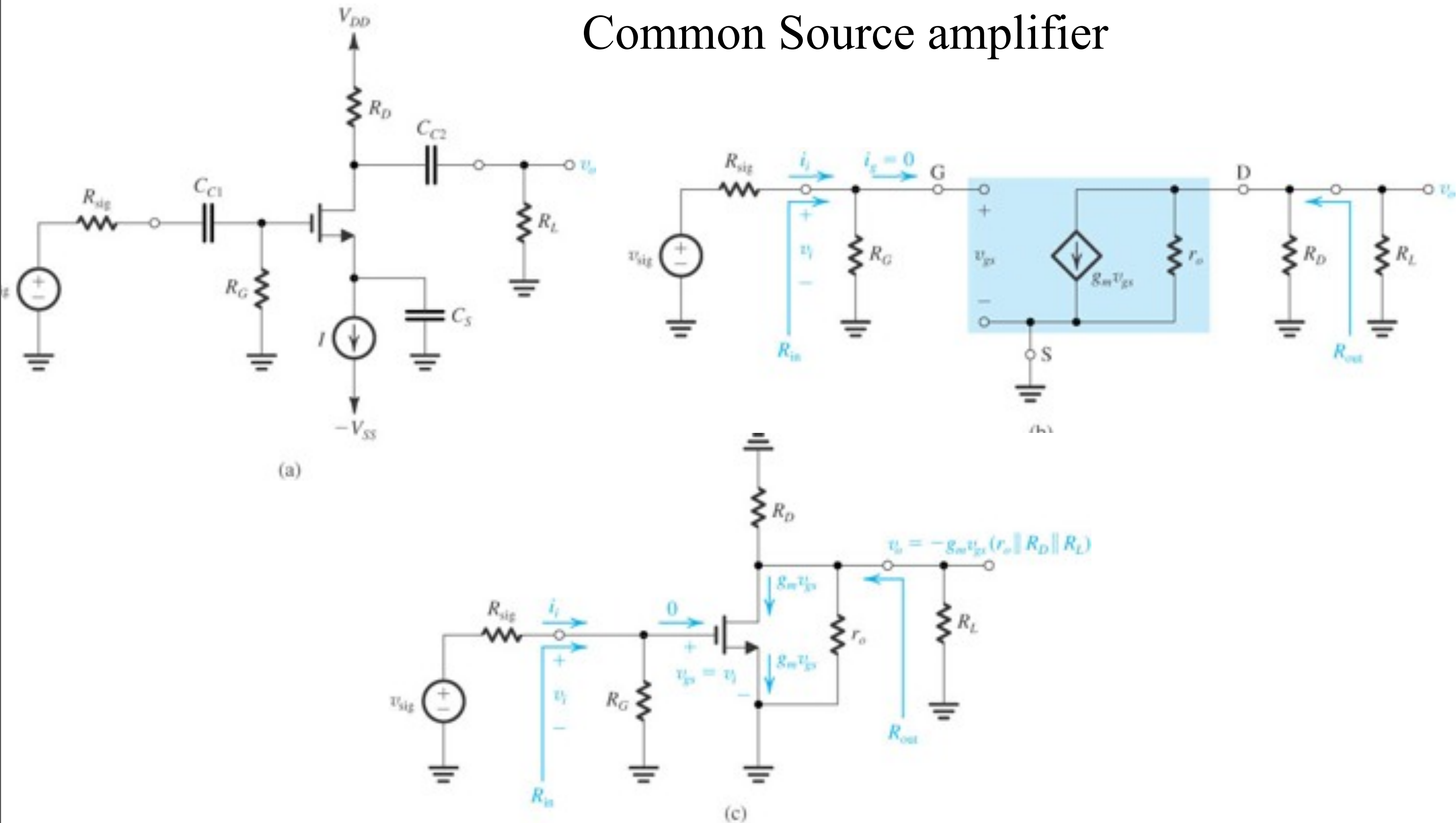

Figure 4.43 **(a)** Common-source amplifier based on the circuit of Fig. 4.42. **(b)** Equivalent circuit of the amplifier for small-signal analysis. **(c)** Small-signal analysis performed directly on the amplifier circuit with the MOSFET model implicitly utilized.

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CS amplifier

Caratteristiche di un CS amplifier: input resistance, voltage gain, output resistance

Dal modello a piccoli segnali del MOS

$$i_g = 0$$

$$R_{in} = R_G$$

$$v_i = v_{sig} \frac{R_{in}}{R_G + R_{sig}}$$

$$A_v = -g_m (r_o \| R_D \| R_L)$$

$$G_v = \frac{R_{in}}{R_{in} + R_{sig}} g_m (r_o \| R_D \| R_L)$$

$$R_{out} = r_o \| R_D$$

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Common Gate amplifier

Input signal sul source, output al drain.

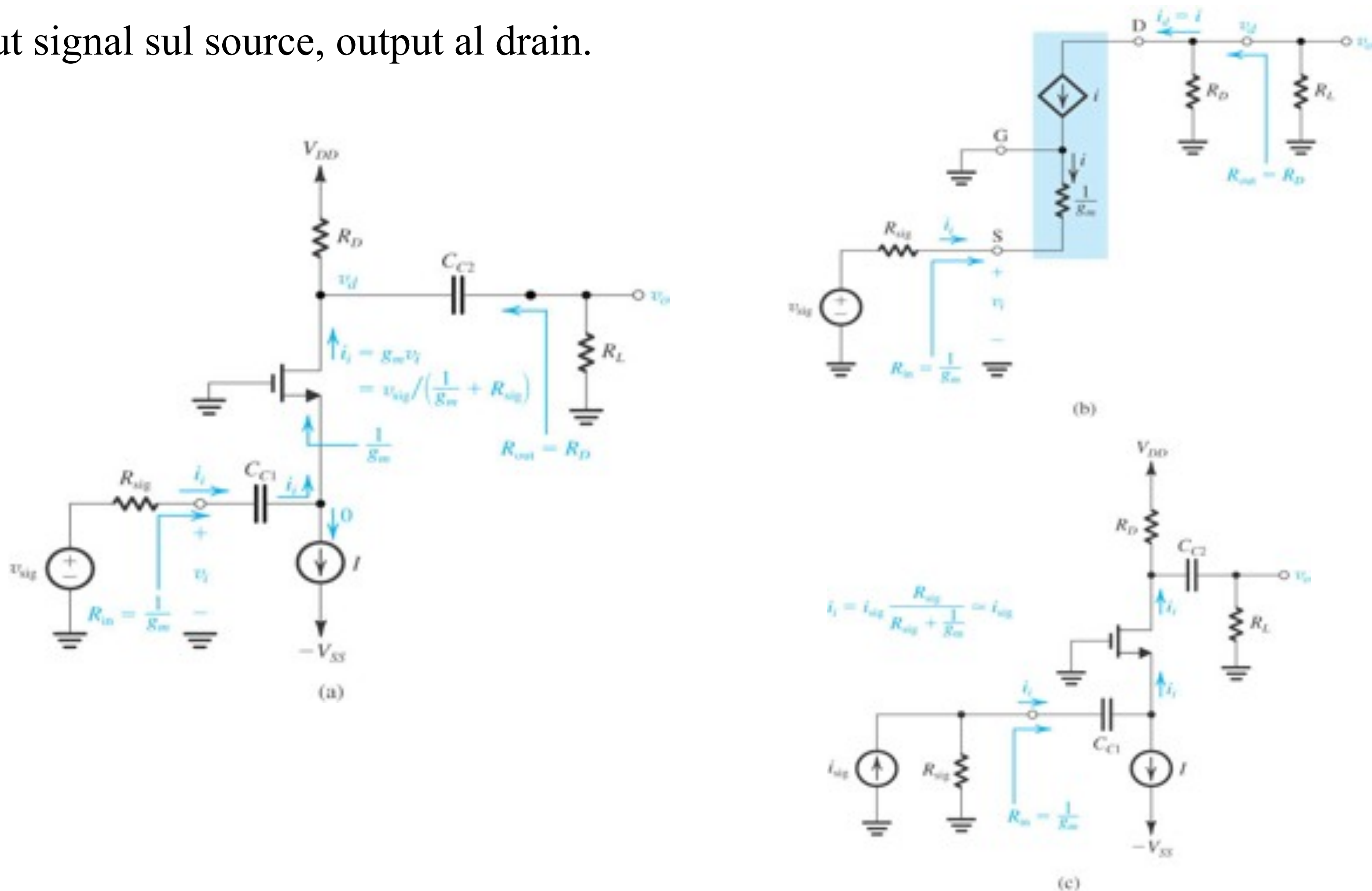

Figure 4.45 **(a)** A common-gate amplifier based on the circuit of Fig. 4.42. **(b)** A small-signal equivalent circuit of the amplifier in (a). **(c)** The common-gate amplifier fed with a current-signal input.

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Dal circuito si nota che $R_{in} = \frac{1}{g_m}$, e $v_i = v_{sig} \frac{1}{1 + g_m R_{sig}}$

ma per non avere riduzione del segnale in input

$$R_{Sig} << \frac{1}{g_m}$$

la corrente $i_i = \frac{v_i}{R_{in}} = \frac{v_i}{1/g_n} = g_m v_i$ e $i_d = i = -i_i = -g_m v_i$

cosi' l'output si puo' trovare come $v_{out} = v_d = -i_d (R_D \parallel R_L) v_i$

da cui il guadagno $A_v = g_m (R_D \parallel R_L)$ e a circuito aperto $A_v = g_m R_D$

Il guadagno totale del circuito $G_v = \frac{g_m (R_D \parallel R_L)}{1 + g_m R_{Sig}}$

e la resistenza di output e' $R_{out} = R_o = R_D$

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in conclusione

Confrontando il Common Source ed il Common Gate si puo' dire che:

1. Diversamente dal CS il CG e' non-invertente

2. Il CS amplifier ha una alta resistenza di input, il CG amplifier ha una bassa resistenza di input

3. Mentre i valori di A_v sia del CS che CG sono simili, il guadagno totale del CG e' minore di un fattore $1+g_mR_{sig}$ che e' dovuto alla piccola resistenza di input del circuito CG.

Il CG avendo una bassa resistenza di input ed una alta resistenza di output agisce come un UNITY GAIN CURRENT AMPLIFIER o CURRENT FOLLOWER

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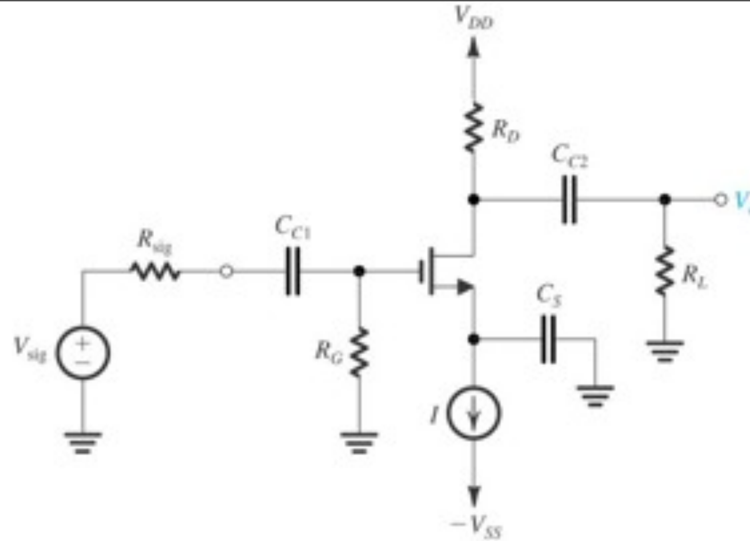

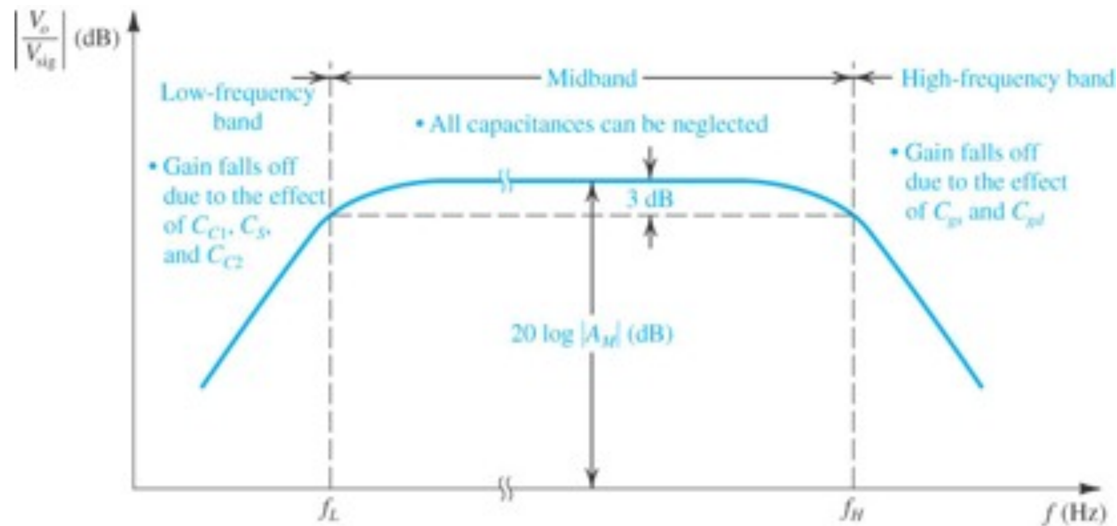

Figure 4.49 **(a)** Capacitively coupled common-source amplifier. **(b)** A sketch of the frequency response of the amplifier in (a) delineating the three frequency bands of interest.

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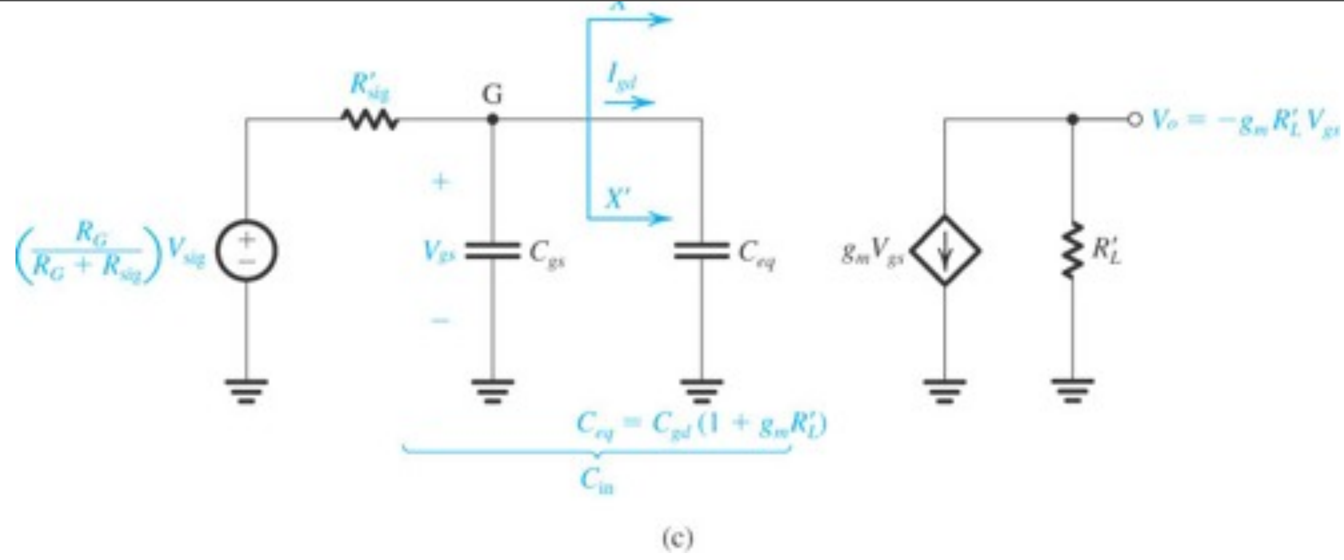
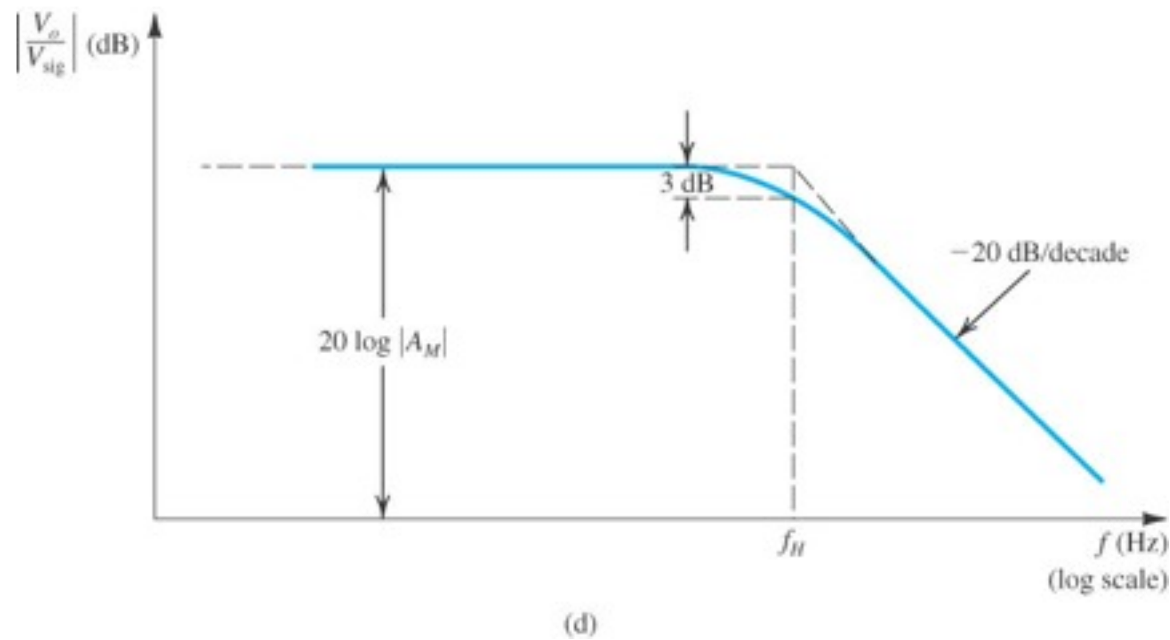


(c)



(d)

Figure 4.50 *(Continued)* **(c)** the equivalent circuit with C_{gd} replaced at the input side with the equivalent capacitance C_{eq}; **(d)** the frequency response plot, which is that of a low-pass single-time-constant circuit.

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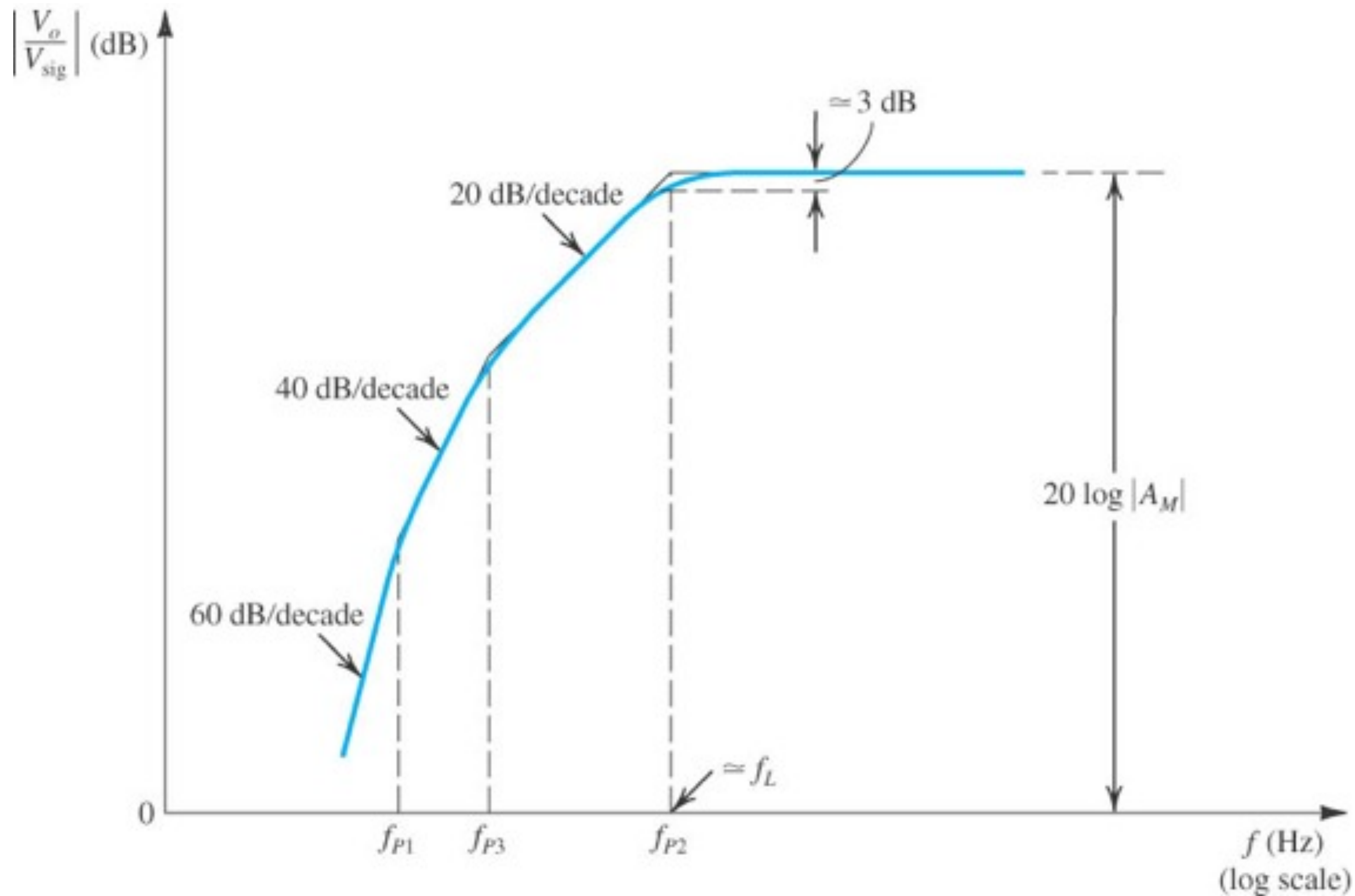

Figure 4.52 Sketch of the low-frequency magnitude response of a CS amplifier for which the three break frequencies are sufficiently separated for their effects to appear distinct.

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