Measurements of Matching and High Count Rate Performance of Multichannel ASIC for Digital X-Ray Imaging Systems

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***Abstract*—We present the measurements of matching and high count rate performance of a 64 channel readout ASIC called DEDIX for high count rate position-sensitive measurements using semiconductor detectors. The ASIC is designed in 0.35 μm CMOS process and its total area is 3900×5000 μm^2. The DEDIX has a binary readout architecture. Each channel is built of a charge sensitive amplifier (CSA) with a pole-zero cancellation circuit, a shaper, two independent discriminators and two independent 20-bit counters. The size of the input device in CSA has been optimized for a detector capacitance in the range of 1–3 pF per strip. An equivalent noise charge of 110 el rms has been achieved for a total detector capacitance of 1 pF at the shaper peaking time of 160 ns. Internal correction DAC implemented in each channel independently ensures a low spread of discriminator effective threshold, namely 0.4 mV at one sigma level. The mean gain in the multichannel ASIC is 54 μV/el, with a good uniformity from channel-to-channel (sd/mean $\approx 0.8\%$). Low noise performance and high rate capability have been demonstrated by the measurement up to and above 1 MHz average rate of input signals.**

***Index Terms*—Charge sensitive amplifier, count rate, matching.**

I. Introduction

TODAY, there is a growing interest in digital position sensitive X-ray imaging systems working in single photon counting modes which are able to cope with high intensity of X-ray radiation. Such systems are needed for gas and semiconductor detectors of different shape like strips, pads or pixels for applications in biology, medicine, chemistry and physics.

To efficiently use the array of sensors an ASIC with multichannel architecture and fast signal processing is necessary [1]–[14]. The critical parameters of the multichannel ASIC are proper operation with high rates of input signals, together with low noise performance and a good uniformity of analogue parameters for all channels. In this paper we present the development of multichannel readout ASIC called DEDIX for low energy (5–50 keV) X-ray imaging system, which fulfils the requirements mentioned above. The ASIC is supposed to work with a silicon strip detector (SSD). The core of the IC consists of 64 front-end channels with a binary readout architecture and two voltage discriminators per channel. Binary information can easily be stored in an integrated circuit, which allows one to cope with the high intensity of X-ray radiation as each channel works independently. The concept of the circuit architecture is similar to previous the RX64, RX64DTH circuits [15], [16]; however, in this design our aim was to significantly increase (ten times) the maximum counting rate per single channel up to 1 MHz for statistically distributed input pulses, keeping low noise performance and very good uniformity of effective threshold spread from channel to channel.

The paper is organized as follows. Section II describes the single channel architecture. Section III details about the layout of the 64-channel IC. The measurements of effective threshold spread of the multichannel ASIC and the correction procedure are presented in Section IV. The measurement results of high count rate performance are shown in Section V. Section VI contains a summary.

II. Single Channel Architecture

The block diagram for a single channel is shown in Fig. 1. Each channel is built of a charge sensitive amplifier (CSA) with a pole-zero cancellation (PZC) circuit, a shaper CR-RC^2 with a peaking time of 160 ns, two discriminators, and two independent 20-bit counters.

The threshold voltages for two discriminators in a single channel are set independently but are common for all 64 channels of ASIC. Because from the CSA input up to the discriminator inputs the signal processing chain is DC-coupled, a correction DAC is necessary (working in each channel independently) to minimize the effects of the DC level spread at the discriminator inputs in the multichannel ASIC. Both the architecture of CSA with PZC circuit and the problem of the DC level spread at discriminator input are discussed below.

A. CSA With PZC Circuit

The CSA is based on the folded cascode configuration (see Fig. 2) with a PMOS input transistor M1 with $W_1/L_1 = 600$ μm/0.45 μm. The transconductance of M1 is $g_{m1} = 9.45$ mA/V for the current $I_{DS1} = 0.9$ mA and $g_{m1} = 12.17$ mA/V for $I_{DS1} = 1.47$ mA (from simulations). The feedback loop of the CSA is formed by the capacitor C_f of

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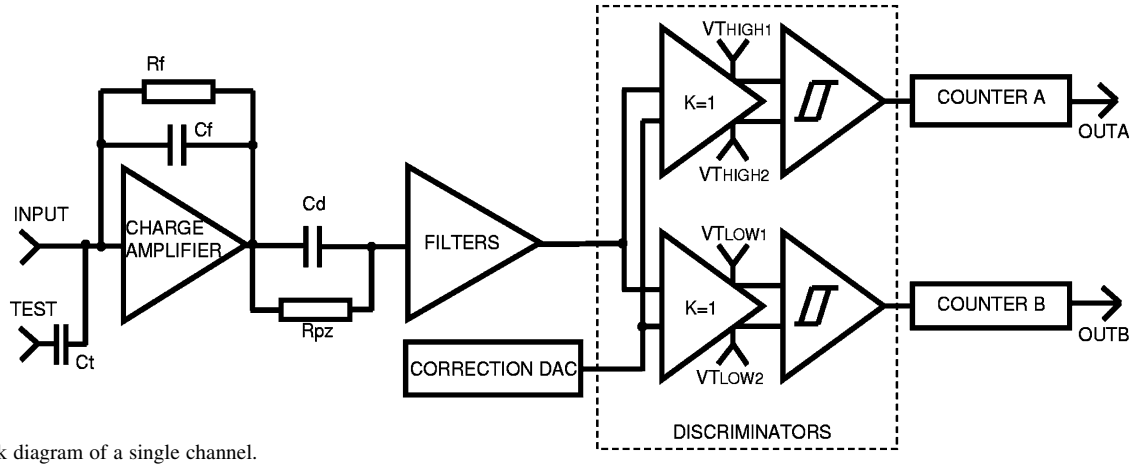

Fig. 1. Block diagram of a single channel.

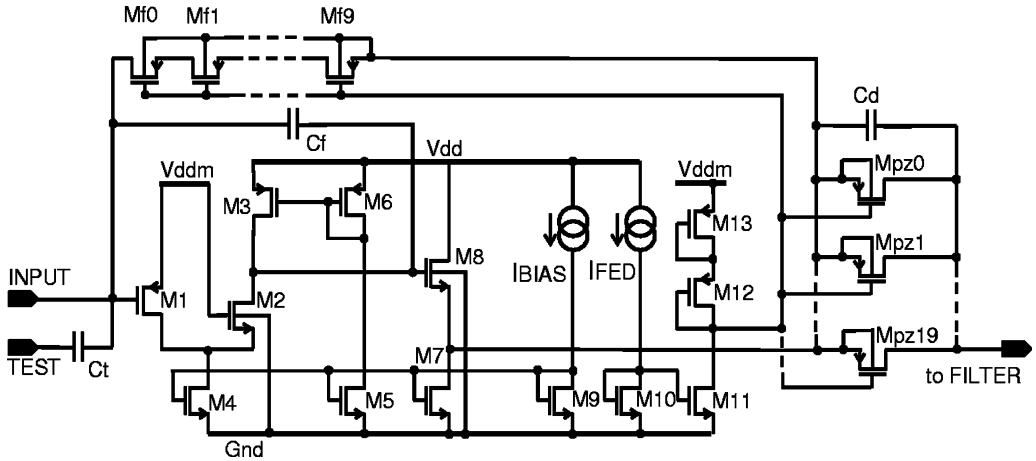

Fig. 2. Scheme of charge sensitive amplifier with PZC circuit.

100 fF and the channel conductance of the array of ten PMOS transistors Mf0–Mf9 with $W_{\rm f}/L_{\rm f} = 0.4\ \mu{\rm m}/10\ \mu{\rm m}$ connected in series. The pole-zero cancellation circuit consists of the capacitor $C_d = 24$ pF and 20 PMOS transistors Mpz0–Mpz19 of $W_{\rm pz}/L_{\rm pz} = 0.4\ \mu{\rm m}/10\ \mu{\rm m}$ connected in parallel. For negligible detector leakage current the transistors in CSA feedback and in PZC circuit are working in the triode region [17], [18]. The gates and sources of the transistors Mf9 and Mpz0–Mpz19 are connected together. This allows for the possibility of setting the effective CSA feedback resistance $\rm R_{Mf}$ in a wide range (from tens of MΩ to tens of GΩ), keeping the PZC circuit working properly even for high rates of input pulses which generate a DC voltage shift $V_{\rm CSAshift}$ at CSA output.

Using the PZC circuit eliminates undershoots after the differentiating filter stage, which are the results of the long time decay of pulses at the CSA output. However, this results in DC coupling between CSA input and discriminator inputs. The offsets propagate from CSA input to discriminator inputs and result in a spread of the effective discriminator threshold in a multichannel ASIC.

B. Simulation of the Effective Threshold Spread at Discriminator Inputs

In the application discussed in this paper the pulses after the filter stage are selected by two discriminators according to their amplitude (see Fig. 3). The threshold levels $VT_{\rm LOW}$ and $VT_{\rm HIGH}$ are set independently, but they are common to all 64 channels. The critical aspects of such a solution in the multichannel ASIC are the channel-to-channel spreads of the following:

— discriminators offsets;

— DC level of the base line at discriminators inputs.

The former problem can be efficiently reduced by a proper circuit architecture, transistors dimensions, bias conditions and symmetry in the layout of discriminators. The latter problem is more complicated, because the gain of the CSA and the filter stage is high, resulting in a much larger channel-to-channel

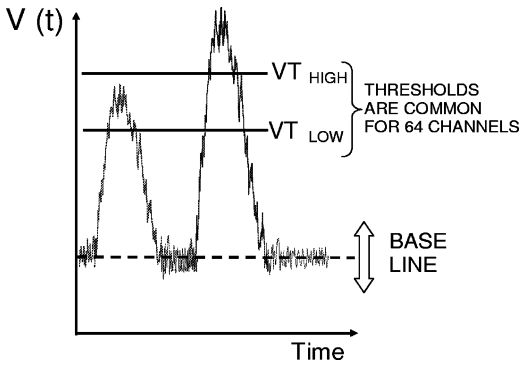

Fig. 3. Pulses after filter stage are selected according to their amplitudes.

TABLE I
MATCHING PARAMETERS FOR MOS TRANSISTORS

Parameter	A_{VT}[mVμm]	K [%μm]
NMOS	8.2	0.2
PMOS	14.9	0.4

DC level spread at the discriminators inputs. To overcome this problem, we propose a simple correction circuit, implemented in each channel independently. To estimate the spread of DC level at the discriminator inputs we performed Monte Carlo simulations during the design stage of the front-end channel.

Monte Carlo Simulations: The mismatch parameters for the threshold voltage V_T and current gain factor K in the technology used are given according to the following equations:

$$\sigma^2(V_T) = \frac{A_{VT}^2}{WL} \tag{1}$$

$$\frac{\sigma^2(K)}{K^2} = \frac{A_K^2}{WL} \tag{2}$$

where the values of mismatch parameters A_{VT} and A_K are listed in Table I.

The resistors and capacitors matching is described by a similar formula as that for current gain factor matching, and the value used for the high-poly resistor is 7% μm, while that for the poly1-poly2 capacitors is 1.2% μm. In the Monte Carlo simulations each of the above mentioned parameters is sampled independently from a given distribution. Since (1) and (2) specify the matching of a pair of the devices, the standard deviation for single devices used in Monte Carlo simulations should be smaller by a factor of $1/\sqrt{2}$. We assumed two corner bias conditions of the CSA and the filter stage with currents I_{BIAS1} and I_{BIAS2} which differ by a factor of 2.

With the above assumptions we performed the Monte Carlo analysis using HSPICE to estimate the channel-to-channel spread of the DC level at the discriminators inputs. The results of MC simulations are presented in Fig. 4. From the performed simulations one can see that the mean DC level at the discriminators input differs significantly in both cases I_{BIAS1} and I_{BIAS2}. This difference should be automatically suppressed in the correction circuit, which should have the same bias reference as the CSA and the filter stage. The DC level spread obtained in both cases is of about sd $= 7.8$ mV. These simulations allow us to set the range of the correction DAC and its necessary resolution. We assumed that the voltage range of the correction DAC should be of about 60 mV. The resolution of the correction DAC was set to 7-bit, that results in nearly a five times smaller step than the minimum step of the threshold DAC.

C. Correction Circuit and Discriminators Architecture

A scheme of the correction circuit and two discriminators is shown in Fig. 5. A large channel-to-channel DC level spread at the discriminator input is suppressed individually in each channel by the input correction circuit consisting of transistors M20, M21 and tuneable current source I_{COR}. This correction circuit generates V_{INREF} voltage to bias the discriminators input stages. We have made the assumption that the V_{INREF} voltage should depend on both the following:

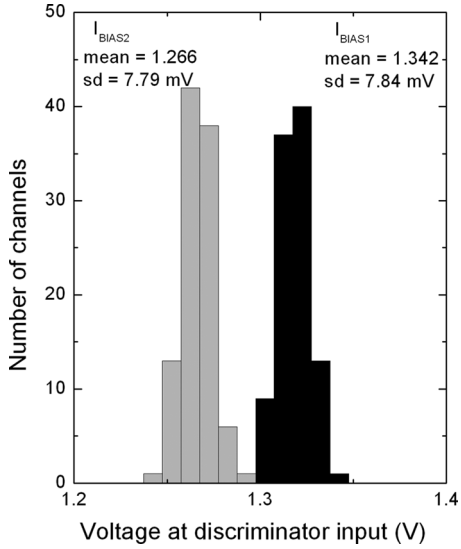

Fig. 4. Distributions of the DC level of the base line at discriminator input of single channel obtained after 100 iterations of Monte Carlo matching analysis.

— power supply voltage V_{ddm} and current reference source I_{BIAS}, which are used to bias the CSA (see Fig. 2) and the filter stage;
— tunable current source I_{COR} controlled by the internal correction DAC (there is an independent correction DAC in each channel).

The reference voltage V_{INREF} generated by the correction circuit can be calculated as

$$V_{\mathrm{INREF}} \approx V_{ddm} - \left(|V_{T20}| + \sqrt{\frac{2L_{20}}{\mu_0 C_{\mathrm{ox}} W_{20}} (I_{\mathrm{COR}} + I_{D21})} \right) \tag{3}$$

where V_{ddm} is the positive power supply of the CSA and the filter stage, V_{T20} is the threshold voltage of the transistor M20, W_{20} and L_{20} are the width and length of the transistor M20, μ_0 is the mobility, C_{ox} oxide capacitance per area, I_{D21} drain current of transistor M21, and I_{COR} is the correction current set by the internal DAC.

There are two fully differential discriminators in each channel, which have a common input (V_{INPUT}) and common reference (V_{INREF})—see Fig. 5. The input differential stages M22–M26 and M36–M40 have gain close to 1 and are used to provide differential threshold voltages:

$$VT_{\mathrm{HIGH}} = VT_{\mathrm{HIGH2}} - VT_{\mathrm{HIGH1}} \tag{4}$$

$$VT_{\mathrm{LOW}} = VT_{\mathrm{LOW2}} - VT_{\mathrm{LOW1}} \tag{5}$$

for the first and the second discriminator, respectively. These threshold voltages are set to a common value for all channels by two 8-bit threshold DACs $(1\ \mathrm{LSB} = 2.96\ \mathrm{mV})$. Due to the differential architecture of the discriminator the IC can work with both positive and negative input pulses. The following stages M27–M35 and M41–M49 are comparators with hysteresis. In order to reduce the effect of the comparator switching on the CSA and the filters performance, the discriminators use a separate positive power supply V_{dd} (separate from V_{ddm}). The power dissipation in each discriminator is about 0.4 mW.

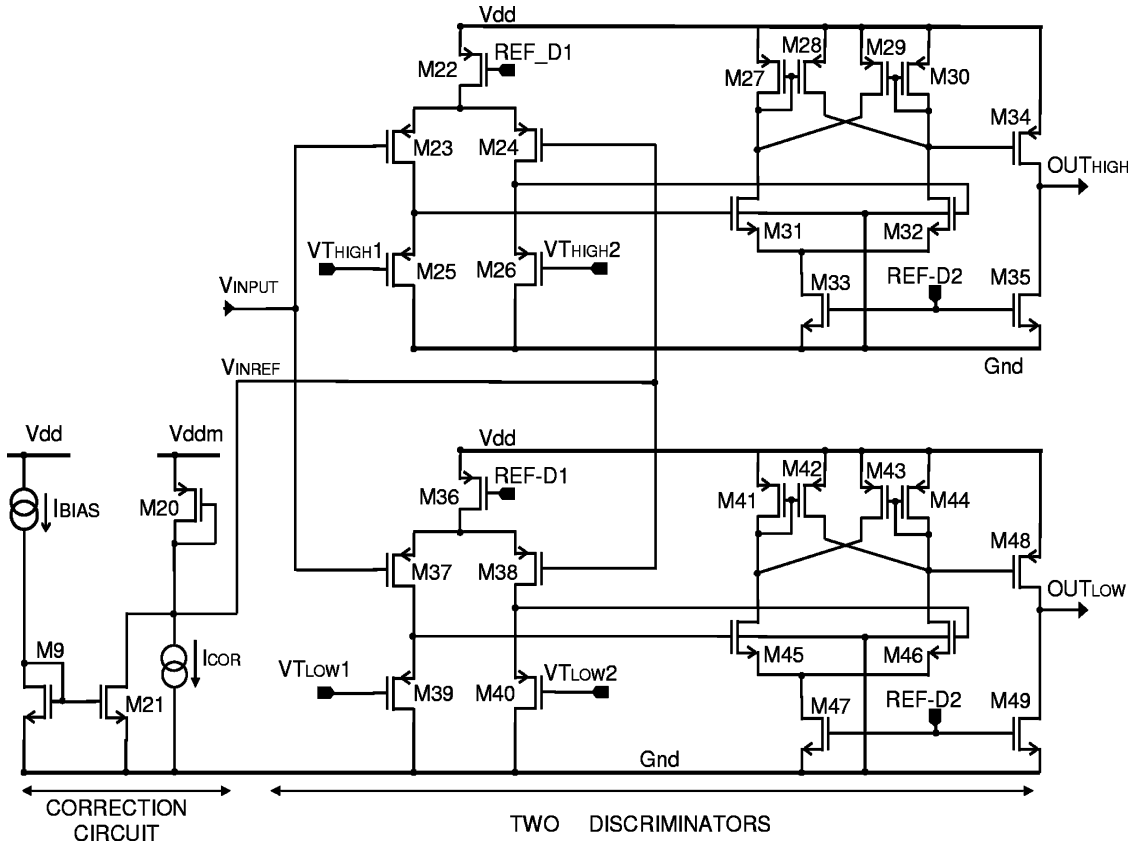

Fig. 5. Scheme of a pair of discriminators and a correction circuit.

Taking into account the process matching parameters and other requirements (power distributions, fast response, circuit area) transistor dimensions in discriminators have been sized to obtain a discriminator offset spread of less than 1.5 mV at one sigma level. This has been also verified by the Monte Carlo simulations.

III. Layout

The ASIC is designed in 0.35 μm CMOS process and the layout total area is 3900×5000 μm^2 (see Fig. 6). Particular attention was paid to the floor plan, guard rings and distribution of power supply voltages. The analog and digital blocks have separate multiple bonding pads for their power supply lines. For example, the analog power supply line V_{ddm} runs across all channels and it is nearly 5000 μm long and nearly 400 μm wide. This line is a stack of metal 2, metal 3, and metal 4 layers and it is connected via triple bonding pads placed symmetrically on each side of ASIC. The input pads are placed in two rows with a 75 μm pitch, and n-wells are used to vertically shield them from substrate noise [19], [20].

The front-end channel has been designed using full custom techniques, following the layout rules for good matching. The layout of the front-end channel is 60 μm wide and 2.4 mm long. At the discriminator inputs we placed small probe pads of 28×28 μm^2 area to test the DC level spread (under a probe station). A full custom design technique has also been used to design the counter block and I/O circuit with the purpose of minimizing the area of these blocks.

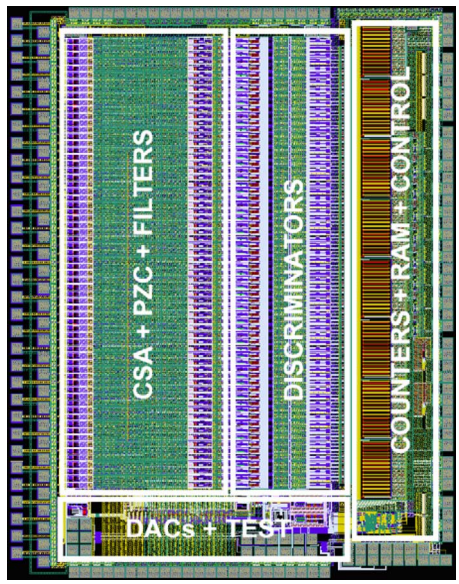

Fig. 6. Layout of DEDIX chip.

IV. Effective Threshold Spread. Measurements and Correction

A. Measurements of DC Level Spread at Discriminator Inputs

To measure the DC level spread in a 64-channel ASIC we used probe pads placed in each channel at the discriminator inputs. The results of these measurements obtained for two dif-

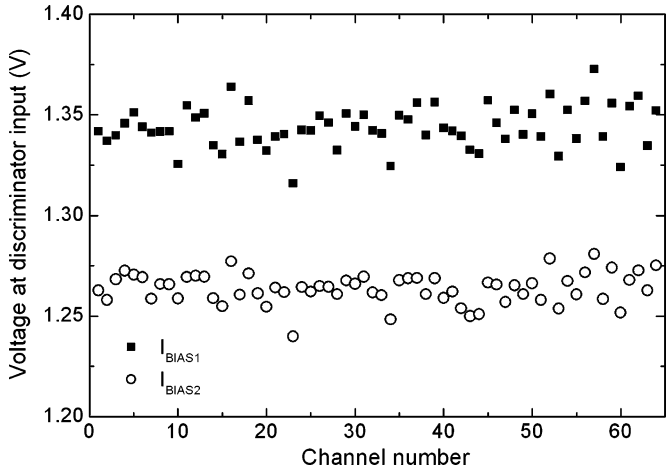

Fig. 7. DC voltages at the discriminators input in different channels.

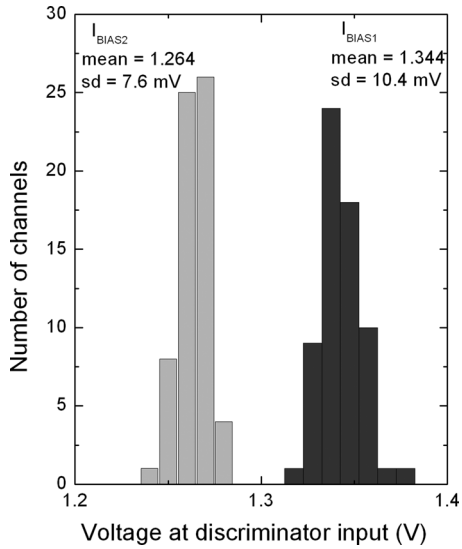

Fig. 8. Histograms DC voltages at the discriminators inputs in different channels.

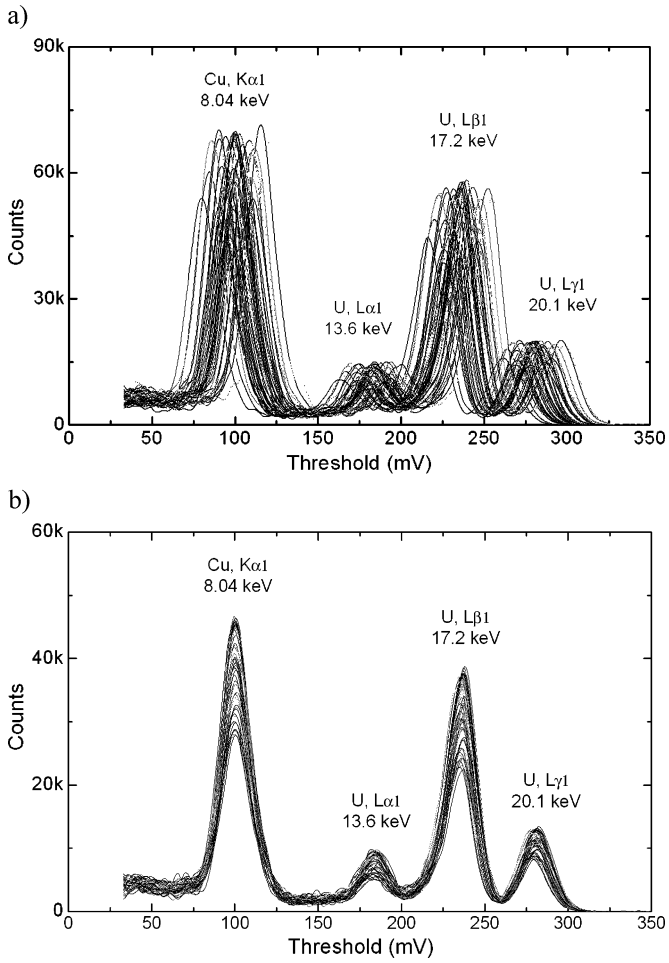

Fig. 9. Spectra of Pu-238 radioactive source and Cu K_α line measured with silicon strip detector and DEDIX chip: (a) before correction and (b) after correction.

ferent bias conditions I_{BIAS1} and I_{BIAS2} are shown in Figs. 7 and 8. We do not observe any gradient across the ASIC in DC level at the discriminator input. The spread of the DC level is at the same level as predicted by the MC simulations.

The measurements described above have several disadvantages.

— They are time consuming.

— They take into account only the dominant spread of the DC level at the discriminator inputs. However, the effective threshold setting for a given input signal depends also on the gain spread of the front-end electronics and on the spread of offsets in the discriminators themselves.

These problems can be effectively overcome using the X-ray calibration source and the possibility of threshold scan in the multichannel ASIC.

B. Correction Procedure

The correction procedure consists of three main steps.

First step. Measurements of effective threshold voltage spread with the multichannel ASIC connected to the strip detector and using X-ray calibration source, which produces photons of given energies (Pu-238 radioactive source with additional copper foil to obtain fluorescent radiation of lower energy). We made a threshold scan with the threshold voltage, for example VT_{LOW}, and with the same value of correction DACs in each channel. To obtain a good statistics (large number of counts), this measurement should be relatively long. By differentiating the measured integral distribution we obtained the spectra of Pu-238 radiation source and Cu K_α peak for all 64 channels, as shown in Fig. 9(a).

Second step. Characterization of correction DAC in each channel is done, using the internal generator circuit. The internal generator circuit produces a small voltage step V_t which is applied through a small test capacitor C_t to the input of the CSA in each channel [16]. The charge injected to the input equals $Q_{\mathrm{inj}} = C_t \times V_t$. These voltage steps are applied with frequency of 200 kHz. Making the threshold scan and differentiating the measured integral distribution we find the peak position for different values of correction DACs (0, 10, 20, ..., 120, 127). The obtained results are fitted to a second order polynomial (see Fig. 10).

Third step. With results from the first and the second step we can exactly calculate the proper value of correction DAC in

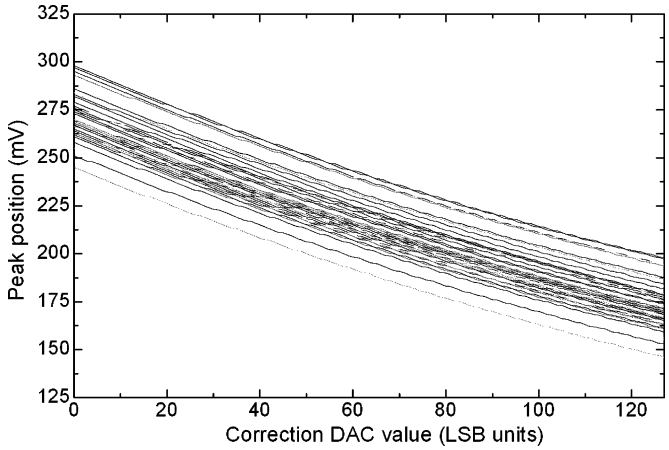

Fig. 10. Peak positions in 64 channels as a function of correction DACs values.

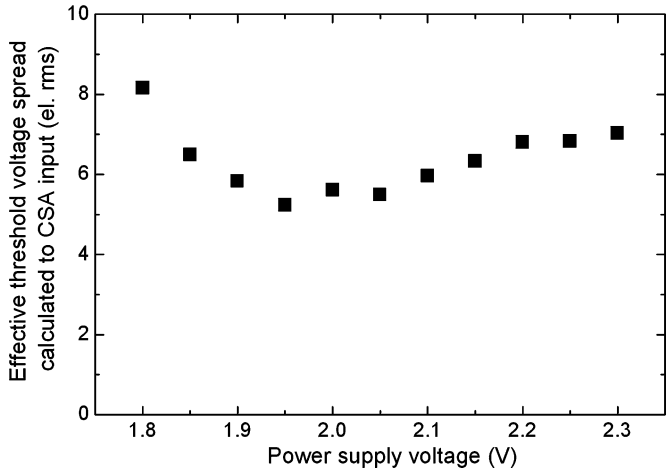

Fig. 12. Sigma of the effective threshold voltage spread referred to the input of CSA versus power supply voltage V_{ddm}, keeping the same values of correction DACs.

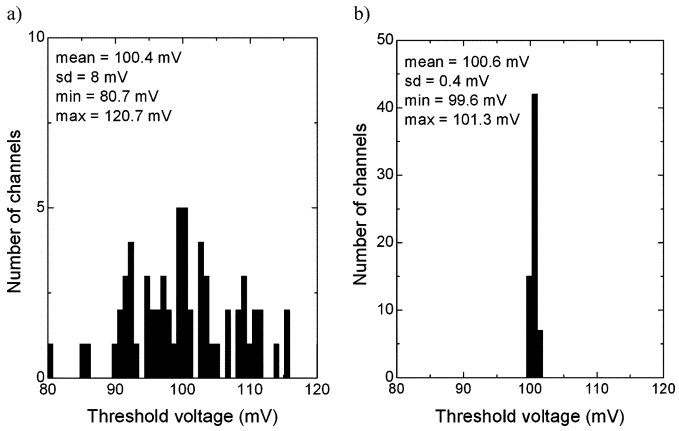

Fig. 11. Histograms of Cu $K_{\alpha 1}$ peak position in 64 channels of DEDIX: (a) before correction and (b) after correction.

TABLE II
GAIN AND NOISE PERFORMANCE OF DEDIX IC WITH DIFFERENT TYPE OF SILICON STRIP DETECTOR

Strip detector type / pitch / length	Mean gain [μV/el]	Spread of gain [%]	Mean ENC [el. rms]	Spread of ENC [el. rms]
AC / 75μm / 1cm	52.9	0.62	136	4.4
	53.6	0.87	136	4.0
	55.2	0.84	137	5.3
	52.9	0.87	133	5.6
	53.0	0.77	137	3.7
	56.0	0.86	144	4.1
AC / 100μm / 1cm	54.8	0.65	138	3.8
	55.5	0.88	137	5.8
AC / 100μm / 2cm	53.8	0.75	194	3.8
DC / 50μm / 2cm	52.7	0.76	230	5.1

Measurements presented above are for 10 different ASICs, randomly selected from a single production run

each channel for a given threshold level (e.g. threshold voltage level equivalent to the Cu K_α peak -8 keV).

To verify the above procedure we repeat the measurement with the X-ray source for the new set of correction DAC values: the corresponding results are shown in Fig. 9(b). Differences in count numbers for various channels are due to non-uniform radiation intensity across the channels. Having these results we make histograms of the Cu K_α peak position before and after correction, shown respectively in Fig. 11(a) and Fig. 11(b). After the correction the spread of effective threshold voltage calculated for Cu $K_{\alpha 1}$ peak offset is equal to sd $= 0.4$ mV rms and, when referred to the input, it corresponds to about 7 el. rms.

The sensitivity of offset correction to fluctuations of the power supply voltage V_{ddm} and temperature changes was also verified. We performed measurements for different values of V_{ddm} keeping the same values of correction DACs as for the nominal bias conditions, i.e. $V_{ddm} = 2.2$ V. The effective threshold voltage spread calculated to CSA input is shown in Fig. 12. One can see that correction circuit works properly for relative wide changes in power supply voltage V_{ddm} which is common to CSA, filter stage and correction circuit. For the measured temperature range from 0 °C to 40 °C the changes of the effective threshold spread after correction were similar.

Two remarks should be added to the correction of effective threshold spread. The first one is that the correction circuit is common for two discriminators in single channel, so if we precisely tune for example threshold VT_{HIGH} (to obtain $\mathrm{sd}_{\mathrm{HIGH}} = 0.4$ mV), then the spread of the other threshold VT_{LOW} is larger $(\mathrm{sd}_{\mathrm{LOW}} = 1.8$ mV) because of the offsets difference between two discriminators and spread of this difference from channel to channel. The other aspect is the spread of the gain (calculated as sd/mean) in multichannel ASIC, given in Table II. The spread of the gain is about 0.8% and in many practical applications it is negligible. However, to obtain the best uniformity of effective threshold settings the value of the correction DACs should be recalculated for different threshold settings.

The ASIC was also tested for the spread of the noise level, using strip detectors of different pitch (50 μm, 75 μm, 100 μm) and different strip length (1 or 2 cm), and the results are summarized in Table II. The noise was calculated as a sigma of Gaussian fit to Cu $K_{\alpha 1}$ peak measured with the silicon strip detectors. The spread of ENC was calculated as the standard deviation of the noise value measured in a single 64-channel ASIC.

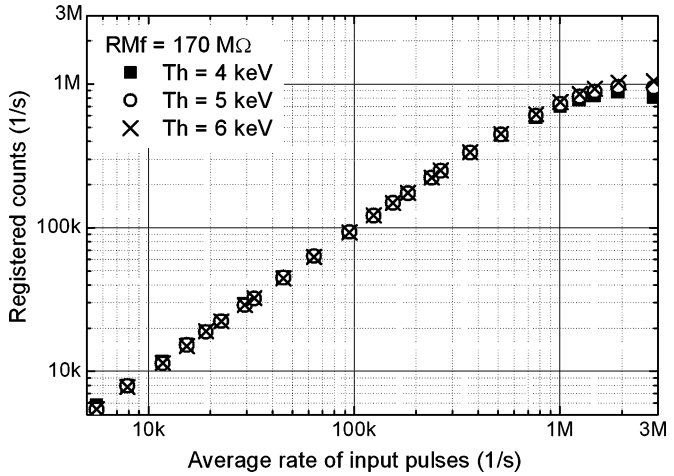

Fig. 13. Number of registered counts as functions of input pulse for different threshold settings.

V. High Counting Rate Characteristics

In order to characterize the high rate performance of the DEDIX IC we performed some tests with signals arriving randomly at the CSA input. For these tests we used photons from an X-ray tube with Cu target (8 keV) after diffraction on a LiF crystal (diffraction peak 111). Measurements were performed for modules equipped with DEDIX ICs connected to small DC diodes of rectangular shape or to AC strip detectors. During the tests we made full scans of discriminator threshold voltages for different rate of input pulses.

To eliminate the influence of the AC coupling at the input of CSA on the high rate measurements of the front-end electronics [21]–[23] most of the tests were performed with small silicon DC coupled diodes $(\mathrm{C_{diode}} = 1\ \mathrm{pF})$ connected to the DEDIX IC inputs. Fig. 13 shows a number of registered counts (for different discriminator threshold settings) versus the average rate of X-rays absorbed in silicon diode. The difference for various threshold settings above 1 MHz is because of the pile-up effect of pulses of given width at shaper output (the sequence of pulses has a Poisson distribution in time) [24], [25].

The most interesting are the measurement results of gain, offset shift at discriminator input (shaper output) and noise, as a function of the average rate of X-ray photons. The measurements were performed for different settings of CSA feedback resistance $\mathrm{R_{Mf}}$. During the measurements with X-ray tube to distinguish between the gain and the offset changes in the front-end electronics, we used additionally an external generator to inject simultaneously pulses to CSA input through the test capacitor $C_t = 75$ fF (see Fig. 2). The frequency of pulses from the generator was of an order of magnitude smaller than the frequency of pulses from the X-ray tube. The obtained results are shown in Fig. 14. The differences for the high count rate performance in the offset shift [see Fig. 14(b)] for different CSA feedback resistance are directly connected with the DC voltage shift at the CSA output for high rates of input pulses. For an extremely high value feedback resistance and a high rate of input pulses this DC voltage shift deteriorates the quality of the PZC circuit [26]. However, for the CSA feedback resistance in the range

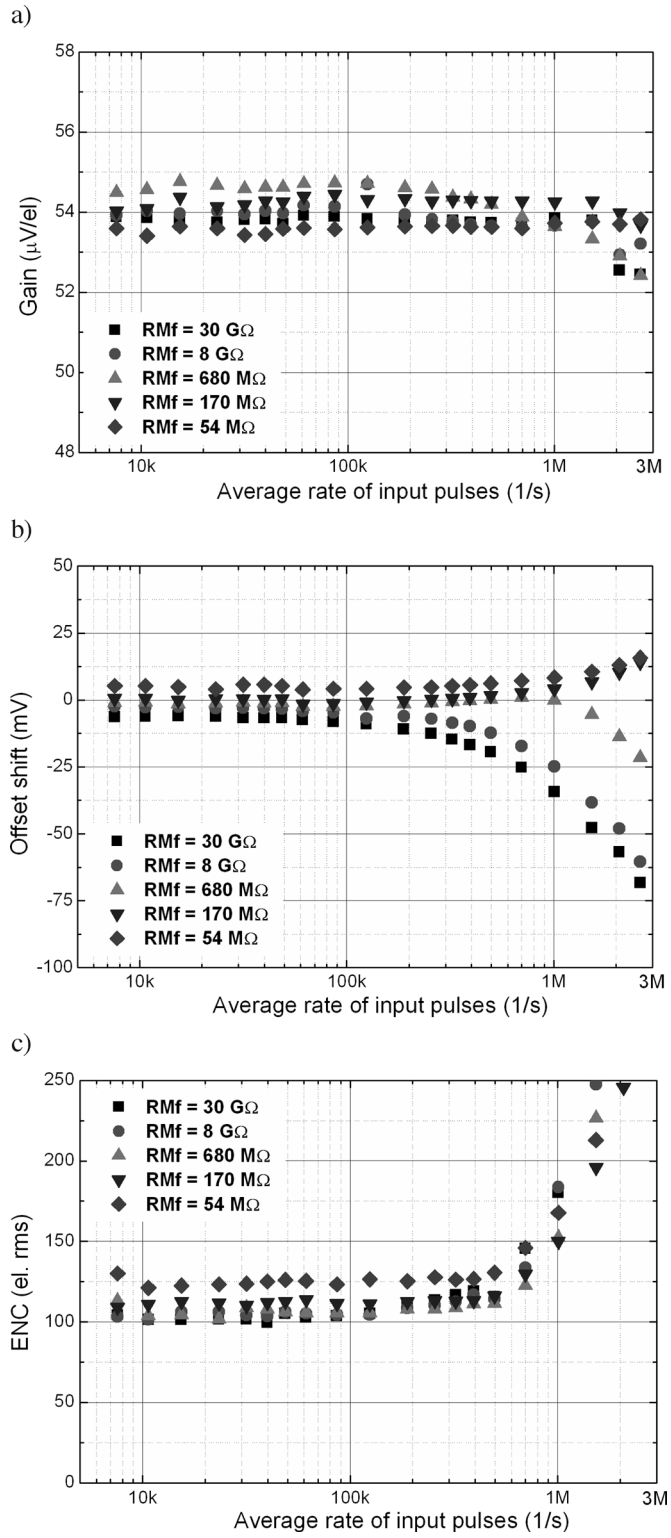

Fig. 14. High count rate characteristic of DEDIX chip: (a) gain; (b) DC level shift at discriminator input; and (c) noise.

from tens to hundreds of MΩ the gain, DC level and noise in front-end electronics do not degrade nearly up to 1 MHz of average rate of input pulses.

The noise increase observed for the higher rates of input pulses is related to the pile up effects. In the readout electronics for X- and γ-ray spectroscopy an additional pile up rejection

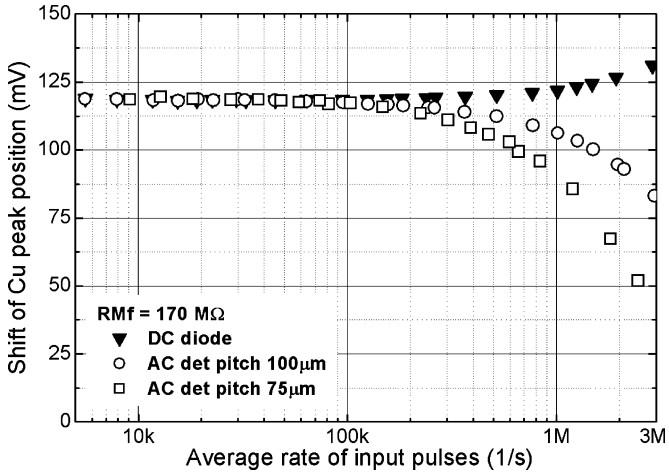

Fig. 15. Shift of the Cu K_α peak position as a function of the average rate of input pulses for DC diodes and AC coupled detectors.

TABLE III
SUMMARIZED PERFORMANCE OF DEDIX IC

Parameter	
Technology	CMOS 0.35 μm
Size	3.9 mm × 5 mm
Number of channels	64
Supply voltage	2.2V /3 V
Power dissipation per channel	5 mW
Peaking time	160 ns
ENC (*Tp* = 160 ns, *Cdet* = 1 pF)	110 el. rms
Gain	54 μV/el.
Effective threshold spread calculated to the input	7 el. rms
Number of discriminators per channel	2
Counters capacity	20-bit
Communication	
- control	LVDS standard
- data output	three state 8-bit bus

circuit is often added [27], [28]; however, this is not an issue for our applications.

Additional comments should be made about the difference in the DC and AC coupled detectors working with a high rate of input pulses. The comparison of these two cases is shown in Fig. 15. There are shifts of Cu K_α peak (measured during the threshold scan) as a function of the average rate of input pulses from X-ray tube. The shift of the Cu K_α peaks in the case of the DC detector shown in Fig. 15 can be easily understood if we compare it with results in Fig. 14(b). For the AC coupled detector we always observed a negative Cu K_α peak position shift (for all settings of R_{Mf}), produced by the AC coupling at the CSA input [21]–[23]. This shift depends on the coupling capacitor, detector bias resistor and CSA input impedance.

VI. SUMMARY

We have presented a 64-channel ASIC, which is a fast fully integrated digital readout for the silicon strip detector for low energy X-ray imaging systems. The IC performance is summarized in Table III.

Because of the additional 7-bit correction DAC in each channel, there is the possibility of precisely tuning the DC level at the discriminator inputs and selecting input pulses according to their amplitude. The properly implemented PZC circuits ensures a correct operation of the front-end electronics for input signals arriving randomly with Poisson statistics with an average rate of up to 1 MHz per channel.

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