Double-Sided, Double-Type-Column 3-D Detectors: Design, Fabrication, and Technology Evaluation

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***Abstract*—We report on the latest results from the development of 3-D silicon radiation detectors at Fondazione Bruno Kessler of Trento (FBK), Italy (formerly ITC-IRST). Building on the results obtained from previous devices (3-D Single-Type-Column), a new detector concept has been defined, namely 3-D-DDTC (Double-sided Double-Type Column), which involves columnar electrodes of both doping types, etched from alternate wafer sides, stopping a short distance (d) from the opposite surface. Simulations prove that, if d is kept small with respect to the wafer thickness, this approach can yield charge collection properties comparable to those of standard 3-D detectors, with the advantage of a simpler fabrication process. Two wafer layouts have been designed with reference to this technology, and two fabrication runs have been performed. Technological and design aspects are reported in this paper, along with simulation results and initial results from the characterization of detectors and test structures belonging to the first 3-D-DDTC batch.**

***Index Terms*—DRIE, numerical simulations, silicon radiation detectors, 3-D technology.**

I. Introduction

FUTURE high energy physics experiments at high-luminosity colliders are pushing the R&D on radiation-hard detectors at the technological frontier. In particular, the foreseen upgrade of the Large Hadron Collider (sLHC) will be able to reach a luminosity of $10^{35}\text{cm}^{-2}\text{s}^{-1}$, corresponding to equivalent hadron fluences up to 10^{16} cm^{-2} in the innermost detector layers after five years of operation [1]. Standard planar detectors are not favored for operation at these high fluences: the increase in the effective doping concentration would prevent from reaching full depletion, and charge trapping would cause the charge carrier drift length to be at most 50 μm, so that the collected charge would be dramatically decreased [2].

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Silicon detectors with three-dimensional electrodes (3-D detectors) are one of the most promising technologies available to cope with these very harsh radiation environments. 3-D detectors were first proposed by Parker and collaborators in 1997 [3]. They consist of a 3-D array of vertical columnar electrodes of both doping types, etched perpendicularly to the wafer surface and penetrating through the entire substrate. In planar detectors the depletion voltage and the collected charge depend on the substrate thickness; on the contrary, in 3-D detectors these features depend on the detector layout, i.e., on the distance between the columnar electrodes, which can be short enough to yield full depletion and high electric fields at low bias voltage, thus allowing for short collection times and high radiation hardness. In particular, electrodes can be placed at a distance comparable to the worst-case carrier drift length, so that a large Signal Efficiency (SE) is ensured. Considerable results have already been reported for these devices: among them, a SE up to 66% after irradiation with neutrons at 8×10^{15} 1-MeV equivalent neutrons/cm^2 was measured with an IR laser setup [4], [5]. Additionally, one important evolution of the 3-D concept, the so-called "active edge" [6], should be mentioned, allowing the insensitive edge region to be reduced down to about 10 μm, to be compared to few hundreds μm for standard planar detectors. This option enables building large area seamlessly tiled detector matrices, i.e., without sensor overlap within the same layer, and thus greatly facilitates the layout, reduces the material budget, and improves the momentum resolution.

The remarkable advantages of 3-D detectors over planar detectors are obtained at the expense of a rather challenging fabrication process, which involves several non-standard steps typical of micro-machining, such as Deep Reactive Ion Etching (DRIE), Chemical Mechanical Polishing (CMP) and wafer bonding [7]. As a matter of fact, the existing prototypes of these detectors were fabricated at a research laboratory (the Stanford Nanofabrication Facility) and the feasibility of a large scale production by an industrial foundry has not been demonstrated yet. In this respect, the development of modified 3-D detector architectures allowing for a simplified fabrication technology is worth investigation, and some research institutes are involved in this effort [8].

In the past few years, Fondazione Bruno Kessler (FBK, formerly ITC-IRST, Trento, Italy) has been developing 3-D detector technologies in collaboration with the Italian National Institute for Nuclear Physics. As a first step in this activity, mainly aimed at studying the critical steps of the technology, we have proposed, fabricated and extensively tested a simplified 3-D geometry (namely, 3-D-STC [9]) having columnar

electrodes of one doping type only (n^+) and not penetrating all the way through the substrate (on the back-side a uniform p^+ ohmic contact is present). Encouraging results have been obtained, among them low leakage currents (~ 1 pA/column), a high process yield [10], [11], and a good Charge Collection Efficiency (CCE) even at low voltage [12]. Nevertheless, 3-D-STC detectors have some important drawbacks: once full depletion between columns is achieved, the electric field strength in the inter-column region can not be increased further by increasing the reverse voltage, and its value depends on the substrate doping concentration only [9]. As a consequence, low-field regions exist within the active volume, that affect the charge collection mechanism and prevent from obtaining a uniform response to particles. Moreover, the current signal shows a fast peak component (in the order of a few ns) but also a slow tail (up to several μs) due to hole diffusion towards the backplane [13]. The long overall collection times limit the radiation hardness of these detectors and also cause ballistic deficit when fast readout systems are employed. These aspects have been studied by numerical device simulations and also observed experimentally by testing 3-D-STC strip detectors connected to the 40 MHz ATLAS SCT Endcap electronics (ABCD3TA chip, with peaking time of 20 ns) [14]. In particular, position resolved charge collection measurements performed with IR pulsed laser evidenced a reduced charge collection from low-field regions both before irradiation [15] and after irradiation [16].

In order to overcome the performance limitations mentioned above, while minimizing the increase in process complexity, an alternative detector concept has been defined, that is the object of this paper. It will be referred to as 3-D-DDTC (Double-sided Double-Type Column) since it involves columnar electrodes of both doping types etched from opposite sides of the wafer. The remaining part of this paper is organized as follows: the 3-D-DDTC detector concept is explained in Section II with the aid of numerical device simulations; in Section III the design and the fabrication technology of the first prototypes are reported; in Section IV initial results from the electrical characterization of detectors and test structures are discussed. Conclusions are drawn in Section V.

II. Detector Concept and Simulations

Building on the experience gained with 3-D-STC detectors, we have developed 3-D-DDTC detectors, which are aimed at performance enhancement while maintaining a reasonably simple process. These detectors are being considered as an alternative to standard 3-D detectors in the ATLAS Pixel Detector upgrade for the sLHC [8], possibly allowing for a reduction of process complexity and cost. A similar approach is being independently developed by the Centro National de Microelectronica (Barcelona, Spain) [17].

3-D-DDTC detectors have 10-μm wide columnar electrodes of both doping types etched by DRIE from alternate wafer sides and stopping a short distance (d, ideally not exceeding few tens of μm) from the opposite surface, as shown in Fig. 1: junction columns are etched from the front side, whereas ohmic columns are etched from the back side. Junction columns are read-out columns and can be arranged in pad, strip or pixel configurations. Ohmic columns are all connected together by surface

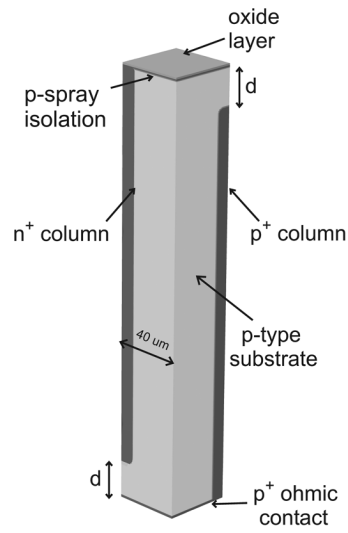

Fig. 1. 3-D sketch of a 3-D-DDTC detector on p-type substrate. A quarter of a unit cell representing a typical pattern present in the layout is shown: the half-pitch between columns of the same doping type is 40 μm.

doping and metallization on the back side. This approach offers some advantages over standard 3-D detectors in terms of process complexity: i) since columns are not etched all the way through the substrate, two process steps can be avoided, i.e., wafer bonding and final mechanical lapping of the sacrificial support wafer; ii) since the DRIE etching is not performed twice from the same wafer side, it is not necessary to grow a thick protection layer after the first DRIE step; iii) similarly to 3-D-STC detectors, columns are not filled with polysilicon, thus avoiding the related deposition and etching steps. The main drawbacks of 3-D-DDTC detectors are the lack of active edge, and the fact that the empty electrodes are dead regions, the latter problem being however attenuated if detectors are tilted by a few degrees, as demonstrated by testbeam results on standard 3-D detectors [18].

From the viewpoint of signal efficiency and radiation hardness, 3-D-DDTC detectors are expected to yield performance comparable to standard 3-D detectors, although a potential concern is represented by the regions in between the column tips and the opposite surface of the wafer, where the electric field is lower. In order to investigate the characteristics of 3-D-DDTC detectors and to compare their performance to 3-D-STC and standard 3-D detectors, numerical device simulations have been performed using Synopsys software [19]. Keeping in mind the main application of these detectors in the ATLAS Pixel upgrade, devices made on p-type substrates are considered in the simulations, due to their superior radiation hardness [20]. Because of symmetry considerations [9], [21], the simulation domain can be reduced to a quarter of a unit cell (see Fig. 1), thus limiting the mesh complexity and the simulation time. The pitch between columns of the same doping type is 80 μm, so that the distance between junction columns and ohmic columns is $40\sqrt{2}$ μm. This structure is representative of a typical pattern present in the layout of n-on-p 3-D diode and strip detectors. The substrate has a thickness of 250 μm and a doping concentration of 2×10^{12}cm^{-3}. Simulations also account for a fixed charge

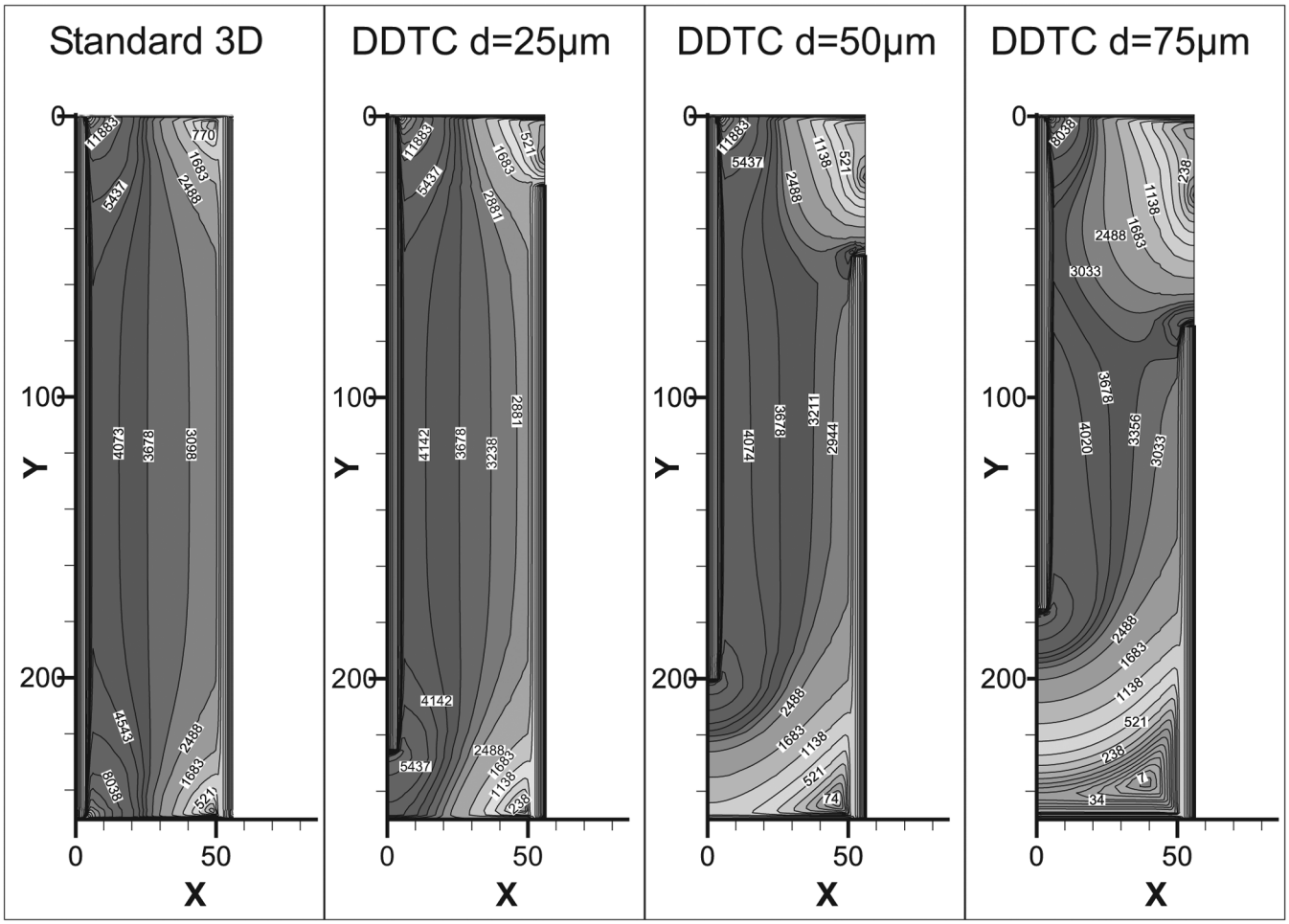

Fig. 2. Simulated electric field distribution in a 2-D cross-section taken along the cell diagonal. X and Y axis units are in μm. The center of the junction column is at $x = 0$, the center of the ohmic column is at $x = 40\sqrt{2}$ μm. The isolines show electric field values in V/cm. Four cases are represented, from left to right: standard 3-D and 3-D-DDTC with $d = 25$, 50, and 75 μm, respectively.

density at the silicon/silicon oxide interface with a concentration of $2 \times 10^{11}\text{cm}^{-2}$. Surface isolation between n^+ regions is realized with a p-spray implant [22], which has already been implemented in the 3-D-STC technology [11]. P-spray is also present on the back-side of standard 3-D detectors, whereas a p^+ region provides an extended ohmic contact on the back side of 3-D-DDTC detectors. Values of all parameters are representative of FBK technology.

Fig. 2 shows the electric field distribution at a reverse bias of 16 V (i.e., slightly beyond lateral depletion, which is achieved at 10 V) in a 2-D cross-section taken along the diagonal of the simulated cell (see Fig. 1), i.e., from the center of the junction column $(x = 0)$ to the center of the ohmic column $\left(= 40\sqrt{2}\ \mu\text{m}\right)$. Four different detector geometries are compared: a standard 3-D detector (i.e., with both columns penetrating all the way through the substrate) and three 3-D-DDTC detectors having d equal to 25, 50 and 75 μm, respectively.

In the standard 3-D detector, the electric field distribution is mainly horizontal, as expected; nevertheless, deviations from this trend can clearly be observed close to the surfaces, because of the p-spray layer. The peak electric field is about 10^4 V/cm at the n^+/p-spray junction on both wafer sides. In spite of the shorter column depth, the electric field distribution in 3-D-DDTC detectors with $d = 25$ μm is comparable to that of standard 3-D detectors, whereas it becomes more and more distorted as d is increased. The peak electric field is always at the n^+/p-spray junction on the front side, but high electric field values can also be observed at both column tips as d is increased. Moreover, low-field regions can be observed in the areas between the column tips and the opposite surface: the shorter the columns, the larger the low-field regions. It should be noted that increasing the bias voltage can of course increase the electric field in the region where the columns overlap, and, to a lower extent, in the bottom region, i.e., in between the junction column tips and the ohmic contacts. However, it can only slightly change the electric field distribution in the top region, i.e., in between the ohmic column tips and the opposite surface. Thus, it is evident that d should be kept small with respect to the wafer thickness in order to achieve a fast and efficient charge collection, as can be appreciated with the aid of Fig. 3.

Fig. 3(a) shows the simulated current signals induced by a minimum ionizing particle impinging on the detector perpendicularly to the surface at 5 μm from the ohmic column. Results refer to a bias voltage of 16 V. The particle track and the bias voltage are chosen as representative of a worst-case

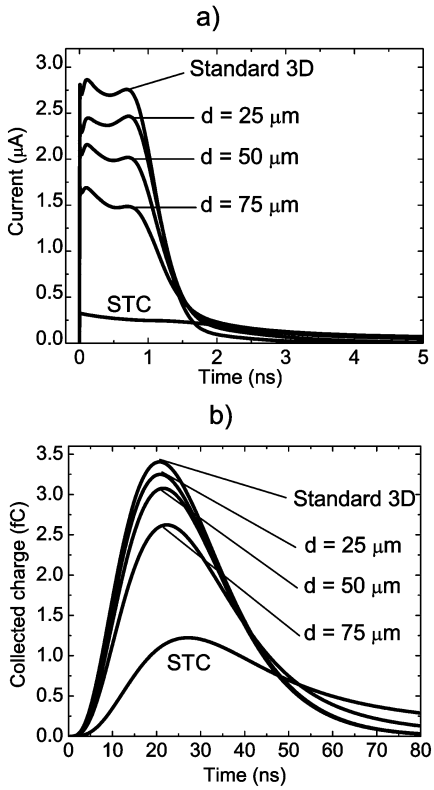

Fig. 3. Simulated transient signals in 3-D detectors of different geometries and biased at 16 V in response to a minimum ionizing particle: a) current signals; b) equivalent charge signals at the output of a semi-gaussian $CR-(RC)^3$ shaper with 20 ns peaking time.

condition from the viewpoint of the electric field configuration. 3-D-DDTC detectors with three d values are compared to a standard 3-D detector and also to a 3-D-STC detector (i.e., without the ohmic column). As it can be seen, all 3-D-DDTC detectors show a much higher current peak and a much shorter collection time with respect to the 3-D-STC detector. The current signals of 3-D-DDTC detectors become similar to that of the standard 3-D detector if d is kept small. In order to make the comparison between the different geometries more meaningful, the current signals of Fig. 3(a) were post-processed to account for a semi-gaussian $CR-(RC)^3$ filter that emulates a fast, ATLAS-like readout electronics with 20 ns peaking time. The results are shown in terms of collected charge in Fig. 3(b) and demonstrate that 3-D-DDTC detectors can be nearly as efficient as standard 3-D detectors at these short peaking times.

Keeping in mind the possible application of these detectors in the ATLAS Pixel upgrade, simulations accounting for severe radiation damage effects have also been performed. An irradiation fluence of 10^{16} 1-MeV equivalent neutrons/cm^2, corresponding to 5 years of operation in the pixel b-layer at sLHC, has been considered. The most promising among 3-D-DDTC detector geometries ($d = 25$ μm) was compared to a standard 3-D detector. Surface damage is included by setting the oxide charge density at its saturation value (3×10^{12}cm^{-2} [23]). As for the displacement damage, a two-step approach has been adopted, incorporating the effective doping concentration in the simulations and then processing the simulated current signals ($I_{\rm sim}(t)$) to account for charge trapping. In particular, the effective doping concentration ($N_{\rm eff}$) has been calculated as

$$N_{\rm eff} = N_{\rm eff0} + g \cdot \phi \tag{1}$$

where $N_{\rm eff0}$ is the pre-irradiation substrate doping concentration, $g = 0.02$ cm^{-1} is the acceptor introduction rate and ϕ is the fluence [24]. The charge trapping effect on the current signals has been calculated as

$$I_{\rm trapping}(t) = I_{\rm sim}(t) \cdot e^{-t/\tau} \tag{2}$$

where $1/\tau$ represents the trapping probability extracted from [24].

Fig. 4 shows results relevant to transient simulations of 3-D detectors biased at 400 V (i.e., beyond lateral depletion, which is achieved at about 350 V at the considered fluence) in response to a minimum ionizing particle with the same characteristics as in the pre-irradiation case. In Fig. 4(a) current signals are shown. A much higher peak value and a much shorter duration with respect to the pre-irradiation case can be observed. It should be stressed that after such a large radiation fluence, even if lateral depletion is achieved and the electric field strength is very high, carrier trapping is the limiting factor for charge collection. In fact, charge carriers have a very short lifetime (less than 0.5 ns) and, as a consequence, their mean drift length is reduced to some tens of μm. The collected charge is indeed lower ($\sim 50\%$) than in the pre-irradiation case, as can be seen in Fig. 4(b). The same figure also confirms that even after irradiation a 3-D-DDTC detector with $d = 25$ μm can be almost as efficient as standard 3-D detectors, the difference between the height of the two charge signals being about 10% in this worst-case condition.

III. Detector Design and Fabrication

In order to experimentally validate the 3-D-DDTC approach, two wafer layouts have been designed, namely 3-D-DTC-1 and 3-D-DTC-2, to be fabricated on n-type and p-type substrates, respectively. As already mentioned, p-type substrates are more appealing for the ATLAS Pixel upgrade: in p-type substrates the main junction remains always on the same side (after irradiation the so-called "type-inversion" does not occur) and read-out electrodes collect electrons which are faster than holes and have a lower trapping probability [20].

However, the first 3-D-DDTC detectors were fabricated on n-type substrates, mainly because of a delay in the wafer procurement. It should be stressed that at the time of starting the detector fabrication the DRIE equipment was not available at FBK, so that column etching had to be performed as an external service at IBS (France). Previous experience with this company indicated that a maximum column depth of about 180 μm could be reliably achieved. Thus, in order to obtain a small value for the distance d, wafers with a thickness of 200 μm should be used, which were not available and whose procurement took several months. Therefore, it was decided to fabricate the first batch of 3-D-DDTC detectors on standard (300 μm thick) n-type wafers, which also allow for a simpler technological process because the surface isolation by p-stop or p-spray implantation is not necessary. Of course these prototypes are not expected to yield very good dynamic performance because the attainable d values are

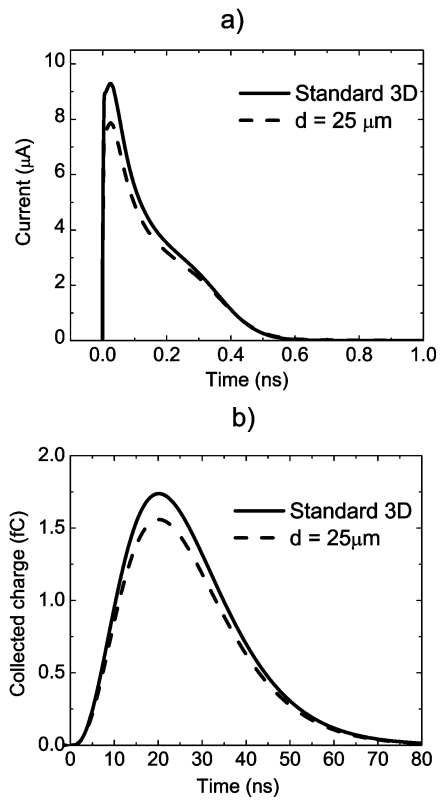

Fig. 4. Simulated transient signals in 3-D detectors of different geometries irradiated at 1×10^{16} 1-MeV eq. n/cm^2 and biased at 400 V in response to a minimum ionizing particle: a) current signals; b) equivalent charge signals at the output of a semigaussian $CR-(RC)^3$ shaper with 20 ns peaking time.

large. Nevertheless, they are appropriate for a first evaluation of the 3-D-DDTC technology, with particular reference to two new aspects: a layout with high column density and p^+ column doping from Boron solid source. Optimized performance is expected from the second batch of detectors, made on 200 μm thick p-type substrates, whose fabrication is under way.

The main features of the two detector batches are reported in Table I. The 3-D-DTC-1 layout contains mainly strip detectors and test structures, in order to ease the electrical tests and the bonding to standard read-out chips for functional characterization. In particular, strip detectors are suitable to be read-out with the ATLAS SCT front-end electronics. 3-D short strip detectors could indeed become an option for tracking at the sLHC [25]. The 3-D-DTC-2 layout is mainly oriented to pixel detectors: 22 ATLAS pixel detectors (single chips) featuring different layout options (i.e., number of columns per pixel) are present, along with 6 CMS pixel detectors (single chips) and other CMS pixel test structures.

The fabrication of the 3-D-DTC-1 batch was completed at FBK at the end of 2007. The substrates are n-type, Float Zone, with $\langle 100 \rangle$ crystal orientation and a nominal resistivity larger than 6 $\mathrm{k}\Omega \cdot \mathrm{cm}$. In the following, the main process steps are summarized with the aid of Fig. 5.

a) A thick oxide is grown, to be used as a masking layer for the DRIE step on the back side. The oxide is patterned on the back side and the first DRIE step is performed.

TABLE I
MAIN FEATURES OF THE TWO 3-D-DDTC DETECTOR BATCHES

Batch	3D-DTC-1	3D-DTC-2
Substrate type	n-type	p-type
Substrate thickness	300μm	200 μm
Column depth	180 μm	180 μm
Strip design	AC/DC coupled,	AC/DC coupled,
Strip pitch	80/100 μm	80/100 μm
Pixel design	ALICE, MEDIPIX1	ATLAS, CMS

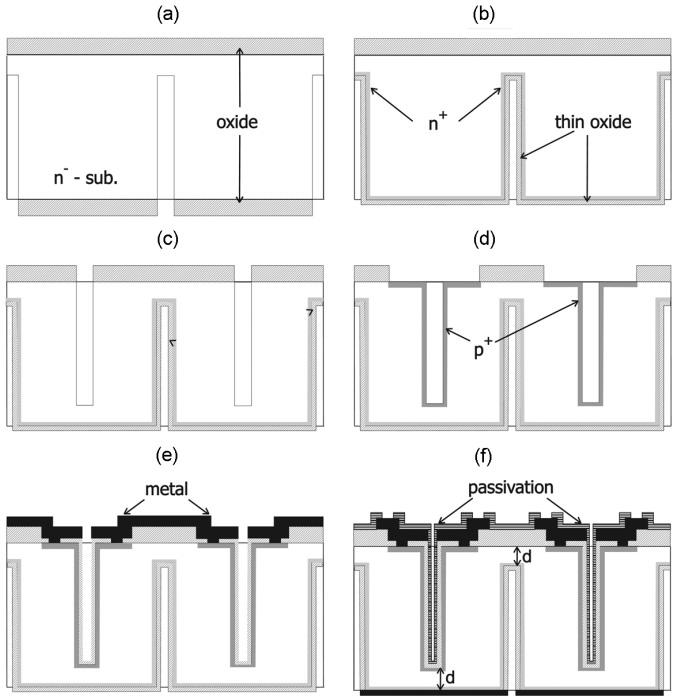

Fig. 5. Main steps of the 3-D-DDTC fabrication process on n-type substrate.

b) The thick oxide layer is removed from the back side and Phosphorus is diffused from a solid source into columns and at the back surface to obtain a good ohmic contact. A thin oxide layer is later grown to avoid out-diffusion of the dopant.

c) The oxide layer on the front side is patterned and the second DRIE step is performed for the column etching.

d) The thick oxide layer on the front side is removed from a ring shaped region surrounding holes; Boron is diffused from a solid source into the columns and at the open surface region to ease contact formation.

e) An oxide layer is grown at the surface and in the columns to prevent the dopant out-diffusion; an additional oxide layer (TEOS) is deposited; then, contact holes are defined and etched through the oxide at the surface; aluminum is sputtered and patterned.

f) The final passivation layer is deposited on the front side, whereas on the back side, after removal of the oxide layer, aluminum sputtering provides a uniform metal electrode. Finally, the passivation layer on the front side is patterned to define the access regions to the metal layer.

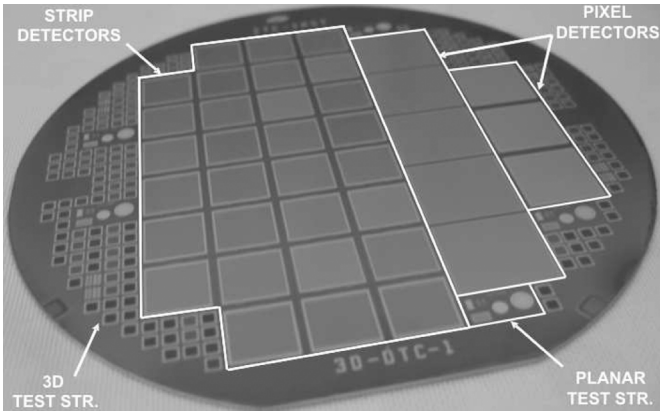

Fig. 6. Photograph of a processed wafer from the 3-D-DTC-1 batch.

Fig. 6 shows a photograph of a processed wafer. Different blocks are indicated, including strip detectors (30 dice) and pixel detectors (8 dice), which cover the center of the wafer, and test structures (both planar and 3-D) which are placed at the wafer periphery. It is worth providing some details about test structures, which will be considered in the experimental part of this paper.

Five sets of planar tests structures are present on the wafer. Each of them contains one diode (4 mm^2 area) with guard ring, one gated-diode, one MOS capacitor and a few Van der Pauw resistors. Planar test structures are aimed at process quality control and at extracting some relevant parameters.

3-D test structures are basically 3-D diodes, whose electrodes can consist of either a single column or a 2-D column array. As an example, Fig. 7 shows the photograph of a 3-D diode featuring an inner array of columns all connected together by strip-like p^+ surface diffusions. A square metal frame contacts the outermost columns and four probing/bonding pads are available at the corners. Around the inner array is a double frame of columns, all connected together by p^+ surface diffusion and metal. This structure acts as a 3-D guard ring, which is to be biased at the same voltage as the diode during measurements. In turn, the 3-D guard ring is surrounded by two narrow planar guard rings (to be left floating during the measurements), which are aimed at improving the surface breakdown performance. The ohmic electrode of the 3-D diode consists of an array of n^+ columns etched from the back-side and all connected together by surface diffusion and metal. Eight versions of multi-column 3-D diodes are indeed available, each of them having a large multiplicity on wafer, and differing in the inner array layout and geometrical details, as summarized in the following:

- p^+ surface diffusion: strip-like fingers or uniform layout;
- array size and column pitch: 16×16 columns at 100 μm pitch or 20×20 columns at 80 μm pitch (both resulting in the same diode area of 2.56 mm^2);
- ohmic electrode: array of n^+ columns plus n^+ surface diffusion (in the following referred to as "dtc") or n^+ surface diffusion only (in the following referred to as "stc"), the latter solution corresponding to that implemented in the earlier 3-D-STC technology [10].

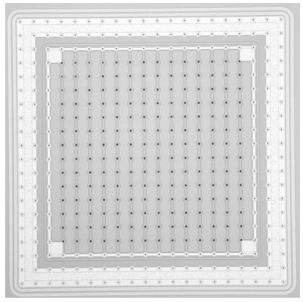

Fig. 7. Photograph of a 3-D diode from the 3-D-DTC-1 batch.

Finally, single column 3-D diodes (i.e., diodes having the junction electrode made of one column only) are also available in different versions featuring similar layout/geometrical options as mentioned for the multi-column ones.

IV. Experimental Results and Discussion

The electrical characterization of test structures and strip detectors belonging to the 3-D-DTC-1 batch has been carried out. Measurements were performed at room temperature and under dark conditions by using a probe-station to contact the devices. For the sake of conciseness, only results relevant to planar and 3-D diodes are reported in the following.

A. Planar Test Structures

Fig. 8(a) shows the leakage current as a function of the reverse voltage in planar test diodes. The leakage current is low and the curve shapes suggest that the main contribution is from thermal generation in the depleted bulk, as expected from the geometry of the devices. The corresponding bulk generation lifetime is about 20 ms. Leakage current measurements were also repeated over a wider reverse voltage range, and junction breakdown was always found to occur on the guard ring at voltages exceeding 350 V.

Capacitance measurements in reverse bias were also performed. From the $1/C^2$-V curves (see Fig. 8(b), full depletion voltage values in the range from 8 V to 10 V can be extracted, corresponding to a very low substrate doping concentration, in the order of 1×10^{11} cm^{-3}.

Table II summarizes the results obtained from diodes and other planar test structures, including the surface related parameters. The surface generation velocity was extracted from gated-diodes. Its value is very low, as typically achieved on $\langle 100 \rangle$ substrates [26]. On the other hand, the fixed charge density extracted from MOS capacitors is much higher than expected. Further tests pointed out that this effect was caused by the TEOS layer, wherein the positive charge density was much higher than normal.

B. 3-D Diodes

Current-voltage and capacitance-voltage measurements were performed on a large number of 3-D diodes belonging to 4 wafers. Selected results from these tests are reported in the following.

Fig. 9(a) shows the leakage current as a function of the reverse voltage in some 3-D diodes of the stc type (i.e., without

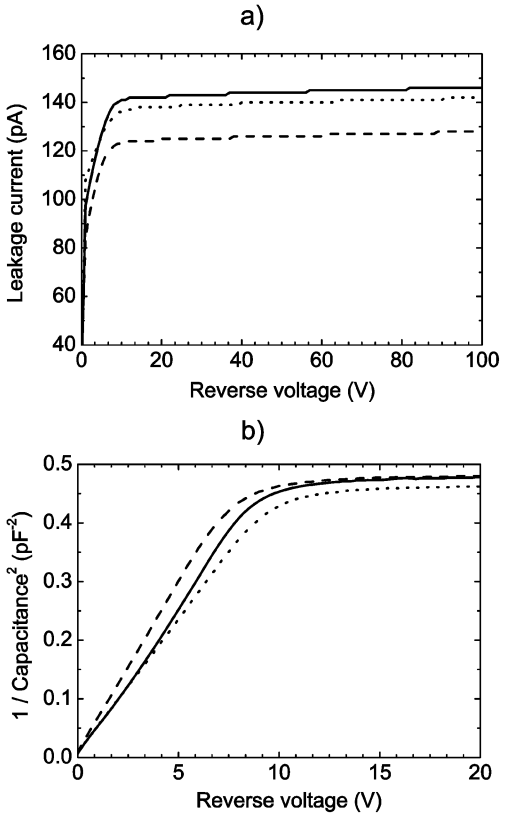

Fig. 8. (a) Leakage current versus voltage, and (b) $1/\mathrm{Capacitance}^2$ versus voltage curves in three planar test diodes from the 3-D-DTC-1 batch.

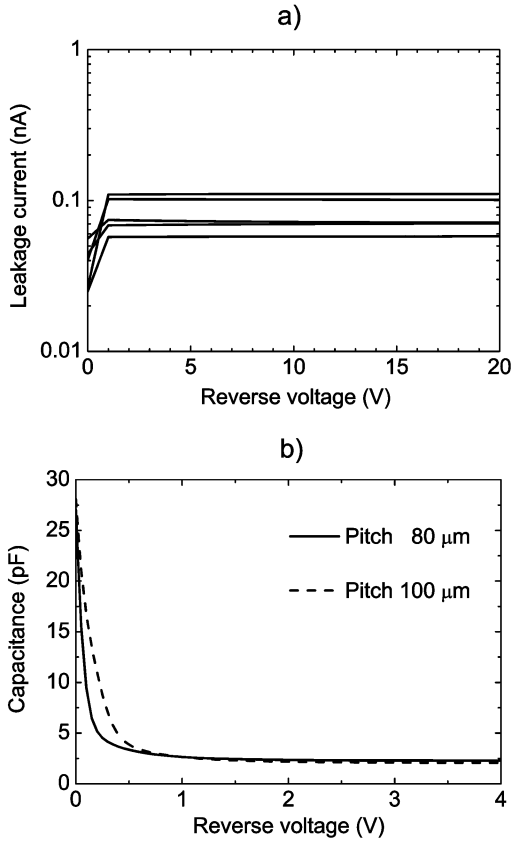

Fig. 9. (a) Leakage current versus voltage, and (b) capacitance versus voltage curves of 3-D test diodes (stc type, i.e., without ohmic columns) from the 3-D-DTC-1 batch.

TABLE II
SUMMARY OF THE ELECTRICAL AND TECHNOLOGICAL PARAMETERS EVALUATED FROM PLANAR TEST STRUCTURES

Parameter	Unit	Value
Substrate doping	10^{11} cm^{-3}	1.2±0.2
Leakage current density	nA/cm^2	3.2±0.3
Breakdown voltage	V	> 350
Bulk generation lifetime	ms	21±3
Surface generation velocity	cm/s	1.5±0.7
Field oxide thickness	nm	575±20
Fixed oxide charge density	10^{11} cm^{-2}	4.4±0.6

the ohmic columns). Diodes with different layout (strip and uniform surface diffusion) and different column number/pitch are considered. In all cases, the current curves saturate at very low voltage, due to the low depletion voltage [see Fig. 9(b)]. The leakage current is very low, its value being much lower than 1 pA/column. No sign of breakdown can be observed within the considered voltage range, neither in the diode current nor in the guard ring current (not shown). From other measurements performed over a wider voltage range, breakdown was always found to occur on the guard ring at voltages typically exceeding 200 V.

Fig. 9(b) shows the capacitance as a function of the reverse voltage in two diodes featuring different pitch between the columns. The curves exhibit a sharp decrease and then almost saturate as lateral depletion is reached. The depletion mechanism is indeed the same as described in [10]: depletion first proceeds sidewards between columns and then backwards from the column tips to the ohmic contact like in a planar detector. As expected, lateral depletion is reached at a slightly lower voltage for the 80 μm pitch. Afterwards, the capacitance values are almost the same for the two pitches because, when the depletion proceeds towards the back side like in a planar diode, the capacitance, to first approximation, depends only on the diode area [10].

The C-V curves of Fig. 9(b) were further analyzed to extract the substrate doping concentration as a function of the depletion depth [10]. As an example, results relevant to two diodes are reported in Fig. 10: as can be seen, the depletion depth below the columns reaches values of 110–120 μm, so that one can infer the column depth values to be 180–190 μm, in good agreement with the expected DRIE performance and with measurements made with SEM on test wafers (see Fig. 11).

Fig. 12(a) shows the leakage current as a function of the reverse voltage in some 3-D diodes of the dtc type (i.e., with the ohmic columns). As can be seen, for some diodes the I-V characteristics are similar to those of the stc ones, with very low saturation values. On the other hand, in some other diodes, a current rise can be observed at low voltage. This phenomenon is present on both diode and guard ring currents (not shown), but more frequently on diodes, thus suggesting a possible dependence on the number of columns (guard rings have a lower number of columns than diodes: 144 versus 256 for the 100 μm pitch, 176 versus 400 for the 80 μm pitch). The current rise is suspected

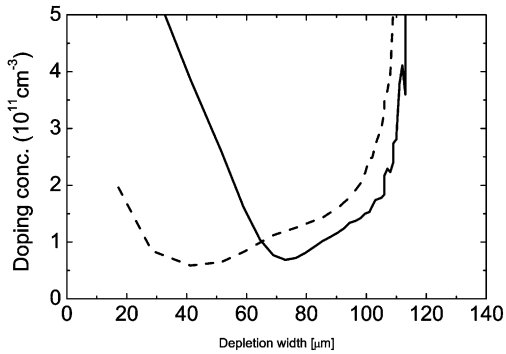

Fig. 10. Substrate doping concentration as a function of depletion depth below the column tips as obtained from C-V measurements of 3-D test diodes (stc type).

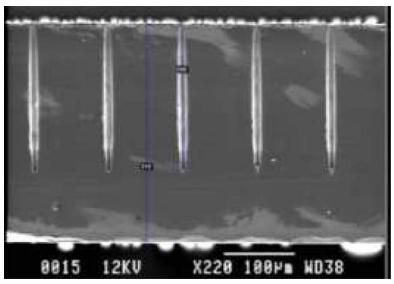

Fig. 11. SEM micrograph of a test wafer after DRIE.

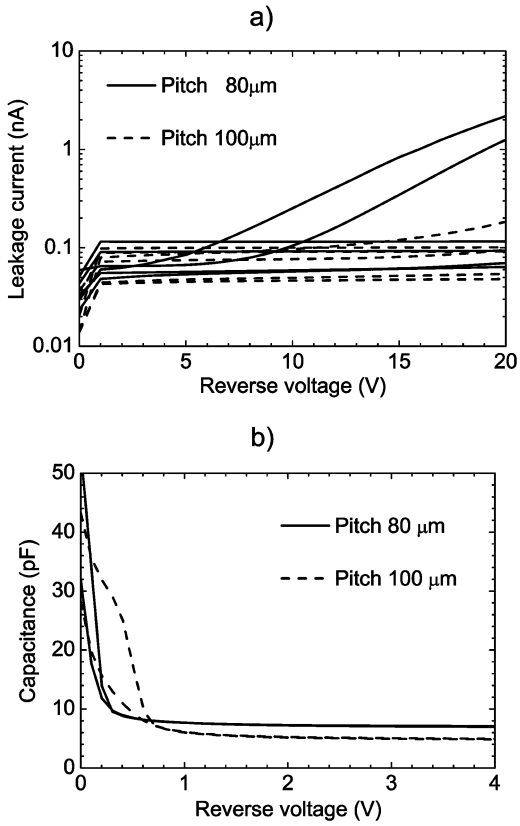

Fig. 12. (a) Leakage current versus voltage, and (b) capacitance versus voltage curves of 3-D test diodes (dtc type, i.e., with ohmic columns) from the 3-D-DTC-1 batch.

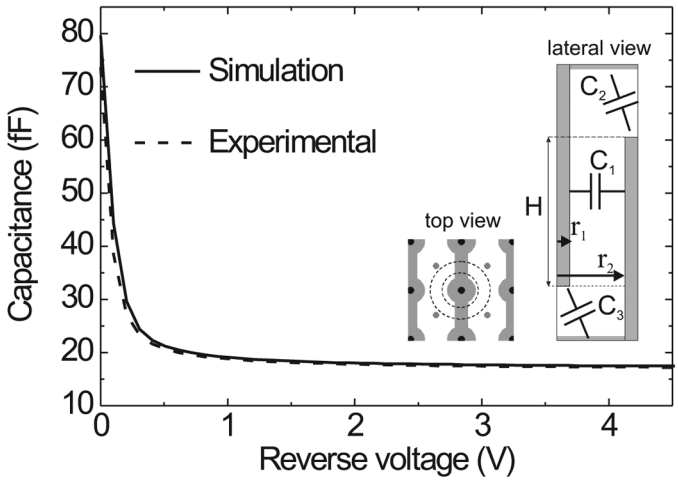

Fig. 13. Experimental and simulated capacitance versus voltage curves of a single column 3-D test diode (dtc type, pitch 80 μm). Schematic drawings of the structure (top view and lateral view) are shown in the insets.

to be caused by defects on the column walls, but further investigations are necessary to gain deeper insight into this problem. Nevertheless, it should be stressed that the current reaches high values only at bias voltages largely exceeding the full depletion voltage.

Fig. 12(b) shows the capacitance as a function of the reverse voltage in a subset of the 3-D diodes considered in Fig. 12(a), chosen as representative of the different layout options (column pitch and surface diffusion geometry). The C-V curves are very similar to those obtained from stc diodes. Nevertheless, it should be noted that in dtc diodes the main contribution to the capacitance is due to the junction-to-ohmic column capacitance. As a matter of fact, the saturation values of the capacitance for dtc diodes are higher than for the stc ones and, among dtc diodes, they are higher for the 80 μm pitch both because of the larger number of columns and of the shorter distance between them. Fig. 12(b) also evidences how the layout of the surface diffusion impacts on the capacitance value at very low voltage, due to the perimeter contribution. In diodes having a uniform surface diffusion, the perimeter contribution is absent, so that the capacitance value at low voltage is smaller than for diodes where the surface diffusion has a strip-like geometry. This effect is enhanced by the rather high oxide charge density, and eventually vanishes when lateral depletion is reached.

Dividing the diode total capacitance at full depletion by the number of columns, capacitance values in the range from 18 to 20 fF are obtained for dtc diodes. The same values were also confirmed by direct capacitance measurements performed on single column test-structures (see Fig. 13).

Comparing capacitance measurements with simulations and analytical calculations, it was also possible to estimate the depth of the ohmic columns, adopting the two following procedures.

1) AC (small signal) simulations were performed using the same junction column depth as extracted from stc diodes (190 μm), and the ohmic column depth as a parameter,

TABLE III
SUMMARY OF THE ELECTRICAL AND TECHNOLOGICAL PARAMETERS EVALUATED FROM PLANAR TEST STRUCTURES

Parameter	Unit	Value (stc)	Value (dtc)
Junction column depth	μm	180-190	180-190
Ohmic column depth	μm	n.a.	160-170
Lateral depletion voltage	V	< 0.5	< 0.5
Full Depletion (FD) voltage	V	~ 1.5	~ 1.0
Leakage current @ FD	pA/col.	0.1 - 0.5	0.1 - 0.7
Breakdown voltage	V	>200	10 - 210
Back plane capacitance	fF/col.	5 - 8	18 - 20

which was varied from 150 to 200 μm, in 5 μm steps. The best-fit simulation indicates the most probable value of the ohmic column depth. As an example, the simulated C-V is compared to the experimental one in Fig. 13, showing a very good agreement.

2) Keeping in mind the geometrical characteristics of the detectors, which are summarized in the inset of Fig. 13, the capacitance between the junction column and the ohmic column (C_1 in the inset of Fig. 13) can be approximated by calculating the capacitance of a cylindrical capacitor [27]

$$C_{\mathrm{cyl}} = 2\pi\varepsilon_{Si}\frac{H}{\ln\left(\frac{r_2}{r_1}\right)} \tag{3}$$

where ε_{Si} is the electrical permittivity of silicon; H is the overlap between the junction column and the ohmic column; r_1 and r_2 are the inner and outer radii of the cylinder, respectively. As also confirmed by simulations, C_1 corresponds to about 90% of the total capacitance between the junction column and the back plane; hence, (3) can be used to extract the most probable value of H.

Both methods were applied to 3-D dtc diodes with 80 and 100 μm pitches, leading to the same column depth value of 165 μm, slightly lower than the design value.

Table III summarizes the main electrical and technological parameters evaluated from 3-D diodes.

V. CONCLUSION

We have reported on the latest developments on 3-D detectors at Fondazione Bruno Kessler. The first prototypes of a new version of detector (3-D-DDTC), featuring columnar electrodes of both doping types etched from alternate wafer sides, and stopping a short distance from the opposite surface, have been designed and fabricated. Initial results from the electrical characterization of detectors and test structures demonstrate the viability of this technological approach. Detectors exhibit a very low depletion voltage, in the order of 1 V. The leakage current values are very low and comparable to typical values for good planar processes. This implies that the two column-etching steps by DRIE do not cause any detrimental effect on the substrate in terms of generation lifetime, also in the case of high column density layouts as those here adopted. Early breakdown problems have been observed on some devices, which are likely to be ascribed to local defects on the column walls. This effect is still under investigation. Nevertheless, all detectors can be operated up to bias voltages comfortably higher than their full depletion voltage. Capacitance values are of course higher than those of planar detectors, but still adequate to allow for low noise figures in case of pixels with properly designed columnar electrodes. In spite of the non optimized column depths, these detectors are expected to yield a significantly improved charge collection performance with respect to the previous 3-D-STC detectors, as predicted by numerical simulations. Functional tests with IR laser and a β source setup are under-way.

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