TEST

LEMO-00D

Threshold control circuit

Stretch time control

Hysteresis control

Input (J8) and output (J5) control connecors

3-NINOASIC's OR summing stage

LVDS reseiver

OR48 LVDS driver

NINOASIC8-76N

Bottom 0V

Projet/ Project:		Resp.:	
Ensemble/ Set:	Echelle/scale	Designer: Oussenko E.	
Sous-ensemble/ Underset:		Drawn: Oussenko E.	25/04/2004
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